CROSSVOLT™ LOW VOLTAGE LOGIC SERIES

DATABOOK

1996 Edition

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Introduction

CROSSVOLT*™** (krôs'vōlt) ***adj. **[cross + voltage]** providing translation (not frustration) between different digital signal levels (e.g. 5V to 3.3V translation) in order to ease the migration from one signal level to another.

National Semiconductor's *CROSSVOLT* Low Voltage Logic Series provides low voltage logic families and specialized translators for low supply voltage and mixed supply voltage applications. Currently this means most of our 3.3V logic, while designed for 3.3V operation, will interface to 5V signals.

By offering this 5V tolerance feature at no extra cost, National's *CROSSVOLT* logic allows system designers the flexibility to choose either 3.3V or 5V system components based on performance, price, availability, etc. This shortens time to market, allows the use of components with the latest features, and removes single supply cost/availability constraints, so that you can provide your customers high value systems quickly and at a low cost.

As supply voltages drop and new signalling technologies are adopted, National's *CROSSVOLT* series of products will continue to provide translation to help you move quickly into the future.

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Definition of Terms

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Low Voltage Logic Selection Guide

Gates

Function/Description	Type	LCX	LVX	LVQ	LVT
Quad 2-Input NAND	00	x, Tiny	x	x	
Quad 2-Input AND	08	x, Tiny	x	x	
Quad 2-Input OR	32	x, Tiny	x	x	
Quad 2-Input NOR	02	x, Tiny	x	x	
Hex Inverter	04	x, Tiny	x	x	
Hex Inverter with OC Outputs	05	x			
Triple 3-Input NAND Gate	10	x			
Triple 3-Input AND Gate	11	x			
Hex Schmitt Trigger Inverter	14	x, Tiny	x	x	
Quad 2-Input NAND with OC Outputs	38	x, Tiny			
Quad 2-Input Exclusive-OR	86	x, Tiny	x	x	

Flip-Flops

Function/Description	Type	LCX	LVX	LVQ	LVT	Data Inputs	TRI-STATE® Outputs	Master Reset
Dual D	74	x	x	x		2	No	No
Dual JK	109	x				2	No	No
Dual JK	112	x				2	No	No
Hex D	174		x	x		6	No	Yes
Octal D	273	x	x	x		8	No	Yes
Octal D	374	x	x	x	x	8	Yes	No
Octal D	574	x			x	8	Yes	No
10-Bit D	821	x				10	Yes	No
16-Bit D	16374	x			x	16	Yes	No
20-Bit D	16821	x				20	Yes	No

Latches

Function/Description	Type	LCX	LVX	LVQ	LVT	Data Inputs	Enable Inputs (Level)	TRI-STATE Outputs	Flow Through Pin Out
Octal Transparent Latch	373	x	x	x	x	8	1 (H)	Yes	No
Octal Transparent Latch	573	x	x	x	x	8	1 (L)	Yes	Yes
10-Bit Transparent Latch	841	x				10	1 (H)	Yes	Yes
16-Bit Transparent Latch	16373	x			x	16	2 (H)	Yes	No
20-Bit Transparent Latch	16841	x				20	2 (H)	Yes	Yes
20-Bit Transparent Latch w/30Ω Resistor	162841	x				20	2 (H)	Yes	Yes

Buffers/Line Drivers

Function/Description	Type	LCX	LVX	LVQ	LVT	Enable Inputs (Level)	Inverting Non-Inverting
Quad Buffer	125	x, Tiny	x	x		4 (L)	N
Quad Buffer	126	Tiny	x	x		4 (H)	N
Octal Buffer/Line Driver	240	x	x	x	x	2 (L)	I
Octal Buffer/Line Driver	241	x		x		1 (L) + 1 (H)	N
Octal Buffer/Line Driver	244	x	x	x	x	2 (L)	N
Octal Buffer/Line Driver w/30Ω Res	2244	x				2 (L)	N
Octal Inverting Buffer/Line Driver	540	x				2 (L)	I
Octal Buffer/Line Driver	541	x				2 (L)	N
16-Bit Buffer/Line Driver	16240	x			x	4 (L)	I
16-Bit Buffer/Line Driver w/30Ω Res	162240				x	4 (L)	I
16-Bit Buffer/Line Driver	16244	x			x	4 (L)	N
16-Bit Buffer/Line Driver w/30Ω Res	162244				x	2 (L)	N

Decoders/Demultiplexers

Function/Description	Type	LCX	LVX	LVQ	LVT	Enable	Active Address Inputs	Outputs
1-of-8 Decoder/Demultiplexer	138	x	x	x		2 (L) + 1 (H)	3	8

Multiplexers

Function/Description	Type	LCX	LVX	LVQ	LVT	Enable Inputs (Level)	TRUE Output	Complement Output
8-Input Multiplexer	151			x		1 (L)	Yes (1)	Yes (1)
Quad 2-Input Multiplexer	157	x	x	x		1 (L)	Yes (4)	No
Quad 2-Input Multiplexer	257	x				1 (L)	Yes (4)	No

Transceivers/Registers

Function/Description	Type	LCX	LVX	LVQ	LVT	Registers	Enable Input Level	TRI-STATE Outputs
Octal Bidirectional Transceiver	245	x	x	x	x	No	1 (L)	Yes
Octal Bidirectional Transceiver w/30Ω	2245	x				No	1 (L)	Yes
Octal Registered Transceiver	543	x			x	Yes	2 (L)	Yes
Octal Bus Transceiver and Register	646	x			x	Yes	1 (L)	Yes
Octal Bus Transceiver and Register	652	x			x	Yes	1 (L) + 1 (H)	Yes
Octal Registered Transceiver	2952	x			x	Yes	2 (L)	Yes
16-Bit Bidirectional Transceiver	16245	x			x	No	2 (L)	Yes
16-Bit Bidirectional Transceiver w/30Ω Res	162245				x	No	1 (L)	Yes
18-Bit Universal Transceiver	16500	x			x	Yes	1 (L) + 1 (H)	Yes
18-Bit Universal Transceiver	16501	x				Yes	1 (L) + 1 (H)	Yes
16-Bit Registered Transceiver	16543	x			x	Yes	4 (L)	Yes
16-Bit Bus Transceiver and Register	16646	x			x	Yes	2 (L)	Yes
16-Bit Bus Transceiver and Register	16652	x			x	Yes	2 (L) + 2 (H)	Yes

Special Purpose Translators

Function/Description	Type	LCX	LVX	LVQ	LVT	TRI-STATE Outputs	3V or 5V Conf. I/O	V_{CCA}	V_{CCB}
Octal Translating Transceivers	4245		x			Yes	No	4.5V–5.5V	2.7V–3.6V
Octal Translating Transceivers	3245		x			Yes	No	2.7V–3.6V	4.5V–5.5V
Octal Translating Transceivers	C4245		x			Yes	Yes	4.5V–5.5V	2.7V–5.5V
Octal Translating Transceivers	C3245		x			Yes	Yes	2.7V–3.6V	3.0V–5.5V
16-Bit Translating Transceivers	C164245		x			Yes	Yes	2.7V–3.6V	4.5V–5.5V

Bus Switches

Function/Description	Type	LCX	LVX	LVQ	LVT	TRI-STATE Outputs	3V or 5V Conf. I/O
10-Bit Bus Switch or 5-Bit Bus Exchanger	3L383		x			Yes	Yes
10-Bit Translating Transceiver	3L384		x, Tiny			Yes	Yes
10-Bit Translating Transceiver	3L384A		x			Yes	Yes
24-Bit Bus Exchanger	16212		x			No	Yes

GTL-TTL Transceivers

Function/Description	Type	Active Edge Rate	5V Ctrl Tolerant	Pwr Up/Dn Hi Z	Prog Edge Rate Ctrl	V_{REF} Options	V_{CC}
18-Bit Universal Transceiver	16612	Y	Y	Y	Option	0.8V or 1.0V	3.3V, 5V or Both
17-Bit Universal Transceiver w/Clock Buffer	16616	Y	Y	Y	Option	0.8V or 1.0V	3.3V, 5V or Both

x = available/planned, Tiny = TinyPak™ single function available/planned

National Semiconductor

Low Voltage Logic Cross Reference to National's CROSSVOLT™ Low Voltage Logic Series

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
TI	SN74LVTxxxx	D	JEDEC SOIC	**74LVTxxxx**	*74LCXxxxx*	M	Direct replacement.
TI	SN74LVTxxxx	DB	5.3 mm SSOPII	**74LVTxxxx**	*74LCXxxxx*	MSA	Direct replacement.
TI	SN74LVTxxxx	DW	Wide JEDEC SOIC	**74LVTxxxx**	*74LCXxxxx*	WM	Direct replacement.
TI	SN74LVTxxxx	PW	4.4 mm TSSOP I	**74LVTxxxx**	*74LCXxxxx*	MTC	Direct replacement.
TI	SN74LVTxxxx	DL	48/56 7.5 mm SSOP III	**74LVTxxxx**	*74LCXxxxx*	MEA	Direct replacement.
TI	SN74LVTxxxx	DGG	48/56 6.1 mm TSSOP II	**74LVTxxxx**	*74LCXxxxx*	MTD	Direct replacement.
TI	SN74LVTZxxxx	D	JEDEC SOIC	**74LVTxxxx**	*74LCXxxxx*	M	Direct replacement.
TI	SN74LVTZxxxx	DB	5.3 mm SSOPII	**74LVTxxxx**	*74LCXxxxx*	MSA	Direct replacement.
TI	SN74LVTZxxxx	DW	Wide JEDEC SOIC	**74LVTxxxx**	*74LCXxxxx*	WM	Direct replacement.
TI	SN74LVTZxxxx	PW	4.4 mm TSSOP I	**74LVTxxxx**	*74LCXxxxx*	MTC	Direct replacement.
TI	SN74LVTZxxxx	DL	48/56 7.5 mm SSOP III	**74LVTxxxx**	*74LCXxxxx*	MEA	Direct replacement.
TI	SN74LVTZxxxx	DGG	48/56 6.1 mm TSSOP II	**74LVTxxxx**	*74LCXxxxx*	MTD	Direct replacement.
TI	SN74LVCxxxx	D	JEDEC SOIC	74LCXxxxx		M	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVCxxxx	DB	5.3 mm SSOPII	**74LCXxxxx**		MSA	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVCxxxx	DW	Wide JEDEC SOIC	**74LCXxxxx**		WM	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVCxxxx	PW	4.4 mm TSSOP I	**74LCXxxxx**		MTC	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVCxxxx	DL	48/56 7.5 mm SSOP III	**74LCXxxxx**		MEA	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVCxxxx	DGG	48/56 6.1 mm TSSOP II	**74LCXxxxx**		MTD	Direct replacement. LCX also offers power down high impedance.
TI	SN74LVC4245	DB	5.3 mm SSOPII	*74LVX4245*			Use TSSOP package. (Not footprint compatible)
TI	SN74LVC4245	DW	Wide JEDEC SOIC	*74LVX4245*		WM	Similar replacement.
TI	SN74LVC4245	PW	4.4 mm TSSOP I	*74LVX4245*		MTC	Similar replacement.
TI	SN74ALVC16xxx	DL	48/56 7.5 mm SSOP III	*74LCX16xxx*		MEA	ALVC is slightly faster, but does not have 5V tolerance.

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
TI	SN74ALVC16xxx	DGG	48/56 6.1 mm TSSOP II	*74LCX16xxx*		MTD	ALVC is slightly faster, but does not have 5V tolerance.
TI	SN74LVxxxx	D	JEDEC SOIC	*74LVXxxx*	*74LVQxxx*	M	LVX has 4 mA output drive instead of 6 mA for LV, but LVX is faster and has 5V tolerant inputs.
TI	SN74LVxxxx	DB	5.3 mm SSOPII	*74LVXxxx*	*74LVQxxx*		Use TSSOP package. (Not footprint compatible)
TI	SN74LVxxxx	DW	Wide JEDEC SOIC	*74LVXxxx*	*74LVQxxx*	WM	LVX has 4 mA output drive instead of 6 mA for LV, but LVX is faster and has 5V tolerant inputs.
TI	SN74LVxxxx	PW	4.4 mm TSSOP I	*74LVXxxx*	*74LVQxxx*	MTC	LVX has 4 mA output drive instead of 6 mA for LV, but LVX is faster and has 5V tolerant inputs.
TI	SN74CBT3383	DB	5.3 mm SSOPII	**74LVX3L383**			Use TSSOP package. (Not footprint compatible)
TI	SN74CBT3383	DW	Wide JEDEC SOIC	**74LVX3L383**		WM	Direct replacement.
TI	SN74CBT3383	PW	4.4 mm TSSOP I	**74LVX3L383**		MTC	Direct replacement.
TI	SN74CBT3384A	DB	5.3 mm SSOPII	**74LVX3L384**			Use TSSOP package. (Not footprint compatible)
TI	SN74CBT3384A	DW	Wide JEDEC SOIC	**74LVX3L384**		WM	Direct replacement.
TI	SN74CBT3384A	PW	4.4 mm TSSOP I	**74LVX3L384**		MTC	Direct replacement.
TI	SN74CBT16212	DL	48/56 7.5 mm SSOP III	**74LVX16212**		MEA	Direct replacement.
TI	SN74CBT16212	DGG	48/56 6.1 mm TSSOP II	**74LVX16212**		MTD	Direct replacement.
TI	SN74GTL16xxx	DL	48/56 7.5 mm SSOP III	**Call Marketing**		MEA	In development.
TI	SN74GTL16xxx	DGG	48/56 6.1 mm TSSOP II	**Call Marketing**		MTD	In development.
Philips	74LVTxxxx/A/B	D	JEDEC SOIC/Wide JEDEC SOIC	**74LVTxxxx**	*74LCXxxxx*	M/WM	Direct replacement.
Philips	74LVTxxxx/A/B	DB	5.3 mm SSOPII	**74LVTxxxx**	*74LCXxxxx*	MSA	Direct replacement.
Philips	74LVTxxxx/A/B	PW	4.4 mm TSSOP I	**74LVTxxxx**	*74LCXxxxx*	MTC	Direct replacement.
Philips	74LVTxxxx/A/B	DL	48/56 7.5 mm SSOP III	**74LVTxxxx**	*74LCXxxxx*	MEA	Direct replacement.
Philips	74LVTxxxx/A/B	DGG	48/56 6.1 mm TSSOP II	**74LVTxxxx**	*74LCXxxxx*	MTD	Direct replacement.

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
Philips	74LVCxxxx	D	JEDEC SOIC	**74LCXxxxx**		M/WM	Direct replacement. LCX also offers 5V inputs and outputs.
Philips	74LVCxxxx	DB	5.3 mm SSOPII	**74LCXxxxx**		MSA	Direct replacement. LCX also offers 5V inputs and outputs.
Philips	74LVCxxxx	PW	4.4 mm TSSOP I	**74LCXxxxx**		MTC	Direct replacement. LCX also offers 5V inputs and outputs.
Philips	74LVCxxxx	DL	48/56 7.5 mm SSOP III	**74LCXxxxx**		MEA	Direct replacement. LCX also offers 5V inputs and outputs.
Philips	74LVCxxxx	DGG	48/56 6.1 mm TSSOP II	**74LCXxxxx**		MTD	Direct replacement. LCX also offers 5V inputs and outputs.
Philips	74LVC4245	D	JEDEC SOIC	*74LVX4245*		WM	Similar replacement.
Philips	74LVC4245	DB	5.3 mm SSOPII	*74LVX4245*			Use TSSOP package. (Not footprint compatible)
Philips	74LVC4245	PW	4.4 mm TSSOP I	*74LVX4245*		MTD	Similar replacement.
Philips	74ALVC16xxx	DL	48/56 7.5 mm SSOP III	*74LCX16xxx*		MEA	ALVC is slightly faster, but LCX16xxx offers 5V tolerant inputs and outputs.
Philips	74ALVC16xxx	DGG	48/56 6.1 mm TSSOP II	*74LCX16xxx*		MTD	ALVC is slightly faster, but LCX16xxx offers 5V tolerant inputs and outputs.
Philips	74LVxxxx	N	PDIP				Use SOIC. (Not footprint compatible)
Philips	74LVxxxx	D	JEDEC SOIC/Wide JEDEC SOIC	*74LVXxxx*	*74LVQxxx*	M/WM	LVX has 4 mA output drive instead of 6 mA for LV, but LVX is faster and has 5V tolerant inputs.
Philips	74LVxxxx	DB	5.3 mm SSOPII	*74LVXxxx*	*74LVQxxx*		Use TSSOP package. (Not footprint compatible)
Philips	74LVxxxx	PW	4.4 mm TSSOP I	*74LVXxxx*	*74LVQxxx*	MTC	LVX has 4 mA output drive instead of 6 mA for LV, but LVX is faster and has 5V tolerant inputs.
IDT	IDT74FCT3xxx	P	PDIP				Use SOIC. (Not footprint compatible)
IDT	IDT74FCT3xxx	SO	JEDEC SOIC	**74LCXxxxx**		M/WM	Direct replacement. LCX also offers 5V tolerance.
IDT	IDT74FCT3xxx	PY	5.3 mm SSOPII	**74LCXxxxx**		MSA	Direct replacement. LCX also offers 5V tolerance.
IDT	IDT74FCT3xxxA	P	PDIP				Use SOIC. (Not footprint compatible)
IDT	IDT74FCT3xxxA	SO	JEDEC SOIC	**74LCXxxxx**		M/WM	FCT/A slightly faster, but LCX also offers 5V tolerance.
IDT	IDT74FCT3xxxA	PY	5.3 mm SSOPII	**74LCXxxxx**		MSA	FCT/A slightly faster, but LCX also offers 5V tolerance.

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
IDT	IDT74FCT163xxx	PV	48/56 7.5 mm SSOP III	**74LCX16xxx**		MEA	Direct Replacement.
IDT	IDT74FCT163xxxA	PV	48/56 7.5 mm SSOP III	**74LCX16xxx**		MEA	Direct Replacement.
Pericom (Pioneer)	PI74FCT163xxxT	V	48/56 7.5 mm SSOP III	**74LCX16xxx**		MEA	Direct Replacement.
Pericom (Pioneer)	PI74FCT163xxxT	A	48/56 6.1 mm TSSOP II	**74LCX16xxx**		MTD	Direct Replacement.
Pericom (Pioneer)	PI74FCT163xxxAT	V	48/56 7.5 mm SSOP III	**74LCX16xxx**		MEA	Direct Replacement.
Pericom (Pioneer)	PI74FCT163xxxAT	A	48/56 6.1 mm TSSOP II	**74LCX16xxx**		MTD	Direct Replacement.
Pericom (Pioneer)	PI5C3383	P	PDIP				Use SOIC. (Not footprint compatible)
Pericom (Pioneer)	PI5C3383	S	Wide JEDEC SOIC	**74LVX3L383**		WM	Direct Replacement.
Pericom (Pioneer)	PI5C3383	Q	QSOP	**74LVX3L383**		QSC	Direct Replacement.
Pericom (Pioneer)	PI5C3384A	P	PDIP				Use SOIC. (Not footprint compatible)
Pericom (Pioneer)	PI5C3384A	S	Wide JEDEC SOIC	**74LVX3L384**		WM	Direct Replacement.
Pericom (Pioneer)	PI5C3384A	Q	QSOP	**74LVX3L384**		QSC	Direct Replacement.
Pericom (Pioneer)	PI74LPTxxx	W	JEDEC SOIC	**74LCXxxxx**		M	Direct Replacement.
Pericom (Pioneer)	PI74LPTxxx	S	Wide JEDEC SOIC	**74LCXxxxx**		WM	Direct Replacement.
Pericom (Pioneer)	PI74LPTxxx	Q	QSOP				Use TSSOP. (Not footprint compatible)
Pericom (Pioneer)	PI74LPTxxx	R	Thin QSOP				Use TSSOP. (Not footprint compatible)
Pericom (Pioneer)	PI74LPTxxx	L	4.4 mm TSSOP I	**74LCXxxxx**		MTC	Direct Replacement.
Pericom (Pioneer)	PI74LPTxxxA/C	W	JEDEC SOIC	*74LCXxxxx*		M	LPTA/C spec'd slightly faster.
Pericom (Pioneer)	PI74LPTxxxA/C	S	Wide JEDEC SOIC	*74LCXxxxx*		WM	LPTA/C spec'd slightly faster.
Pericom (Pioneer)	PI74LPTxxxA/C	Q	QSOP				Use TSSOP. (Not footprint compatible)
Pericom (Pioneer)	PI74LPTxxxA/C	R	Thin QSOP				Use TSSOP. (Not footprint compatible)
Pericom (Pioneer)	PI74LPTxxxA/C	L	4.4 mm TSSOP I	*74LCXxxxx*		MTC	LPTA/C spec'd slightly faster.
Pericom (Pioneer)	PI74LPT16xxx/A/C	V	48/56 7.5 mm SSOP III	**74LCX16xxx**		MEA	Direct Replacement.
Pericom (Pioneer)	PI74LPT16xxx/A/C	A	48/56 6.1 mm TSSOP II	**74LCX16xxx**		MTD	Direct Replacement.

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
Quality Semi	QS74FCT3xxx	SO	JEDEC SOIC	**74LCXxxxx**		M/WM	Direct Replacement.
Quality Semi	QS74FCT3xxx	Q	QSOP				Use TSSOP package. (Not footprint compatible)
Quality Semi	QS74FCT3xxxA	SO	JEDEC SOIC	*74LCXxxxx*		M/WM	FCT/A slightly faster, but LCX offers 5V tolerant inputs and outputs.
Quality Semi	QS74FCT3xxxA	Q	QSOP				Use TSSOP package. (Not footprint compatible)
Quality Semi	QS74FCT163xxxA	Q2	QVSOP	*74LCX16xxx*			Use TSSOP package. (Not footprint compatible)
Quality Semi	QS3383/QS3L383	P	PDIP				Use SOIC. (Not footprint compatible)
Quality Semi	QS3383/QS3L383	SO	Wide JEDEC SOIC	**74LVX3L383**		WM	Direct Replacement. "L" means low power version.
Quality Semi	QS3383/QS3L383	Q	QSOP	**74LVX3L383**		QSC	Direct Replacement. "L" means low power version.
Quality Semi	QS3384/QS3L384	P	PDIP				Use SOIC. (Not footprint compatible)
Quality Semi	QS3384/QS3L384	SO	Wide JEDEC SOIC	**74LVX3L384**		WM	Direct Replacement. "L" means low power version.
Quality Semi	QS3384/QS3L384	Q	QSOP	**74LVX3L384**		QSC	Direct Replacement. "L" means low power version.
Cypress (& Performance)	CYBUS3384	P	PDIP				Use SOIC. (Not footprint compatible)
Cypress (& Performance)	CYBUS3384	SO	Wide JEDEC SOIC	**74LVX3L384**		WM	Direct Replacement.
Cypress (& Performance)	CYBUS3384	Q	QSOP	**74LVX3L384**		QSC	Direct Replacement.
Motorola	MC74LVTxxx	DW	Wide JEDEC SOIC	**74LVTxxxx**		WM	Direct Replacement.
Motorola	MC74LVTxxx	DT	4.4 mm TSSOP I	**74LVTxxxx**		MTC	Direct Replacement.
Motorola	MC74LCXxxx	DW	Wide JEDEC SOIC	**74LCXxxxx**		WM	Direct Replacement.
Motorola	MC74LCXxxx	M	EIAJ SOIC	**74LCXxxxx**		SJ	Direct Replacement.
Motorola	MC74LCXxxx	DT	4.4 mm TSSOP I	**74LCXxxxx**		MTC	Direct Replacement.
Motorola	MC74LVQxxx	DW	Wide JEDEC SOIC	**74LVQxxxx**		SC	Direct Replacement.
Motorola	MC74LVQxxx	M	EIAJ SOIC	**74LVQxxxx**		SJ	Direct Replacement.
Motorola	MC74LVQxxx	DT	4.4 mm TSSOP I	*74LVQxxxx*			Use QSOP package. (Not footprint compatible)

Competitor	Family	Pkg Code	Package	National Replacement	Alternate	Pkg Code	Comments
Toshiba	TC74LCXxxx	FN	JEDEC SOIC	**74LCXxxxx**		M	Direct Replacement.
Toshiba	TC74LCXxxx	FW	Wide JEDEC SOIC	**74LCXxxxx**		WM	Direct Replacement.
Toshiba	TC74LCXxxx	F	EIAJ SOIC	**74LCXxxxx**		SJ	Direct Replacement.
Toshiba	TC74LCXxxx	FS	4.4 mm SSOP I	**74LCXxxxx**		MTC	Direct Replacement. Our TSSOP is footprint compatible with their SSOP.
Toshiba	TC74LVXxxx	FN	JEDEC SOIC	**74LVXxxxx**		M	Direct Replacement.
Toshiba	TC74LVXxxx	FW	Wide JEDEC SOIC	**74LVXxxxx**		WM	Direct Replacement.
Toshiba	TC74LVXxxx	F	EIAJ SOIC	**74LVXxxxx**		SJ	Direct Replacement.
Toshiba	TC74LVXxxx	FS	4.4 mm SSOP I	**74LVXxxxx**		MTC	Direct Replacement. Our TSSOP is footprint compatible with their SSOP.
Toshiba	TC74LVQxxx	FN	JEDEC SOIC	**74LVQxxxx**		SC	Direct Replacement.
Toshiba	TC74LVQxxx	FW	Wide JEDEC SOIC	**74LVQxxxx**		SC	Direct Replacement.
Toshiba	TC74LVQxxx	F	EIAJ SOIC	**74LVQxxxx**		SJ	Direct Replacement.

Important Note:

National Semiconductor does not guarantee device compatibility and does not assume liability for device incompatibility either stated or implied by this document. Device compatibility must be verified by the user.

Key:

BOLD: Direct replacement.

Italics: Similar replacement.

(blank): No replacement or no footprint compatible replacement.

Section 1

Description and Family Characteristics

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National Semiconductor

Description and Family Characteristics

Introduction

In order to provide optimum logic solutions for a variety of low voltage applications, National Semiconductor offers several low voltage logic product families. Each of these families possess a unique set of features and operating characteristics optimized for a particular low voltage application. All National low voltage logic devices share the following features:

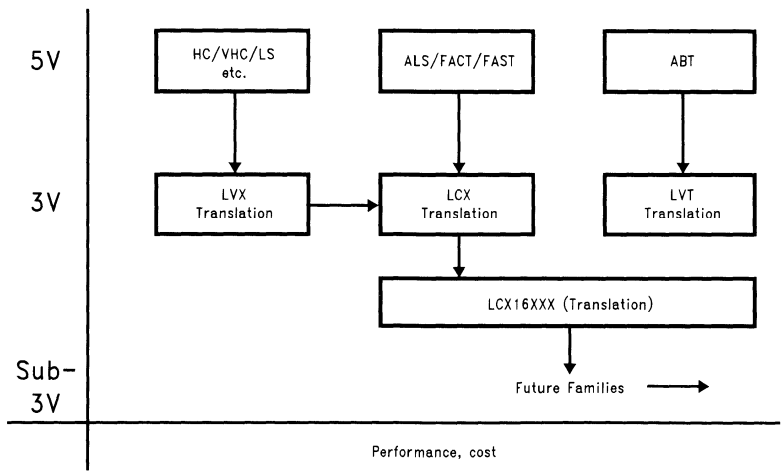
- low or "zero" static power dissipation (<100 nA typical for LVQ)
- reduced dynamic power consumption
- lower switching noise than comparable higher supply voltage counterparts
- compliance with EIA-JEDEC low voltage interface standard #8-1B

Output drive, translation capabilities, switching speed and interface flexibility are examples of the characteristics that differentiate these low voltage logic families.

Family Specifications

To assist the designer in selecting one of National Semiconductor's Low Voltage Logic families the specifications for a '245 function are compared below for easy reference. Please reference individual data sheets for specific device information.

CROSSVOLT Portfolio At-A-Glance



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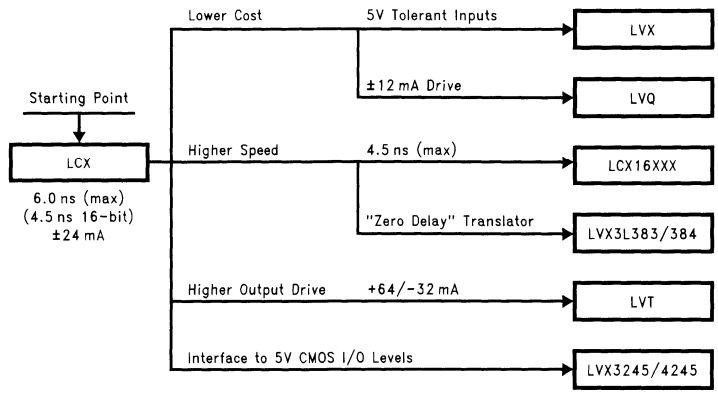
Selecting a CROSSVOLT Family



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Recommended Operating Conditions

	LVQ	LVX			LCX	LVT*	ALCX* (Advance Information)	GTL* (Preliminary)
		LVX	Dual Supply Translating Transceivers	Bus Switches				
	'245	'245	4245	'3L383	'245	'245	'245	'16612
Supply Voltage (V_{CC})	2.0V to 3.6V	2.0V to 3.6V	2.7V to 3.6V and 4.5V to 5.5V	4.0V to 5.5V	2.0V to 3.6V	2.7V to 3.6V	2.0V to 3.6V	3.15V to 3.45V 4.75V to 5.25V
Input Voltage (V_I)	0V to V_{CC}	0V to 5.5V	0V to 5.5V		0V to 5.5V	0V to 5.5V	0V to 5.5V	0V to 5.5V
Output Voltage (V_O)								
Active	0V to V_{CC}	0V to V_{CC}	0V to V_{CC}		0V to V_{CC}	0V to V_{CC}	0V to V_{CC}	0V to V_{CC} (TTL Side) 0V to V_{TT} (GTL Side)
TRI-STATE®	0V to V_{CC}	0V to V_{CC}	0V to V_{CC}		0V to 5.5V	0V to 5.5V	0V to 5.5V	0V to 5.5V
Operating Temperature (T_A)	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C

*planned or in development

DC Electrical Characteristics

		LVQ	LVX			LCX	LVT*	ALCX* (Advance Information)	GTL* (Preliminary)	
			LVX	Dual Supply Translating Transceivers	Bus Switches				TTL Side	GTL Side
		'245	'245	4245	'3L383	'245	'245	'245		'16612
V_{IH}	Min	2.0V	2.0V	2.0V	2.0V	2.0V	2.0V	2.0	2.0	V_{REF} + 50 mV
V_{IL}	Max	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8	0.8	V_{REF} − 50 mV
V_{OH}	Min	2.48V @ I_{OH} = −12 mA	2.48V @ I_{OH} = −4 mA	3.76V @ I_{OH} = −24 mA		2.2V @ I_{OH} = −24 mA	2.0V @ I_{OH} = −32 mA	2.2V@ I_{OH} = −24 mA	2.0V@ I_{OH} = −32 mA	V_{tt}
V_{OL}	Max	0.44V @ I_{OL} = +12 mA	0.44V @ I_{OL} = 4 mA	0.44V @ I_{OL} = 24 mA		0.55V @ I_{OL} = 24 mA	0.55V @ I_{OL} = 64 mA	0.55V@ I_{OL} = 24 mA	0.55V@ I_{OL} = 64 mA	0.55V@ I_{OL} = 40 mA
I_{IN}	@ V_{IN} = V_{CC} or GND Max	±1.0 μA	±1.0 μA	±1.0 μA	±1 μA	±5.0 μA	±10 μA	±5 μA	±10 μA	
I_{CC}	Max	40 μA	40 μA	80 μA	3 μA	10 μA	12 mA	10 μA	30 mA	
I_{OZ}	Max	±3.0 μA	±2.5 μA	±5 μA	±1 μA	±5 μA	±1 μA	±5 μA	±1 μA	
V_{OLP}	Max	0.8V	0.8V	1.5V/0.8V		0.8	TBD	0.8	0.8V	TBD
V_{OLV}	Min	−0.8V	−0.8V	−1.2V/−0.8V		0.8	TBD	0.8	−0.8V	TBD
V_{IHD}	Max	2V	2V	2V			TBD		TBD	
V_{ILD}	Max	0.8V	0.8V	0.8V			TBD		TBD	
$I_{BHL/H}$								±75 μA	±75 μA	
$I_{BHLO/HHO}$								±450 μA		

AC Electrical Characteristics

		LVQ	LVX			LCX	LVT*	ALCX* (Advance Information)	GTL* (Preliminary) A → B/B → A
			LVX	Dual Supply Translating Transceivers	Bus Switches				
	Units = ns	'245	'245	4245	'3L383	'245	'245	'245	'16612
T_{PHL}	Max	10.5	11.5	8.5	0.25	7	4	3.6	3.9/5.0
T_{PLH}	Max	10.5	11.5	8	0.25	7	4	3.6	4.0/6.0
T_{PZL}	Max	13.5	16.5	9	6.5	8.5	5.5	5.0	4.5
T_{PZH}	Max	13.5	16.5	9.5	6.5	8.5	5.5	5.0	4.5
T_{PHZ}	Max	15	14.5	8.5	5.5	7.5	5.9	5.0	5.0
T_{PLZ}	Max	15	14.5	7	5.5	7.5	4.8	5.0	5.0
T_{OSHL}	Max	1.5	1.5	1.5		1	1	0.5	1.0
T_{OSLH}	Max	1.5	1.5	1.5		1	1	0.5	1.0

Operating Voltage Features of National Semiconductor's Low Voltage Logic Families

One of the most popular uses of low voltage logic is for translation between voltage levels. '244 and '245 functions are most often used for translation, but other functions are also used. The following table summarizes the translation capabilities for each family.

Parameter	Pure 3V	Mixed Voltage Tolerant	Translators			Mixed Voltage Tolerant	Mixed Voltage Tolerant	ALCX* (Advance Information)	GTL* (Preliminary)
			Non-Configurable	Configurable	Conditional (Note 1)				
	LVQ	LVX	LVX3245/4245	LVXC3245/4245	LVX3L383/4	LCX	LVT*		
V_{CC}	2.0V–3.6V	2.0V–3.6V			4.0V–5.5V	2.0V–3.6V	2.7V–3.6V	2.0V–3.6V	
V_{CC}@ A Side			4.5V–4.5V or 2.7V–3.6V	2.7V–3.6V or 4.5V–5.5V					3.0V–3.6V
V_{CC}@ B Side			4.5V–5.5V or 2.7V–3.6V	2.7V–5.5V or 3.0V–5.5V					4.5V–5.5V
Inputs	3V	Accepts 3V and 5V	0V–V_{CC}	0V–V_{CC}	0V–V_{CC}	Accepts 3V and 5V	Accepts 3V and 5V	Accepts 3V and 5V	Accepts 3V and 5V
I/O and Outputs	3V	3V Only	0V–V_{CC}	0V–V_{CC}	Interfaces with 3V/5V	Accepts 3V and 5V (Note 2)	Accepts 3V and 5V (Note 2)	Accepts 3V and 5V	
A-Port			Interfaces with 3V or 5V (Fixed)	Interfaces with 3V or 5V (Fixed)					Accepts 3V and 5V (Note 2)
B-Port			Interfaces with 3V or 5V (Fixed)	Interfaces with 3V or 5V (Configurable)					From GTL Level up to 5V

Note 1: Translation feature implemented by adding a diode between V_{CC} and the device.

Note 2: Only when outputs in TRI-STATE condition (when an I/O is an input it can accept a 5V stimulus).

All the families except LVQ provide some sort of translation capability. LVX and LCX will accept 5V signals on the inputs, and LCX will also tolerate 5V signals on the outputs when the outputs are in TRI-STATE. The LVX3L383/4 devices can be used as "zero delay" translators when a diode is used between V_{CC} and the devices. For pure translation, the LVX Dual Supply Translating Transceivers are unsurpassed. They can even be used to drive 5V CMOS inputs and the LVXC3245/4245 devices have B-port I/O which can be configured for 3V or 5V "on the fly".

Low Voltage Logic Family Feature Comparison

Feature	LVQ	LVX			LCX	LVT*	ALCX* (Advance Information)	GTL* (Preliminary)
		LVX	Dual Supply Translating Transceivers	Bus Switches				
Translation (5V ⟷ 3V)								
Input	no	yes	yes	yes	yes	yes	yes	yes
Bidirectional	no	no	yes	yes	yes	yes	yes	yes
Configurable	no	no	yes	no	no	no	yes	yes
V_{OLP} < 0.8V	yes	yes	yes	yes	yes	yes	yes	yes
Zero Static Power	yes	yes	yes	yes	yes	no	yes	no
Low EMI	yes	yes	yes	yes	yes	yes	yes	yes
Latchup > 300 mA	yes	yes	yes	yes	>500 mA	>500 mA	>500 mA	yes
Alternative Source Available	yes	yes	yes	yes	yes	yes	yes	yes
Power Up Output Hi-Impedance	no	no	no	no	yes	yes	yes	yes
Power Down Output Hi-Impedance	no	no	no	no	yes	yes	yes	yes
Bus Hold						yes	yes	yes
Live Insertion					yes	yes	yes	yes
Corner Supply Pin	yes	yes	yes	yes	yes	yes	yes	yes
Product Range								
Gates/MSI	yes	yes	no	no	yes	yes	no	no
Octals	yes	yes	yes	no	yes	yes	no	TBD
10-Bit	no	no	no	yes	no	no	no	TBD
16-Bit	no	no	yes	no	yes	yes	yes	18/17-Bit
Current/Planned Package Offerings	SOIC, QSOP-Octals Only	SOIC, SSOP I, TSSOP	SOIC, QSOP, TSSOP	SOIC, QSOP, TSSOP	SOIC, TSSOP, SSOP	SOIC, TSSOP, SSOP	SSOP, TSSOP	SSOP TSSOP

Process Technology

A wide range of processing technologies are used to manufacture the various low voltage product families. Process selection is based upon the conversion of product electrical features to technological demands at the device level. Table I summarizes the process characteristics by product line.

TABLE I

Product Line	LVQ	LVX			LCX	LVT*	ALCX* (Advance Information)	GTL* (Preliminary)	Units
		LVX	Dual Supply Translating Transceivers	Bus Switches					
Process	**1.5 CMOS**	**1.0 CMOS**	**0.8 CMOS**	**1.0 BiCMOS**	**0.8 CMOS**	**1.0 BiCMOS**	**0.6 CMOS**	**0.8 CMOS**	
Device Characteristics									
TOX nom	225	150	150	150	150	150		150	A
Abs Max V_{CC} max	7.0	7.0	7.0	7.0	7.0	7.0		7.0	V
LEFF NMOS nom	1.05	0.65	0.6	0.65	0.6	0.65		0.6	μm
LEFF PMOS nom	1.05	1.0	0.75	0.7	0.75	0.7		0.75	μm
β_{NPN} nom	n/a	n/a	n/a	n/a	n/a	90			
Process Characteristics									
Starting Material	P-epi on P++	P-epi on P++	N-epi/N++	N-epi/N++	N-epi/N++	N-epi/N++		N-epi/N++	
Minimum Feature	1.4	1.0	0.8	1.0	0.8	1.0		0.8	μm
M1 Pitch min	4.5	3.5	2.0	3.5	2.0	3.5		2.0	μm
M2 Pitch min	6.0	5.0	2.5	5.0	2.5	5.0		2.5	μm

Switching Speed and Static Output Drive

National Semiconductor offers the low voltage system designer choices when it comes to switching speed, output drive and mixed supply level flexibility. Table II summarizes the performance of the various low voltage logic families with regard to these system critical parameters.

TABLE II

Parameters	LVQ	LVX			LCX	LVT*	Units
		LVX	Dual Supply Translating Transceivers	Bus Switches			
T_{PD} (3.0V, 85°C)	9.5	12.0	9.0	250 ps (Note 1)	6.5	4.0	ns
I_{OL} (Note 2)	12	4	24	n/a	24	64	mA
I_{OH} (Note 3)	−12	−4	−24	n/a	−24	−32	mA
Abs Max V_{CC}	7	7	7	7	7	7	V
Maximum V_{IH} (V_{CC} = 3.0V)	V_{CC} + 0.5	5.5	V_{CC} + 0.5	5.5	5.5	5.5	V
Maximum V_{OH} (V_{CC} = 3.0V)	V_{CC} + 0.5	V_{CC} + 0.5	V_{CC} + 0.5	5.5	5.5 (Note 4)	5.5 (Note 4)	V

Note 1: Calculated based upon 50 pF load and 5Ω nominal channel resistance

Note 2: Refer to individual datasheets for V_{OL} level.

Note 3: Refer to individual datasheets for V_{OH} level.

Note 4: V_{OH} is permitted to rise above V_{CC} only when OEb ≥ V_{IH}.

Switching Induced Noise

Reducing the power supply potential and compressing the output swing of a high drive output buffer reduces the switching induced noise that it propagates or generates. At the same time using advanced technology to provide aggressive propagation delay and large load driving capabilities serves to increase V_{OLP} and V_{OLV}. The net result is that great care must be taken in the design of high speed, low voltage line drivers if the noise benefits of the reduced supply and compressed swing are to be preserved. By incorporating a low-voltage-tuned version of National Semiconductor's proven **G**raduated **T**urn-**O**n (GTO™) circuitry (Note 1), best-in-class propagation delay guarantees are achieved along with the industry's only guaranteed maximum specifications for ground bounce, undershoot and dynamic input thresholds.

Figure 1 depicts a functionally correct, but schematically simplified representation of the National Semiconductor GTO circuit used throughout the low voltage portfolios. In the case of an output high-to-low transition this circuit behaves according to the following flow.

Note 1: United States Patents #4,961,010, #5,036,222 and #5,081,374

INITIAL CONDITIONS

- Vg[P1] and Vg[P2]are discharged to ~ 0V
- Vgs[P1,P2] = V_{CC}
- Vds[P1,P2] = 0V ⟶ Ids[P1] = Ids[P2] = 0 (assumes purely capacitive load)
- Vgs[N1] and Vgs[N2] = 0V ⟶ Ids[N1] = Ids[N2] = 0
- V_O = V_{CC}

NODES A AND B ARE EXTERNALLY CHARGED TO V_{CC} FROM 0V

- Vg[P1,N1] rises to V_{CC}
- The Δt circuits delay the delivery of the signals A and B to P2 and N2
- Vgs[P1] = 0V, Ids[P1] = 0 ⟶ P1 is off
- Vgs[N1] = V_{CC}, Vds[N1] = V_{CC}, N1 saturates and begins to discharge C_L
- The Δt circuits now pass the signals at A and B
- Vgs[P2] = 0V, Ids[P2] = 0 ⟶ P2 is off
- Vgs[N2] = V_{CC}, Vds[N2] = V_{CC}, N2 saturates and discharges C_L
- Ids[N2] ≫ Ids[N1] and Ids[P2] ≫ Ids[P1]

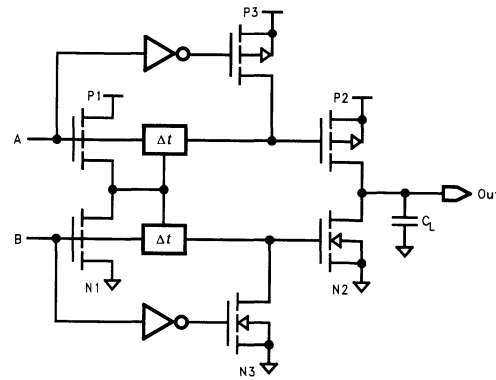

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FIGURE 1. Simplified Schematic of GTO Noise Control

The connectivity within the Δt blocks is such that all signals arriving at nodes A and B are delayed en route to P2 and N2. This would serve to degrade the disable time performance of the buffer. N3 and P3 restore the disable time performance by bypassing the delay elements during LZ or HZ output transitions only. The turn-off signals to N2 and P2 are thereby delivered without delay.

Low Voltage Product Summaries

To assist the system designer in understanding the specific operating characteristics of each of the various products a brief description of the circuit topology for each is presented.

LVQ—Low Voltage Quiet CMOS Logic

The **LVQ** product line is targeted for 3.3V-only applications where interfacing to 5V or other interface levels is not a requirement. *Figure 2* depicts the circuitry common to the LVQ family. Complementary diode input protection is used but **without** the usual current limiting input resistor. This dramatically reduces the forward resistance associated with these junctions and significantly improves their input overshoot and undershoot clamping capabilities. Diode D1 protects the input node from positive voltage ESD events by conducting the charge to the V_{CC} node and away from the ESD sensitive structures internal to the device. D1 becomes forward biased when charge builds up on the input node such that the potential difference across D1 is larger than V_F for D1. This type of input protection circuit precludes the application of input signals containing components that rise above V_{CC} by more than the V_F of D1.

The complementary MOS output drivers used throughout the LVQ family include drain isolation junctions D5 and D6 that are reverse biased during normal operation. This implies that signals applied to any LVQ output node must not rise above $V_{CC} + V_F[D5]$ or below $GND - V_F[D6]$. Operation outside this range will forward bias D5 or D6 and thus creating an undesirable forward conducting path to V_{CC} or ground. This current may result in violation of the Absolute Maximum Ratings for these devices which in turn may adversely and permanently affect device performance and reliability.

LVQ devices include output drivers that feature National Semiconductor's GTO noise control circuitry. The output transistors are designed with suitable dynamic current sourcing and sinking capabilities to assure incident wave switching when driving non-terminated transmission lines having a characteristic impedance of 750Ω or greater.

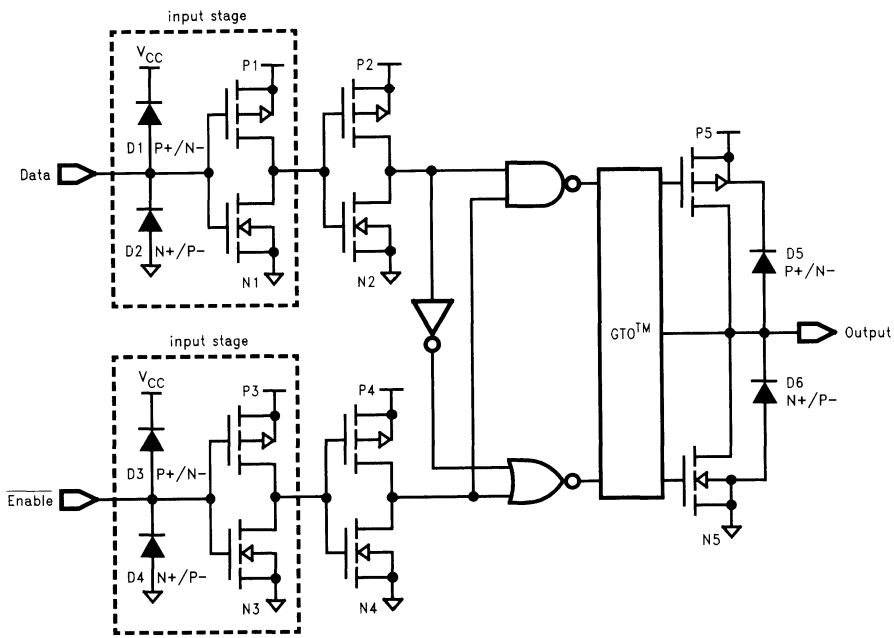

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FIGURE 2. Simplified LVQ Schematic Diagram

LVX—Low Voltage CMOS Logic (with 5V Tolerant Inputs)

The LVX family is made up of three product groupings, each possessing a unique set of interfacing capabilities and characteristics optimized for specific applications.

- Gates, octals and MSI types
- Dual Supply Translating Transceivers
- Bus Switches

The LVX gates, octals and MSI types all feature an alternate input ESD protection scheme that permit their inputs to receive signals whose logic-high levels exceed the supply voltage. *Figure 3* shows a simplified LVX input buffer schematic that includes the alternate ESD structure.

Since there no longer exists a forward junction between the data input pin and V_{CC} the conduction path between the data pin and V_{CC} is disrupted. The positive voltage limitation on the input pins increases from $V_{CC} + V_F$ to the minimum breakdown path tied to the input. For the LVX family of gates, octals and MSI products this value (BVDSS) is in excess of 7V. As in the case of LVQ products, LVX utilizes complementary MOS devices in its output stage and therefore cannot tolerate signals applied to its outputs outside the range defined by GND $- V_F$ and $V_{CC} + V_F$.

The output drive available from LVX is scaled to provide the lowest possible dynamic power dissipation and leakage. By virtue of their pin capacitance specifications, low noise and high speed, LVX products are ideally applied in 3.3V battery powered systems where system performance requires 5V FACT propagation delays.

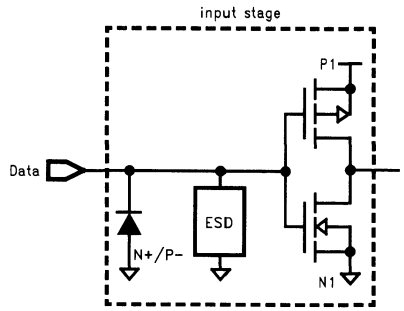

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FIGURE 3. Simplified LVX Input Buffer Schematic as Used in Gates, Octals and MSI Types

LVX—Low Voltage Dual Supply CMOS Translating Transceivers

The LVX family of true translating transceivers use an entirely different approach to the mixed supply interfacing issue. Not just overvoltage tolerant, these devices are true translators—meaning that they receive 3V signals and output 5V signals, and receive 5V signals and output 3V signals. This is accomplished by internally dividing the devices such that the circuitry associated with the A-side is electrically isolated from the B-side. This dual supply architecture permits the LVX translator family to interface 3V signals and 5V signals with **zero static power dissipation**.

In the case of the 74LVX4245 device the A-side is dedicated to 5V operation and V_{CCA} is specified for the range 4.5V–5.5V. The B-side is dedicated 3.3V and V_{CCB} is specified for the range 2.7V–3.6V. The LVXC3245 and LVXC4245 offer further enhanced interfacing in that the B-side is designed to operate over an extended range of I/O and supply levels. For these types V_{CCB} is permitted to be set to any value between 2.7V and 5.5V. The I/O levels on the B-side will track or scale automatically according to the level set on V_{CCB}. This B-side operation is completely independent of V_{CCA}. The A-port and control input buffers are referenced to V_{CCA} and do not vary with V_{CCB}. Refer to *Figure 4.* The configurable dual supply translating transceivers (LVXC) are designed to tolerate floating inputs on the B-port when V_{CCA} and the control signals are set to valid operating levels. The combination of on-the-fly interface flexibility together with "empty socket" tolerance is intended to benefit designers of PC card systems where expansion cards with different supply potentials must be accommodated.

Along with the advanced interfacing capabilities offered by the LVX dual supply translators, these products offer switching speeds equivalent to 5V FCT/FAST but with Quiet Series noise performance and 3.3V supply.

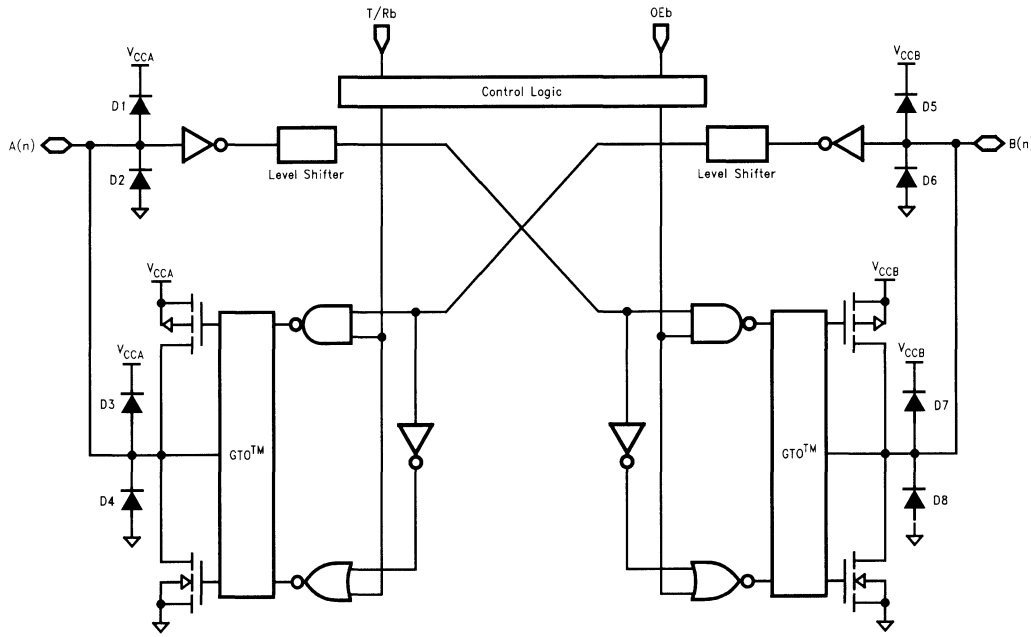

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FIGURE 4. Simplified LVX Translator Schematic Diagram

LVX—Low Voltage CMOS Bus Switches

The LVX3L383 and LVX3L384 low impedance switches complete the LVX family. By virtue of their low "on" resistance these ten channel NMOS pass gates can be used to provide a high speed, bi-directional interface between mixed supply busses. *Figure 5* depicts a single channel representation of the LVX3L384.

The enhancement type NMOS pass gate N1 utilized in all LVX3L383 and LVX3L384 low impedance switches provides bi-directional signal level translation capability. The source (Note 1) of the pass gate will always be clamped to Vg-Vtn irrespective of the drain potential. Vg is set by V_{CC} via inverter I1. Consider the following case:

- V_{CC} is set to 4.1V
- Vtn = 0.8V
- Va = 5.0V
- Venable = 0V
- Vb is initially discharged

Given these conditions pass gate N1 saturates (Vds > Vgs − Vt) and begins charging its source B(N) positively. As B(n) rises the difference between B(n) and V_{CC} (Vgs[N1]) decreases. When B(n) rises to within Vtn of V_{CC}, N1 is cutoff and conduction ceases independent of the potential at A(n). The final terminal conditions then are

V[A(n)] = 5.0V
V[B(n)] = V_{CC} − Vtn = 3.3V

and the translation is completed.

Note 1: For an NMOS transistor the source is defined as the diffusion with lowest potential.

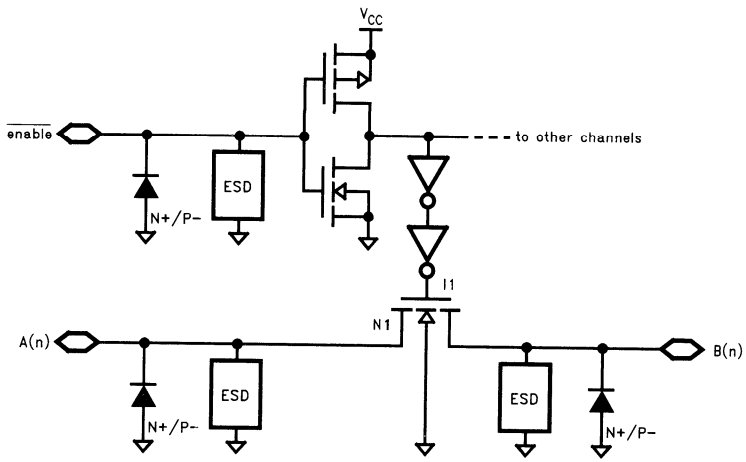

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FIGURE 5. Simplified LVX3L384 Schematic Diagram

LCX—Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs)

The **LCX** product line represents National Semiconductor's most advanced low voltage CMOS product line. These devices offer mixed 3V–5V capability and are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where low power consumption is a necessity. By virtue of a proprietary input/output structure (Note 1), the LCX family of products will tolerate input and output (Note 2) node exposure to signals or DC levels that exceed the V_{CC} level. Refer to *Figure 6* for schematic description of a typical LCX circuit.

Note that the output PMOS device P5 has its bulk potential supplied by the output of the comparator X1 rather than by V_{CC} as in conventional CMOS. The circuitry contained within the comparator is designed such that the output is always the greater of V_{CC} or V_O. This technique circumvents the P+/N− bulk-source forward junction that usually appears between the PMOS drain at the output and the bulk connection of the output PMOS which is usually tied to V_{CC}. Eliminating this junction is fundamental to the powered-down high Z and overvoltage tolerance features that distinguish LCX from other low voltage CMOS products.

Note 1: U.S. and international patent protection applied for.

Note 2: Output overvoltage is permitted unconditionally for tri-stated outputs. For active outputs, see datasheet.

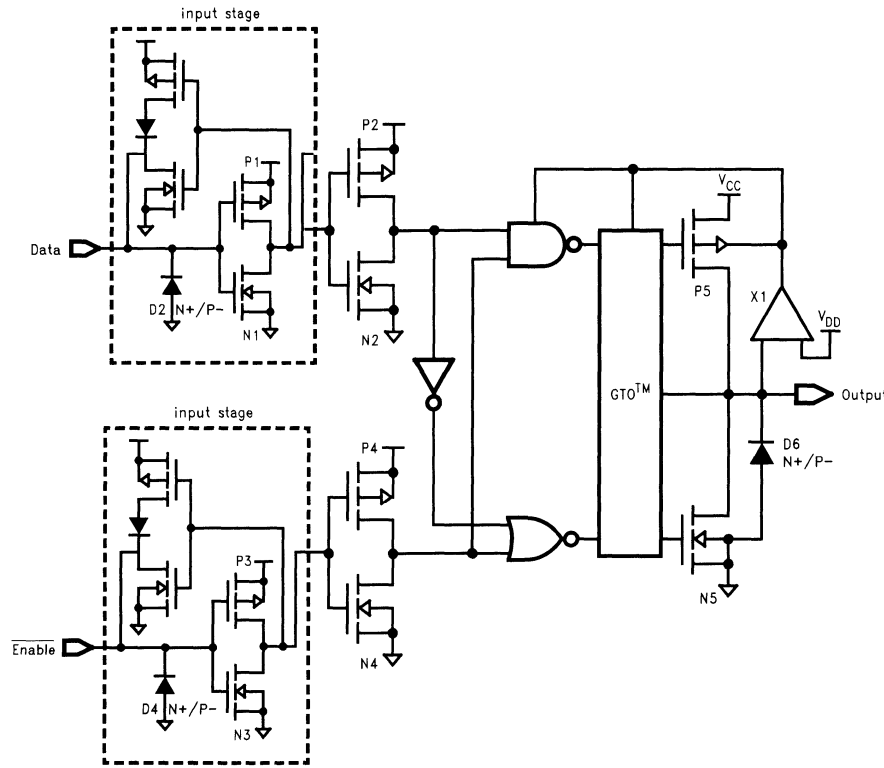

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FIGURE 6. Simplified LCX Schematic Diagram

LVT—Low Voltage High Speed BiCMOS Logic

LVT is National Semiconductor's highest performance low voltage family of products. Manufactured using sub-micron BiCMOS technology, LVT includes all the mixed-supply interface features of LCX in addition to BJT-enhanced propagation delays. These 5V tolerant low voltage devices are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where high speed and high drive are required. By virtue of hysteresis applied by I1 and I2 directly at the input node (refer to *Figure 7*), LVT devices will tolerate floating input conditions that would otherwise lead to increased leakage or compromises in system data integrity.

The output buffer design is based upon the LCX circuit and includes overvoltage tolerance at the output as does LCX. AC and DC performance in the LVT version of the output is augmented by the addition of the parallel NPN devices Q3 and Q4. The Q4 base drive required to sink the rated I_{OL} results in a nominal I_{CCL} of less than 10 mA. The reverse-biased Schottky device D3 prevents output overvoltages that exceed BVCEO from corrupting the low voltage supply. LVT benefits from this protection when V_{CC} is applied as well as when the device is powered-down.

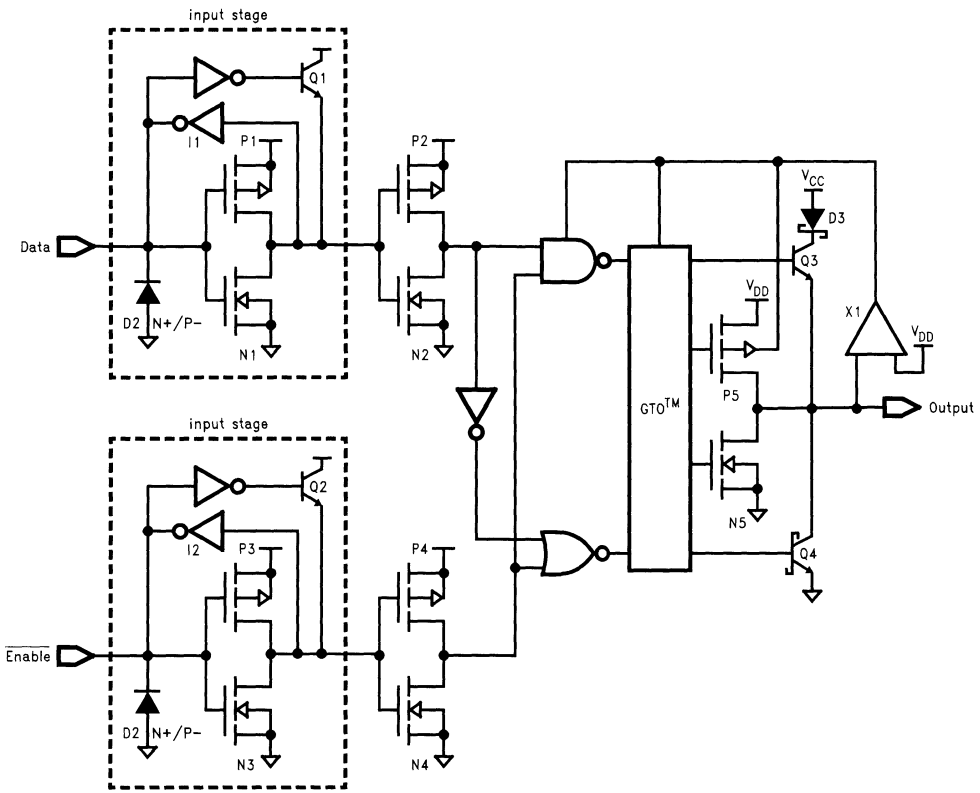

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FIGURE 7. Simplified LVT Schematic Diagram

At National Semiconductor it is our mission to excel in serving chosen markets by delivering semiconductor intensive products and services of the highest quality and value, thereby providing a competitive advantage to our customers worldwide. Should you have any additional questions about our Low Voltage Products, please contact your local sales office or our Customer Response Center at 1-800-272-9959 within the U.S., 1-800-258-6768 in Canada.

ALCX—Advanced Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs)

The **ALCX** product line offers mixed 3V–5V capability and is recommended for applications where 3.3V and 5.0V subsystems interface with one another and where low power consumption is a necessity. By virtue of a proprietary input/output structure (Note 1), the ALCX family of products will tolerate input and output (Note 2) node exposure to signals or DC levels that exceed the V_{CC} level. Refer to *Figure 6* for schematic description of a typical ALCX circuit.

Note that the output PMOS device P5 has its bulk potential supplied by the output of the comparator X1 rather than by V_{CC} as in conventional CMOS. The circuitry contained within the comparator is designed such that the output is always the greater of V_{CC} or V_O. This technique circumvents the P+/N− bulk-source forward junction that usually appears between the PMOS drain at the output and the bulk connection of the output PMOS which is usually tied to V_{CC}. Eliminating this junction is fundamental to the powered-down high Z and overvoltage tolerance features that distinguish ALCX from other low voltage CMOS products.

ALCX inputs, I/O, and control pins also feature bus hold circuitry to eliminate the need for pull-up resistors on unconnected or floating pins. The need for pull-ups is common on many processor buses where non-active devices are placed in TRI-STATE. The speed, drive, and bus hold capabilities of ALCX make it well suited for these applications.

ALCX also features power up/down high impedance. ALCX inputs and outputs power up and power down in the high impedance state, facilitating both live insertion and power management applications.

Note 1: U.S. and international patent protection applied for.

Note 2: Output overvoltage is permitted unconditionally for tri-stated outputs. For active outputs, see datasheet.

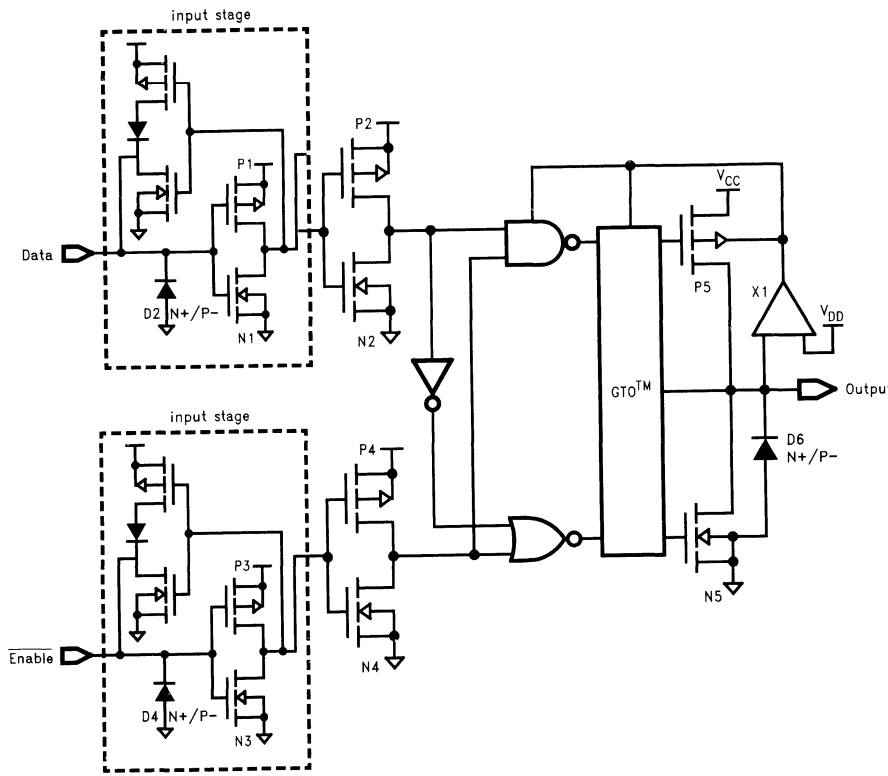

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FIGURE 6. Simplified ALCX Schematic Diagram

Section 2

Ratings, Specifications and Waveforms

Section 2 Contents

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National Semiconductor

Low Voltage Logic Ratings, Specifications, and Waveforms

Definition of Terms

DC Characteristics

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

I_{CC} The current flowing into the V_{CC} supply terminal when the device is at a quiescent state.

I_{CCH} The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL} The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

ΔI_{CC} Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ} The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_I, I_{IN} Input Current. The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.

I_{OH} Output HIGH Current. The current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW Current. The current flowing into an output which is in the LOW state.

I_{OS} Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

I_{OZ} Output OFF current. The current flowing into or out of a disabled TRI-STATE® output when a specified LOW or HIGH voltage is applied to that output.

$I_{I(HOLD)}$ Input hold Current. Input current that holds the input at the previous state when the driving device goes to a high impedance state.

$I_{I(OD)}$ Input over-drive current. Input current that is specified to switch a logic level which is held at previous state.

I_{OFF} Input/Output power-off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input/output from 0V to 5.5V with V_{CC} = 0V.

V_{CC} Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

V_{IK} Input Clamp Diode Voltage. The voltage on an input (−) when a specified current is pulled from that input.

V_{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

V_{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

V_{IL} Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

V_{ILD} Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

V_{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

V_{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_t Maximum Transistor Operating Frequency—The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Toggle Frequency/Operating Frequency—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time—The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time—The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W Pulse Width—The time between specified amplitude points of the leading and trailing edges of a pulse.

t_H Hold Time—The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_S Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between specified levels on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between specified levels on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

t_{rec} Recovery Time—The time between the specified level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

Multiple (Simultaneous) Output Switching Propagation Delays—These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF output load.

Multiple Output Switching Skew—Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

AC Dynamic (Noise) Characteristics

V_{OLP}, V_{OLV}—Ground Bounce (Quiet Output Switching)—Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

V_{ILD}, V_{IHD}—Dynamic Threshold—Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

Input Edge Rate—This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

Power

Power-Up I_{CC} Traces—Shows how the supply current reacts to various input conditions during power up.

I_{CC} vs V_{IN} Traces—Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

I_{CCD} (Dynamic I_{CC})—Determines the amount of current an IC will consume at frequency.

Capacitance

Input/Output Capacitance (C_{IN}/C_{OUT})
Power Dissipation Capacitance (C_{PD})

Reliability Tests

Latch-Up—Testing detemines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

Electrostatic Discharge, Human Body—Per MIL-STD-883C and Machine model.

Characterization Philosophy

During the National new product introduction process for logic IC's, a new low voltage IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, V_{tn}, V_{tp}, L_{eff}, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, V_{CC}, temperature, and condition. This allows product to be shipped on demand without problems or delays.

Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

Power Dissipation—Test Philosophy (Continued)

Gates/Buffers/ Line Drivers:	Switch one input. Bias the remaining inputs such that one output switches.
Latches:	Switch the Enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock pin with other inputs biased such that the device shifts.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generator:	Switch one input.
Priority Encoders:	Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Figure 1 shows the AC test circuit used in characterizing and specifying propagation delays for all of the low voltage logic devices as shown, unless otherwise specified in the data sheet of a specific device.

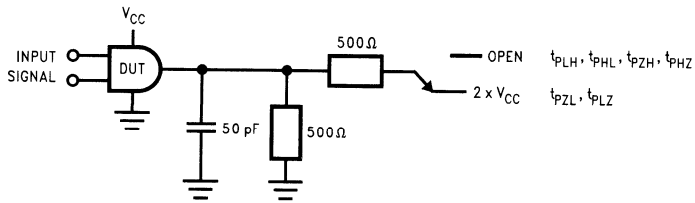

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FIGURE 1a. AC Test Circuit for LVQ, LVX Translator Families

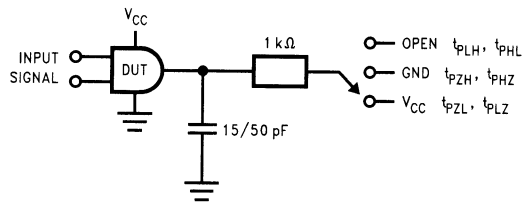

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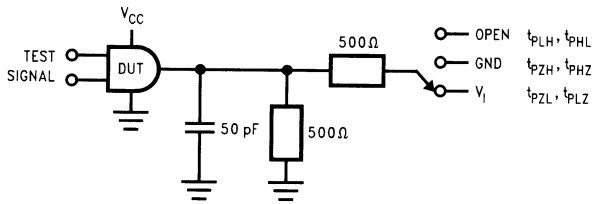
FIGURE 1b. AC Test Circuit for LVX Family



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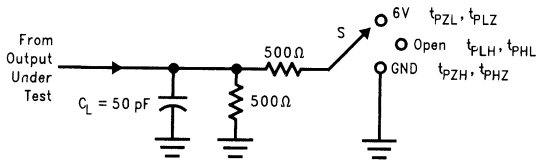
Family	V_I
LCX, ALCX	6V
LVT	6V
LVX Bus Switch	7V

FIGURE 1c. AC Test Circuit for LCX, ALCX, LVT, LVX Bus Switch Families

Test Circuit for A Outputs



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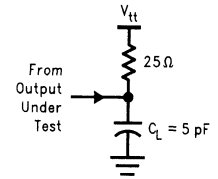
Test Circuit for B Outputs



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Note: C_L includes probe and jig capacitance.

Note: For B port outputs, C_L = 5 pF is used for worst case edge rate.

FIGURE 1d. AC Test Circuit for GTL Family

Test Conditions

Figure 2 describes the input signal voltage levels to be used when testing low voltage logic circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0V to V_{CC}. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 3.3V then dropping it to a level corresponding to V_{IH} characteristics, and then raising it again to the 3.3V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL}, then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

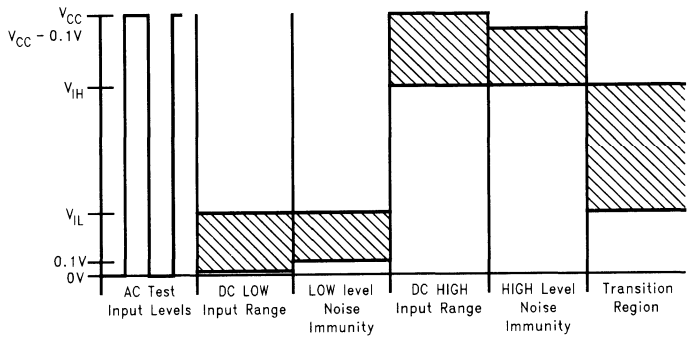

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FIGURE 2. Test Input Signal Levels

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See *Figures 3* and *4*.

Enable and Disable Times

Figures 5 and *6* show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from V_{OL} or V_{OH}, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the 10% and 90% points. This better reflects actual test points and does not change specification limits.

Waveforms

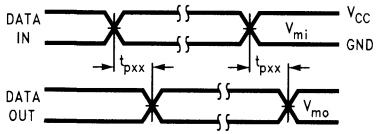

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FIGURE 3. Waveform for Inverting and Non-Inverting Functions

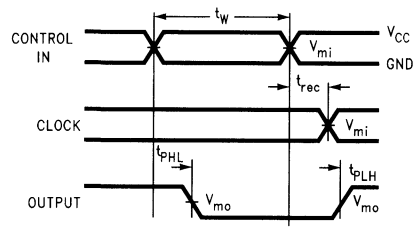

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FIGURE 4. Propagation Delay, Pulse Width and t_{rec} Waveforms

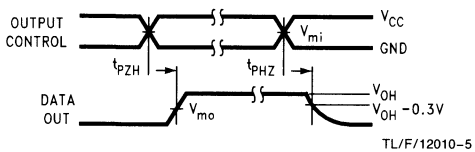

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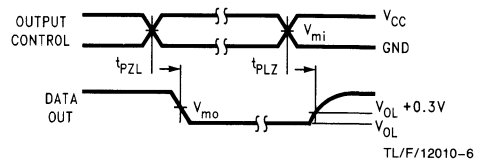
FIGURE 5. TRI-STATE Output High Enable and Disable Times for Low Voltage Logic



TL/F/12010–6

FIGURE 6. TRI-STATE Output Low Enable and Disable Times for Low Voltage Logic

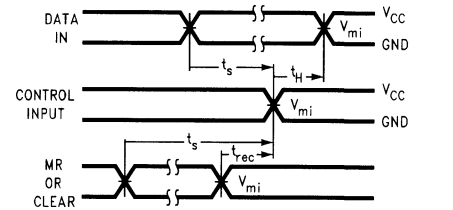


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FIGURE 7. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

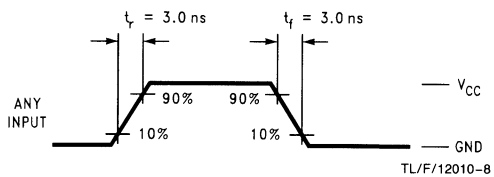

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FIGURE 8. t_{rise} and t_{fall}

	V_{mi}	V_{mo}	
LVQ	50% V_{CC}	50% V_{CC}	
LVX	50% V_{CC}	50% V_{CC}	
LVXX	50% V_{CC}*	50% V_{CC}	
LCX	1.5V	1.5V	
LVT	1.5V	1.5V	
ALCX	1.5V	1.5V	
GTL	1.5V (A)	V_{REF} (B)	A → B
	V_{REF} (B)	1.5V (A)	B → A
	1.5V (Control)	1.5V (A)	ZH/ZL

*1.5V for TTL Compatible

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to low voltage logic devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all parts of the tester, which are near the device, are conductive and connected to ground.

Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture or Equivalent
HP54100 Oscilloscope or Equivalent

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 3.3V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3.3V HIGH. Verify levels with a digital volt meter.

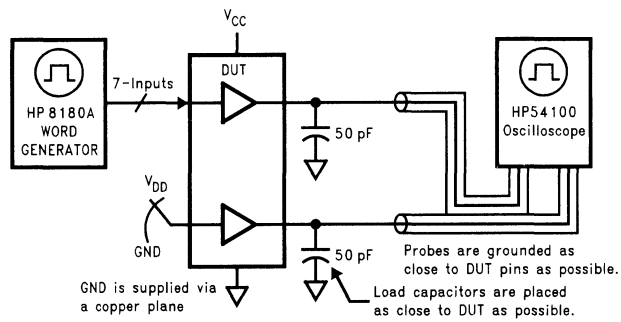

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FIGURE 9. Simultaneous Switching Test Circuit

Noise Characteristics (Continued)

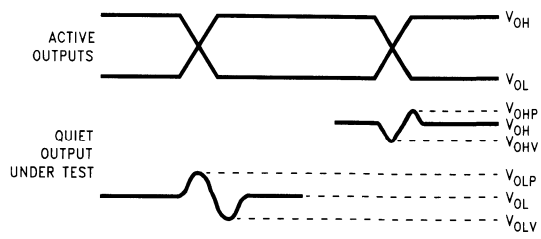


FIGURE 10. Quiet Output Noise Voltage Waveforms

Note 1: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 2: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 10 kΩ scope probe plugged into a standard SMB type connector on the test fixture.
- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 10 kΩ scope probe plugged into a standard SMB type connector on the test fixture.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output low level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Extended Specifications

National has taken new steps in aiding the system designer with a better method to predict device performance in his application. National now offers system oriented performance specifications so a designer can feel confident in the way a device will perform over a wider variety of switching conditions. Performance specifications in the form of Extended Specifications are provided with each product datasheet.

In the past, most extended databook specifications depended on a representative product family function to provide the guaranteed performance data for the rest of the family. The drawback from this method of test and specmanship leaves rather large process, tester and function guardbands in the final maximum or minimum specifications. The test data for National's low voltage logic product family, taken during product development on each function, provides the low voltage logic family with device specific and guaranteed extended specifications that can be passed directly to the system designers. National offers the extended specifications with the belief that customers can reduce their incoming test requirements and in essence reduce the cost and time for product design-in.

Additional specifications provided by National include: Quiet Output Switching (QOS) V_{OLP}, V_{OLV}, and Dynamic Threshold (DVTH), V_{ILD}, and V_{IHD}.

Each of the guaranteed extended specifications involve multiple output switching events. During a multiple output switching event, stray inductance and capacitance inhibit product performance. National has developed standardized hardware that aligns with the industry for low voltage logic product evaluations. Some of the features of the test fixturing include ground planes and low inductive connections, critical in evaluating the product and not the fixture.

The extended specfication tests have very similiar if not identical test setups. The results of the measurements from each test depend on the application focus. The quantitative analysis from the tests provides insight into product performance. The parameters and typical results from each test type can be easily explained in the sections that follow.

TABLE I. Test Conditions for QOS, DVTH

Parameter	Value
Input Edge Rate	2.5 ns
Input Skew	< 300 pS
Input Amplitude	0V to 3.0V
Input Frequency	1 MHz
Output Load	50 pF

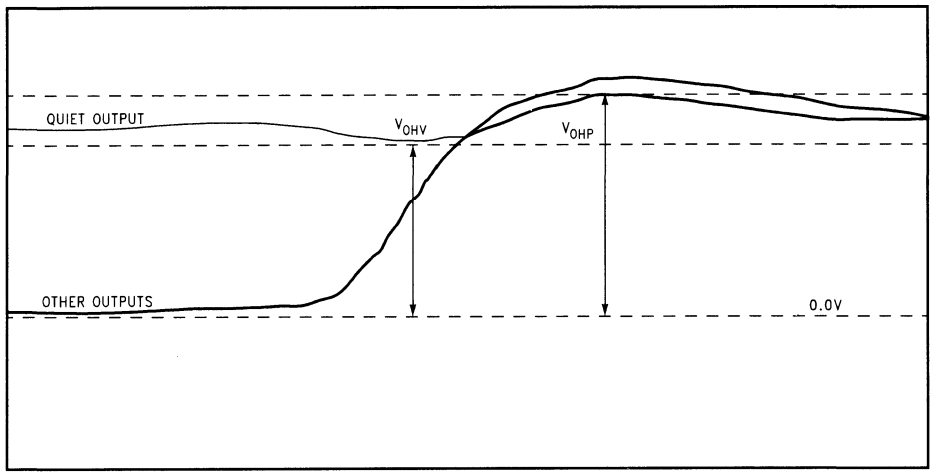
Extended Specifications (Continued)

QUIET OUTPUT SWITCHING

Quiet output switching, (QOS), specifications provide the system designer quantification of low voltage logic effective control of noise and performance to threshold specifications. The QOS specification is a representation of the resultant shift of an output voltage, either from a static high or low level on a single bit, while the other bits switch simutaneously in phase. The voltage shift from a quiet output is specified through four parameters.

- V_{OLP} and V_{OLV} describe the peak or valley of a voltage shift for a quiet output low level.
- V_{OHP} and V_{OHV} describe the peak or valley of a voltage shift for a quiet output high level.

The concern for the system designer evolves from the possiblity that the quiet output voltage shift could impact attached circuitry. V_{OLP} values on some product families peak above threshold high and become recognized as a logic HIGH. The period of time the voltage shift spends in the opposite state is short, in the neighborhood of 10–100 pS, and may not disrupt sequencial circuitry if it is level sensing. If the attached circuitry needs a rising edge, such as a clock input, the sequencial circuitry may take the inadvertent deflection and interpret it. National provides the QOS specification to assist in noise margin planning.



TL/F/12010–11

FIGURE 11. V_{OHP}, V_{OHV} LH Transition V_{CC} = 3.3V, T_A = 25°C

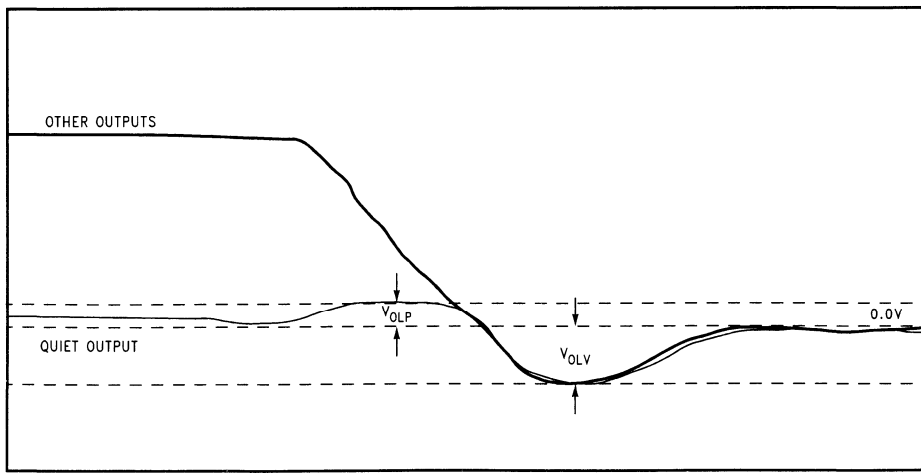


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FIGURE 12. V_{OLP}, V_{OLV} HL Transition V_{CC} = 3.3V, T_A = 25°C

Extended Specifications (Continued)

DYNAMIC THRESHOLD

Dynamic threshold data, (DVTH), like QOS data, provides the system designer with noise performance criteria. DVTH specifications quantify the magnitude of output voltage deflection that a logic high or low might experience under a multiple output switching condition. The voltage deflection is a result of an apparent shift of an input's threshold due to noise generated from MOS switching on the internal die ground and V_{CC} busses. The phenomenon occurs during any logic state transition: LH, HL, ZL, etc. As a practice, National determines the worse case transition for each product and generates the specification based on that transition.

Dynamic threshold specifications are denoted by the nomenclature, V_{ILD} and V_{IHD}, where the "D" represents "Dynamic". The definitions for each are as follows,

- V_{ILD} - The maximum LOW input level such that normal switching/functional characteristics are observed on the output
- V_{IHD} - The minimum HIGH input level such that normal switching/functional characteristics are observed on the output

Dynamic threshold failures are bundled into five main failure modes. The most predominant failure is an output deflection in violation of an input threshold level. Others include propagation delay step out in excess of an MOS propagation delay specification, state changes and oscillations. A detailed definition of each failure can be described as follows,

1. On a low output, the LOW level will not rise above an input threshold low level of 0.8V after the transition of the output. *Figures 13* and *14*. Numbered output curve deflections are a result of 10 mV incremental changes on the low input signal level.

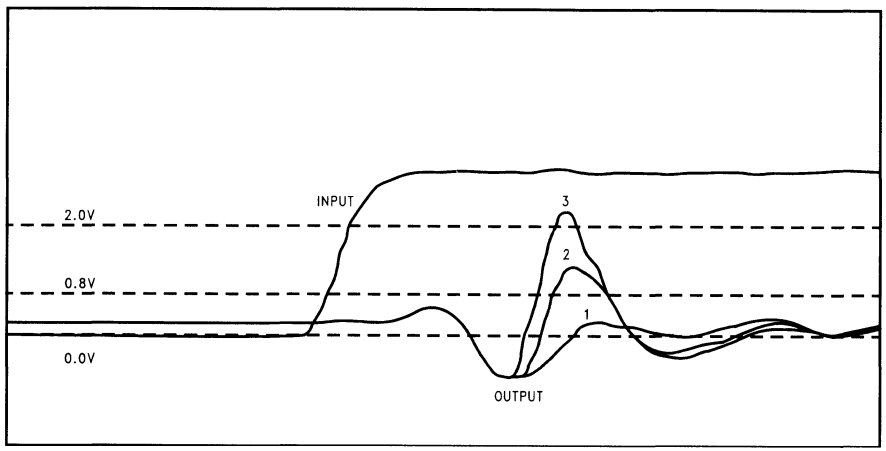

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FIGURE 13. V_{ILD} 7 Outputs Switching
V_{CC} = 3.3V, T_A = 25°C

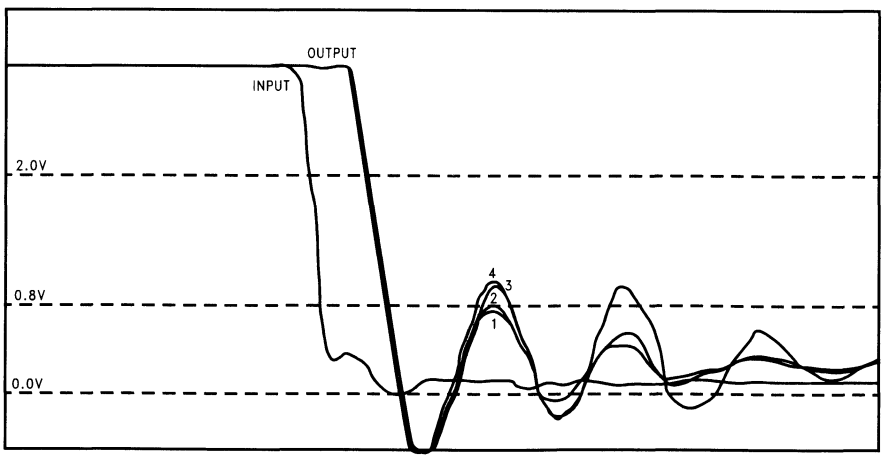

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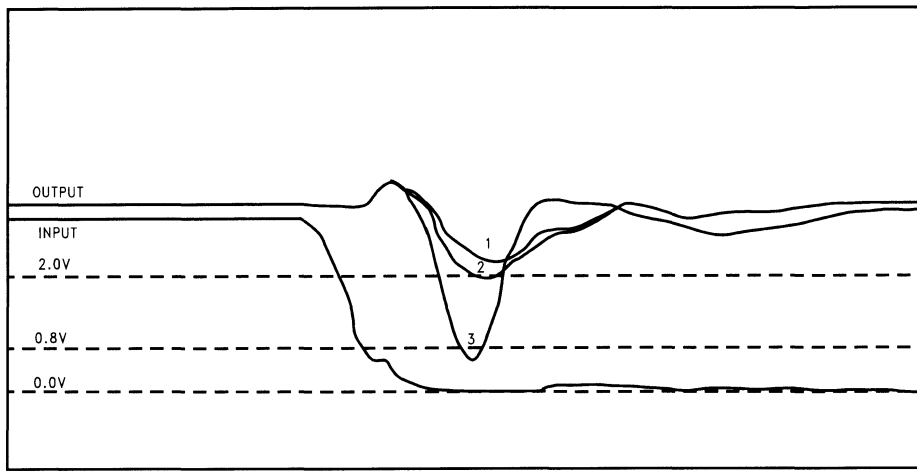
FIGURE 14. V_{ILD} 8 Outputs Switching
V_{CC} = 3.3V, T_A = 25°C

Extended Specifications (Continued)

2. On a high output, the HIGH level will not drop below an input threshold high level of 2.0V after the transition of the output. *Figures 15* and *16*. Numbered output curve deflections are a result of 10 mV incremental changes on the high input signal level.



TL/F/12010–15

FIGURE 15. V_{IHD}
7 Outputs Switching
V_{CC} = 3.3V, T_A = 25°C

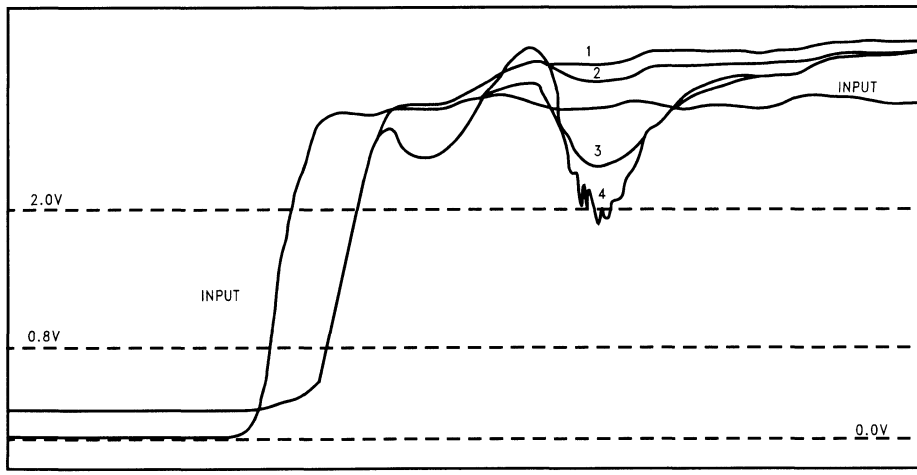


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FIGURE 16. V_{IHD}
8 Outputs Switching
V_{CC} = 3.3V, T_A = 25°C

Extended Specifications (Continued)

3. If the natural ringing, other than the initial bounce, of the output violates an input threshold level, the starting voltage level is noted and monitored until a 100 mV amplitute change towards threshold. If no amplitude change occurs, then the next peak or valley on the output is monitored for input threshold violation. *Figure 17.*
4. The propagation delay is monitored and is determined a failure when it exceeds the MOS propagation delay for that transition.
5. Gross failures including oscillation and functional state changes.

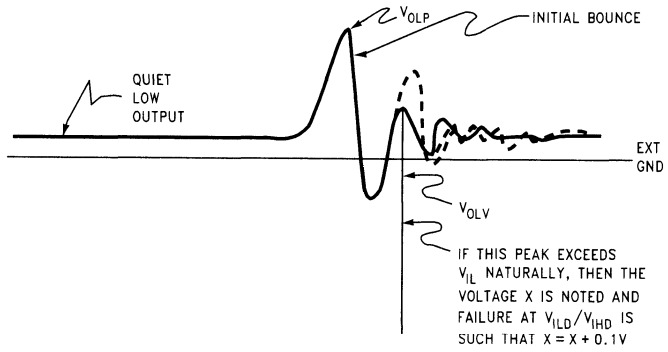

FIGURE 17

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into low Voltage devices. This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 18.*

Example:

If signal appears at output #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device and duty cycle.

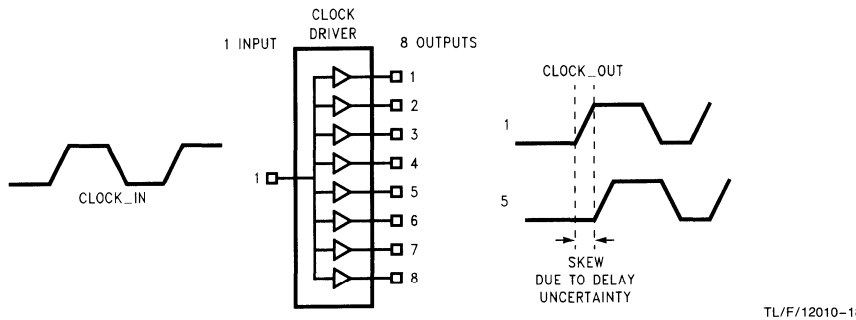

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FIGURE 18. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

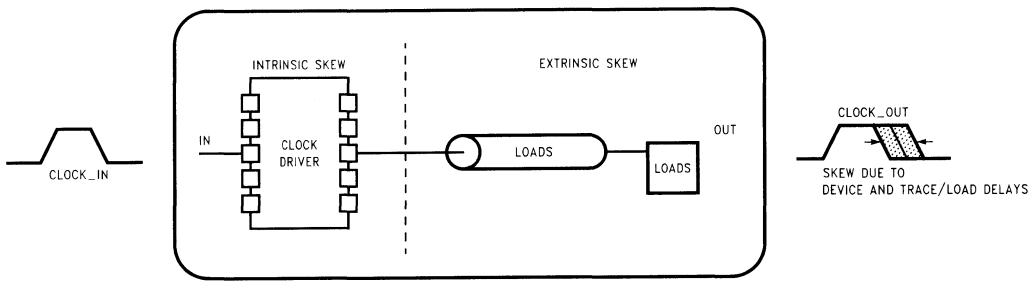

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FIGURE 19. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns

If extrinsic skew = 1 ns → − 1 ns

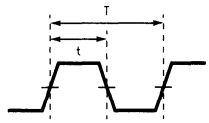
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

Skew Definitions and Examples (Continued)

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *HIGH* or *LOW* in a given clock cycle.



TL/F/12010–20

Duty Cycle = t/T * 100%

FIGURE 20. Duty Cycle Calculation

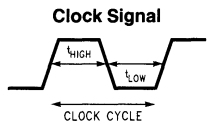


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FIGURE 21. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

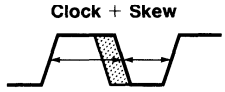

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FIGURE 22. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE II

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

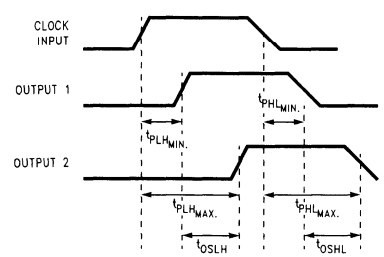
$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example



TL/F/12010–23

FIGURE 23. t_{OSLH}, t_{OSHL}

Section 3

Quality and Reliability

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National Semiconductor

Quality and Reliability

Introduction

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe "real life" operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a "world class" supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification program when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Specific family qualification data is available and may be obtained by calling our customer response center at 1-800-272-9959 within the US. 1-800-258-6768 in Canada.

Qualification Requirements for Logic Integrated Circuits

Test	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T_A = 125°C	77
High Temperature Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature-Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature-Humidity-Bias with Preconditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	77
Autoclave	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles −65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

Quality Information and Communication (QUIC) System

BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

HOW A CUSTOMER LINKS TO QUIC

1. Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)

   IBM/PC compatible computer with at least 128k memory.

   Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).

   Touch tone phone.
2. Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
3. Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the "User Friendliness" of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

Wafer Level Reliability (WLR)

BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0–10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of "good" devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to:

1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
2. Reduce process qualification cycle time.
3. Improve process qualification success rate.
4. Assess reliability trends of production processes.
5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies such as those used by the Low Voltage logic families.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

Wafer Level Reliability (WLR) (Continued)

Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

Metal Stress Voids

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

Gate Oxide Integrity:

JEDEC J_{RAMP}, V_{RAMP} and Q_{BD} test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

Passivation Integrity

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

Electrostatic Discharge Sensitivity (ESD)

Low Voltage logic products are manufactured using either submicron CMOS or BiCMOS technology. To protect these circuits from the harmful effects of Human Body Model (HBM) ESD events, proprietary protection circuitry along with traditional ESD diodes are used.

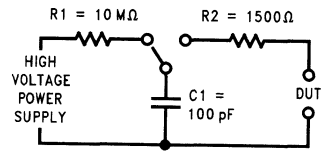
By design, this circuitry improves immunity to both HBM and Electrical Overstress (EOS). Protection from pin-to-ground (GND), pin-to-V_{CC} is achieved through traditional diodes. Additional protection is provided via proprietary solutions that provide a low resistance path between V_{CC} and GND during various ESD zap combinations.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable affect on speed or increase in capacitance.

Low voltage logic ESD sensitivity is guaranteed greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

HBM Test Circuit



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Normal handling precautions should be observed as in the case of any semiconductor.

Repeatability of HBM ESD Results

Research has shown that stray capacitance in the ESD testers can cause device degradation or early ESD failure. For this discussion, stray capacitance is defined as capacitance that is distributed from the device socket through the board connections and lines to the HBM R-C network: 1500Ω ±1%, and charging capacitor: 100 pF ±10%. This degradation is seen mainly in N-channel protection and is caused by the charge delivered by the stray capacitance, charge that is not accounted for in MIL STD-883C/3015.7.

Lowering stray capacitance in the tester is advocated by the EOS/ESD Association under their EOS/ESD-S5.1-1991 spec. This specification helps to improve tester-to-tester repeatability independent of part type, by designating ESD zap waveform guidelines, similar in fashion to those of MIL STD-883C/3015.7. The waveform guidelines ensure that stray capacitance of the tester will be limited to 30 pF or less.

The EOS/ESD Association has recommended EOS/ESD-S5.1-1991 be used in conjunction with MIL STD-883C/3015.7 to provide a better testing environment as well as the most representative HBM ESD zap waveform. Using this methodology will provide greater repeatability without compromising the intent of HBM ESD testing.

Repeatability of HBM ESD Results

(Continued)

More information on stray capacitance and the EOS/ESD S5.1-1991 can be found in the 1993 EOS/ESD Symposium Proceedings' article "Analysis of HBM ESD testers and specifications using a 4th order lumped element model", pp. 129–137.

Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of faster speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0 μm geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed "Absolute Maximum Ratings" causing unrecoverable device damage.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include "Absolute Maximum Ratings" and adherence to this specification is essential in ensuring component and system level reliability.

1. A. Amerasekera, A. Chatterjee, *"An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies"*, EOS/ESD Symposium, p5B.6.1.

Latchup Testing

Latchup in CMOS and BiCMOS circuits can vary in severity from being a temporary condition of excessive I_{CC} current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the "FACT Advanced CMOS Logic Data book" Lit. # 40019).

National has characterized its Low Voltage logic for robustness using an IMCS 4600 Automated Latchup Test System, complying to the JEDEC Standard No. 17. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of time.

The JEDEC Standard No. 17 is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptability/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short, the JEDEC Standard No. 17 follows a sequence of:

1. Apply power
2. Setup I/O conditions to place device in desired state
3. Apply trigger source for desired duration
4. Measure supply current
5. Remove power supply if $I_{CC} \geq$ test limit
6. Inspect for electrical damage

For Low Voltage logic products, all logic states are checked for a susceptibility to latchup with all outputs high, all outputs low, and all outputs in TRI-STATE®. If the device is a bi-directional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

For products with clamp diodes at inputs and outputs, a Positive and a Negative Current Trigger are required as stimuli for latchup. National characterizes latchup testing on all low voltage logic products at 125°C and at maximum supply voltage.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.

Section 4

LCX Family

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National Semiconductor

LCX
Low Voltage High Speed CMOS Logic with 5V Tolerant Inputs and Outputs

Features	Advantages
5V tolerant inputs and outputs	Interfaces seamlessly to 3V and/or 5V devices
High speed (6.5 ns max t_{PD} for LCX244, 4.5 ns max t_{PD} for LCX16244)	Talks to the latest high speed processor buses
Very low static (10 μA max I_{CCQ} for octals) and dynamic power	Saves power, extends battery life
Power up/down high impedance inputs and outputs	Facilitates power management and live insertion
Extended 2.0V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Balanced $\pm$24 mA output drive	Drives transmission lines down to 50Ω
Patented Quiet Series™ noise reduction circuitry	Low ground bounce, overshoot, undershoot, and EMI
Latch-up performance exceeds 500 mA, ESD performance exceeds 2000V HBM	Great for robust applications
SOIC, TSSOP, and SSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

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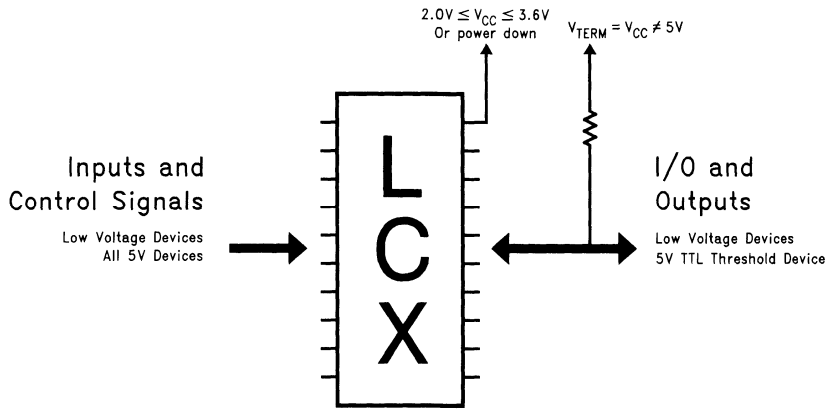
Using the Advanced Features of LCX Logic

LCX High Speed CMOS Low Voltage Logic can be used in low voltage applications just as traditional LS, F, AC, etc. logic is commonly used in 5V applications. LCX does, however, offer many additional features which allow it to perform other roles such as interfacing 3V and 5V devices, facilitating power management, isolating subsystems during power failure, and live insertion.

Interfacing 3V and 5V Devices

Though designed for low voltage operation, LCX devices are overvoltage tolerant allowing them to interface to both 5V and low voltage devices.



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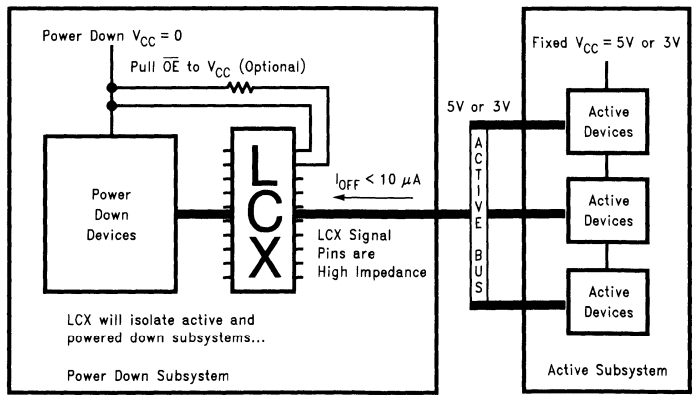
Power Management

When powered down, LCX signal pins are at high impedance so LCX devices can isolate active portions from powered down portions of a system. Pulling up the $\overline{OE}$ pin to V_{CC} during power up/down provides glitch-free power up/down operation.



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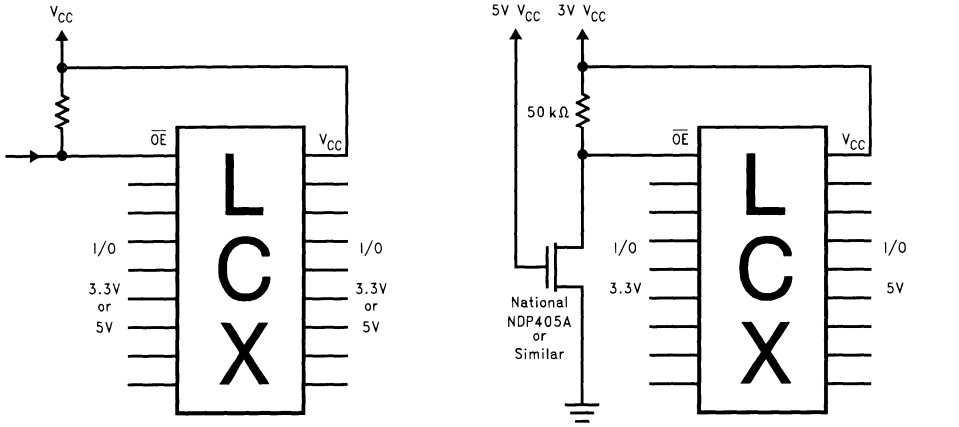
Subsystem Isolation during Power Failure

The power down high impedance feature of LCX devices also allows LCX devices to isolate 3V and 5V busses during failure of either supply. This feature also provides large telecom systems an extra measure of robustness during power failures, by isolating the active and powered down subsystems.



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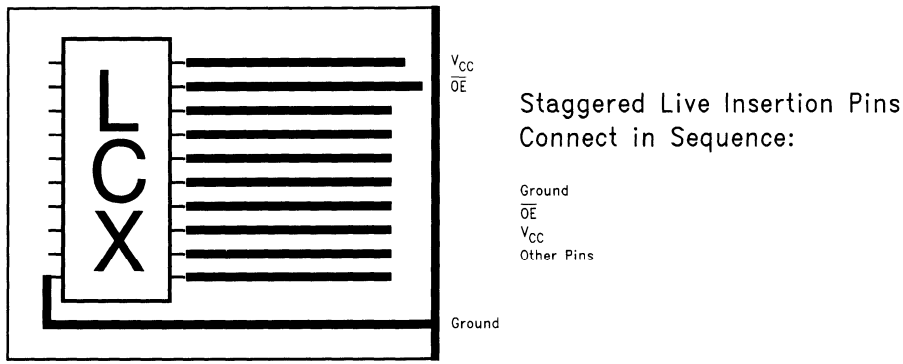
Live Insertion

If a staggered pin edge connector is implemented, LCX devices can satisfy level 2 live insertion isolation for backplane applications.



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Summary

The LCX family aids the design of robust pure 3V and mixed 3V/5V systems from small battery powered, power managed systems to large telecom systems requiring live insertion and power failure isolation. LCX serves these diverse needs and is a broad, low cost, high speed, low power, low noise, multi-sourced family.

National Semiconductor

ADVANCE INFORMATION

NC7LCX00
Low Voltage Single 2-Input NAND Gate with 5V Tolerant Inputs

General Description

The LCX000 contains a single 2-input NAND gate. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

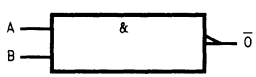
Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol

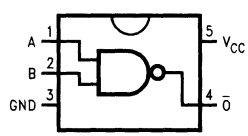
IEEE/IEC



TL/F/12664–1

Connection Diagram

Pin Assignment for TinyPak



TL/F/12664–2

Pin Names	Description
A, B	Inputs
$\overline{O}$	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX00M5 NC7LCX00M5X	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	5.2	1.5	6.0	ns
t_{PLH}		1.5	5.2	1.5	6.0	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX02
Low Voltage Single 2-Input NOR Gate with 5V Tolerant Inputs

General Description

The LCX02 contains a single 2-input NOR gate. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Tiny LCX logic allows designers to place logic exactiy where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

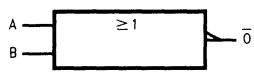
Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- 24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol

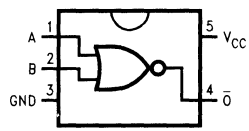
IEEE/IEC



TL/F/12665–1

Connection Diagram

Pin Assignment for TinyPak



TL/F/12665–2

Pin Names	Description
A, B	Inputs
$\overline{O}$	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX02M5 NC7LCX02MX	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time	1.5	5.2	1.5	6.0	ns
t_{PLH}		1.5	5.2	1.5	6.0	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX04
Low Voltage Single Inverter with 5V Tolerant Inputs

General Description

The LCX04 contains a single inverter. The input will tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

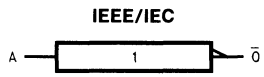
Tiny LCX logic allows designers to place logic exactly where its needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

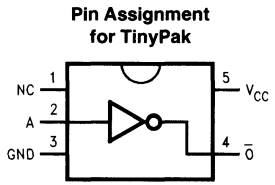
- 5V tolerant input
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance input and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12666–1

Connection Diagram



TL/F/12666–2

Pin Names	Description
A	Input
$\overline{O}$	Output
NC	No Connect

	5-Pin SOT23-5	Supplied As
Order Number	NC7LCX04M5	250 Units in Tape and Reel
	NC7LCX04M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time	1.5	5.2	1.5	6.0	ns
t_{PLH}		1.5	5.2	1.5	6.0	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCXU04
Low Voltage Single Unbuffered Inverter with 5V Tolerant Inputs

General Description

The LCXU04 contains a single unbuffered inverter.

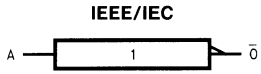
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

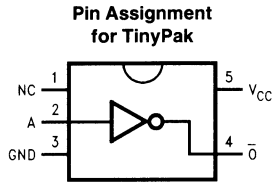
- 5V tolerant input
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance input and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12667–1

Connection Diagram



TL/F/12667–2

Pin Names	Description
A	Input
$\overline{O}$	Output
NC	No Connect

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCXU04M5 NC7LCXU04M5X	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time	1.5	5.2	1.5	6.0	ns
t_{PLH}		1.5	5.2	1.5	6.0	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	TBD	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	TBD	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	TBD	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX05
Low Voltage Single Inverter (Open Drain) with 5V Tolerant Inputs

General Description

The LCX05 contains a single open drain inverter. The input will tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

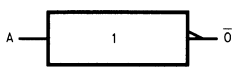
Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant input
- Power down high impedance input and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol

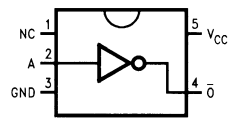
IEEE/IEC



TL/F/12668–1

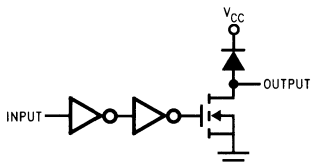
Connection Diagram

Pin Assignment for TinyPak



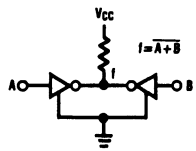
TL/F/12668–2

Logic Diagram



TL/F/12668–3

Typical Application



TL/F/12668–4

Note: Can be extended to more than 2 inputs.

Pin Names	Description
A_n	Input
$\overline{O}_n$	Output
NC	No Connection

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX05M5	250 Units in Tape and Reel
	NC7LCX05M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

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National Semiconductor

ADVANCE INFORMATION

NC7LCX08
Low Voltage Single 2-Input AND Gate with 5V Tolerant Inputs

General Description

The LCX08 contains a single 2-input AND gate. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

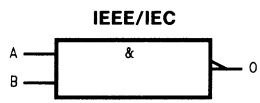
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

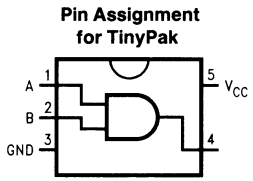
- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12669–1

Connection Diagram



TL/F/12669–2

Pin Names	Description
A, B	Inputs
O	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX08M5 NC7LCX08M5X	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	5.5	1.5	6.2	ns
t_{PHL}		1.5	5.5	1.5	6.2	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX14
Low Voltage Single Inverter with 5V Tolerant Schmitt Trigger Inputs

General Description

The LCX14 contains a single inverter with a Schmitt trigger input. It is capable of transforming a slowly changing input signal into a sharply defined, jitter-free output signal. In addition, it has greater noise margin than conventional inverters.

The LCX014 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

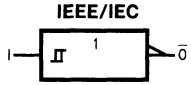
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

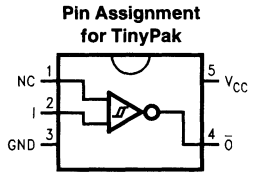
- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance input and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/ EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12670–1

Connection Diagram



TL/F/12670–2

Pin Names	Description
I	Input
Ō	Output

Truth Table

Input	Output
A	Ō
L	H
H	L

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX14M5	250 Units in Tape and Reel
	NC7LCX14M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{t+}	Positive Input Threshold		3.0	1.2	2.2	V
V_{t-}	Negative Input Threshold		3.0	0.6	1.5	V
V_H	Hysterisis		3.0	0.4	1.2	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.5	1.5	7.5	ns
t_{PLH}		1.5	6.5	1.5	7.5	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX32
Low Voltage Single 2-Input OR Gate with 5V Tolerant Inputs

General Description

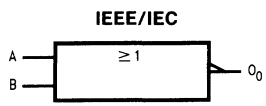
The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The NC7LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

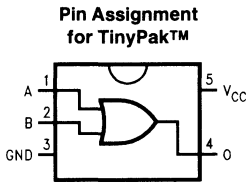
- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12671–1

Connection Diagram



TL/F/12671–2

Pin Names	Description
A, B	Inputs
O	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX32M5	250 Units in Tape and Reel
	NC7LCX32M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	5.5	1.5	6.2	ns
t_{PLH}		1.5	5.5	1.5	6.2	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX38
Low Voltage Single 2-Input NAND Gate (Open Drain) with 5V Tolerant Inputs

General Description

The LCX38 contains a single 2-input open drain NAND gate. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

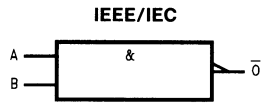
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

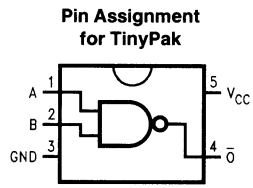
- 5V tolerant inputs
- 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12672–1

Connection Diagram



TL/F/12672–2

Pin Names	Description
A, B	Inputs
$\overline{O}$	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX38M5 NC7LCX38M5X	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		+24 +12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ to V_{CC}				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PZL}	Propagation Delay	1.5	5.2	1.5	6.0	ns
t_{PLZ}		1.5	TBD	1.5	TBD	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

NC7LCX86
Low Voltage Single 2-Input Exclusive-OR Gate with 5V Tolerant Inputs

General Description

The LCX86 contains a single 2-input exclusive-OR gate. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

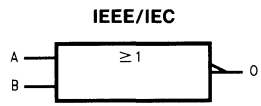
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

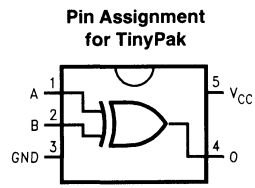
- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs
- 2.0V–3.6V V_{CC} supply operation
- Supports live insertion/withdrawal
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12673–1

Connection Diagram



TL/F/12673–2

Pin Names	Description
A, B	Inputs
O	Output

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX86M5	250 Units in Tape and Reel
	NC7LCX86M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
(T_A)	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.5	1.5	7.0	ns
t_{PLH}		1.5	6.5	1.5	7.0	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

NC7LCX125
Low-Voltage Single Buffer with 5V Tolerant Inputs and Outputs

General Description

The LCX125 contains a single non-inverting buffer with a TRI-STATE® output. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

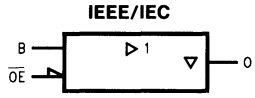
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

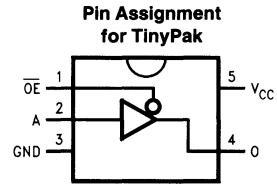
- 5V tolerant inputs and output
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12674–1

Connection Diagram



TL/F/12674–2

Pin Names	Description
A, $\overline{OE}$	Inputs
O	Output

Truth Table

Inputs		Output
A	$\overline{OE}$	O
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX125M5	250 Units in Tape and Reel
	NC7LCX125M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

NC7LCX126
Low-Voltage Single Buffer with 5V Tolerant Inputs and Outputs

General Description

The LCX126 contains a single non-inverting buffer with a TRI-STATE® output. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

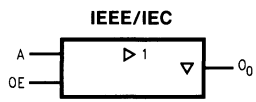
Tiny LCX logic allows designers to place logic exactly where it's needed on a printed circuit board. This eliminates excessive signal routing, saving board space and cost, improving reliability and reducing delays and skew introduced by the signal traces.

Tiny LCX logic in the TinyPak™ is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

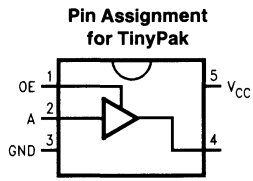
- 5V tolerant inputs and output
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and output
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12675–1

Connection Diagram



TL/F/12675–2

Pin Names	Description
A, OE	Inputs
O	Output

Truth Table

Inputs		Output
A	OE	O
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

	5-Pin SOT-23-5	Supplied As
Order Number	NC7LCX126M5	250 Units in Tape and Reel
	NC7LCX126M5X	3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +6.0		V
V_I	DC Input Voltage	−0.5 to +6.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX00
Low Voltage Quad 2-Input NAND Gate with 5V Tolerant Inputs

General Description

The LCX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

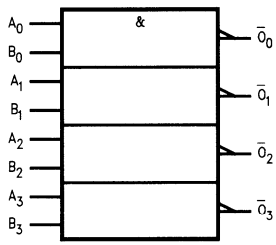
The 74LCX00 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 00
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

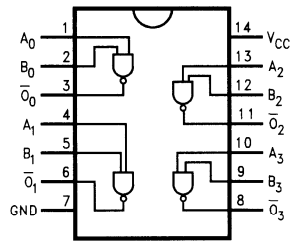
IEEE/IEC



TL/F/12408–1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12408–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX00M 74LCX00MX	74LCX00SJ 74LCX00SJX	74LCX00MTC 74LCX00MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these iimits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX02
Low Voltage Quad 2-Input NOR Gate with 5V Tolerant Inputs

General Description

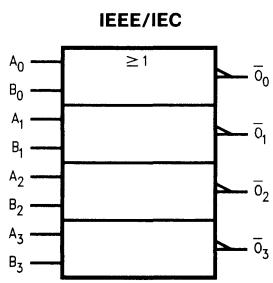
The LCX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX02 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

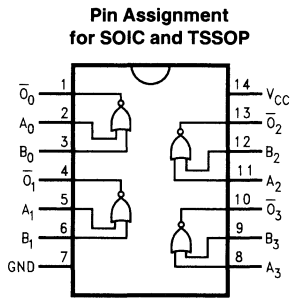
- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- 24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 02
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12409–1

Connection Diagram



TL/F/12409–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX02M 74LCX02MX	74LCX02SJ 74LCX02SJX	74LCX02MTC 74LCX02MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Time	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX04
Low Voltage Hex Inverter with 5V Tolerant Inputs

General Description

The LCX04 contains six inverters. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

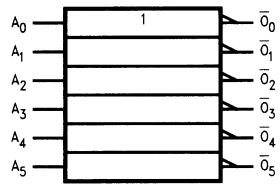
The 74LCX04 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patentend Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 04
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

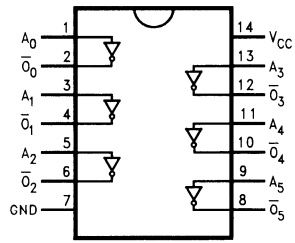
IEEE/IEC



TL/F/12410–1

Connection Diagram

Pin Assignment
for SOIC and TSSOP



TL/F/12410–2

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX04M 74LCX04MX	74LCX04SJ 74LCX04SJX	74LCX04MTC 74LCX04MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Time	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (T_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

74LCX05
Low Voltage Hex Inverter (Open Drain) with 5V Tolerant Inputs

General Description

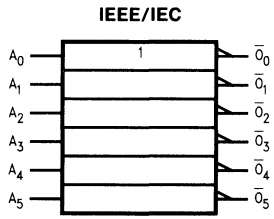
The 74LCX05 is an open drain hex inverter. The 74LCX05 requires the addition of an external resistor to perform a wire-NOR function. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX05 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

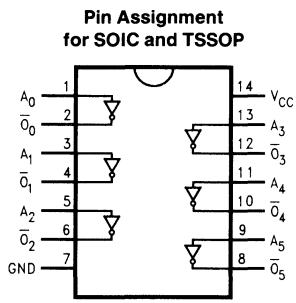
- 5V tolerant inputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 05
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



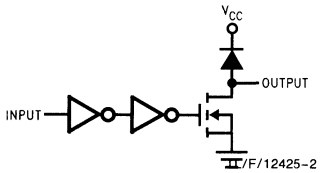
TL/F/12425–4

Connection Diagram



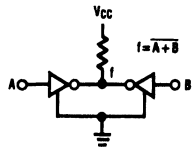
TL/F/12425–5

Logic Diagram



TL/F/12425–2

Typical Application



TL/F/12425–3

Note: Can be extended to more than 2 inputs.

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX05M 74LCX05MX	74LCX05SJ 74LCX05SJX	74LCX05MTC 74LCX05MTCX
See NS Package Number	M14A	M14D	MTC14

National Semiconductor

74LCX08
Low Voltage Quad 2-Input AND Gate with 5V Tolerant Inputs

General Description

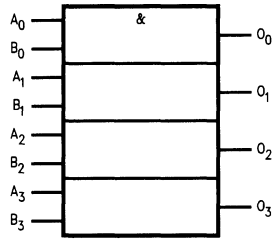
The LCX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 08
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 150V

Logic Symbol

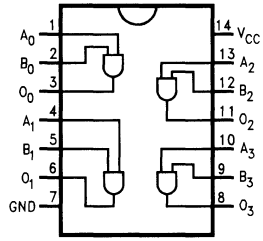
IEEE/IEC



TL/F/12411–1

Connection Diagram

Pin Assignment for SOIC JEDEC, EIAJ and TSSOP



TL/F/12411–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX08M 74LCX08MX	74LCX08SJ 74LCX08SJX	74LCX08MTC 74LCX08MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	5.5 5.5	1.5 1.5	6.2 6.2	ns
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

74LCX10
Low Voltage Triple 3-Input NAND Gate with 5V Tolerant Inputs

General Description

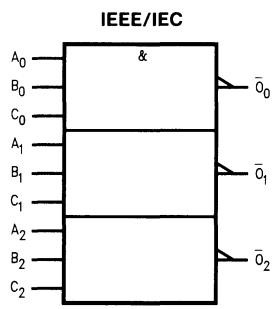
The 74LCX10 is a triple 3-input NAND gate with buffered outputs. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX10 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

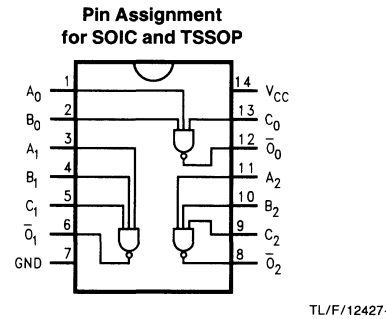
- 5V tolerant inputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 10
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12427–1

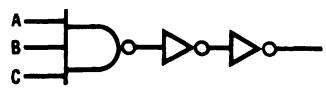
Connection Diagram



TL/F/12427–3

Pin Descriptions

Pin Names	Description
A_n, B_n, C_n	Inputs
$\overline{O}_n$	Outputs



$Y = \overline{ABC}$

TL/F/12427–2

National Semiconductor

ADVANCE INFORMATION

74LCX11
Low Voltage Triple 3-Input AND Gate with 5V Tolerant Inputs

General Description

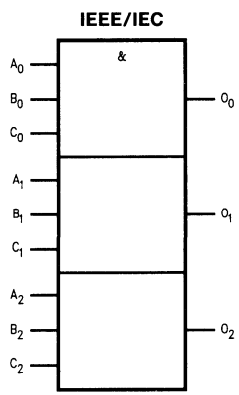
The 74LCX11 is a triple 3-input AND gate with buffered outputs. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX11 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

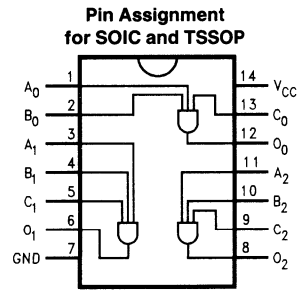
- 5V tolerant inputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 11
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



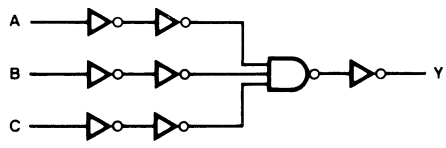
TL/F/12426–3

Connection Diagram



TL/F/12426–4

Pin Names	Description
A_n, B_n, C_n	Inputs
O_n	Outputs



TL/F/12426–2

National Semiconductor

74LCX14
Low Voltage Hex Inverter with 5V Tolerant Schmitt Trigger Inputs

General Description

The LCX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

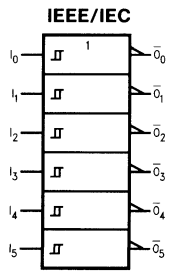
The LCX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

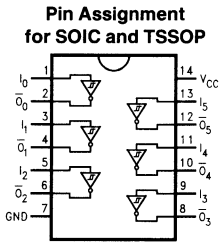
- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/ EMI reduction circuitry
- Functionally compatible with 74 series 14
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12412–1

Connection Diagram



TL/F/12412–2

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

Input	Output
A	$\overline{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX14M 74LCX14MX	74LCX14SJ 74LCX14SJX	74LCX14MTC 74LCX14MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{t+}	Positive Input Threshold		3.0	1.2	2.2	V
V_{t-}	Negative Input Threshold		3.0	0.6	1.5	V
V_H	Hysterisis		3.0	0.4	1.2	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX32
Low Voltage Quad 2-Input OR Gate with 5V Tolerant Inputs

General Description

The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

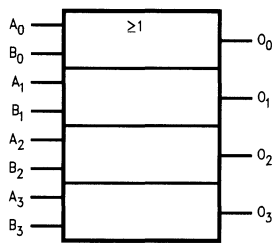
The 74LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 32
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 150V

Logic Symbol

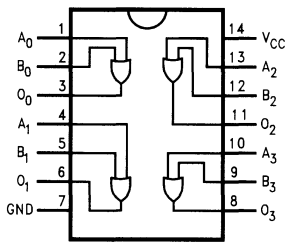
IEEE/IEC



TL/F/12413–1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12413–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX32M 74LCX32MX	74LCX32SJ 74LCX32SJX	74LCX32MTC 74LCX32MTCX
NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	5.5 5.5	1.5 1.5	6.2 6.2	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX38
Low Voltage Quad 2-Input NAND Gate (Open Drain) with 5V Tolerant Inputs

General Description

The LCX38 contains four 2-input open drain NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

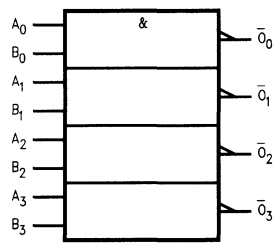
The 74LCX38 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 38
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

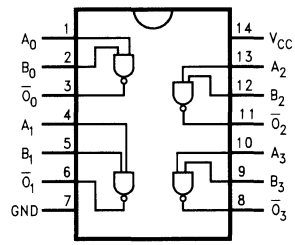
IEEE/IEC



TL/F/12574–1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12574–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX38M 74LCX38MX	74LCX38SJ 74LCX38SJX	74LCX38MTC 74LCX38MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		+24 +12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ to V_{CC}				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PZL}	Propagation Delay	1.5	5.2	1.5	6.0	ns
t_{PLZ}		1.5	6.5	1.5	7.0	
t_{OSHL}	Output to Output Skew (Note 1)		1.0			ns
t_{OSLH}			1.0			

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

The LCX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

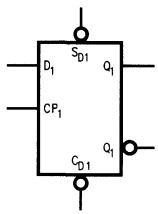
Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- 5V tolerant inputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_C supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 74
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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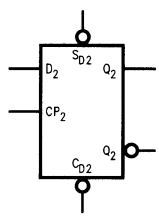
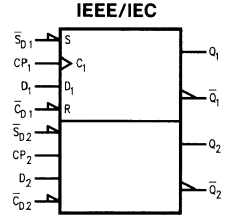


TL/F/12414–2

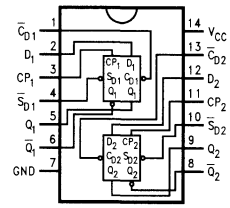
IEEE/IEC



TL/F/12414–3

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12414–4

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX74M 74LCX74MX	74LCX74SJ 74LCX74SJX	74LCX74MTC 74LCX74MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width CP and $\overline{C}_D$, $\overline{S}_D$	3.3		3.3		ns
t_{rem}	Removal Time	2.0		2.5		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX86
Low Voltage Quad 2-Input Exclusive-OR Gate with 5V Tolerant Inputs

General Description

The LCX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

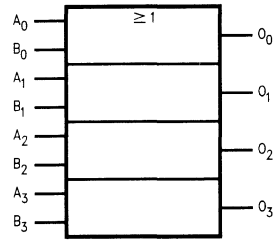
The 74LCX86 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs
- 2.0V–3.6V V_{CC} supply operation
- Supports live insertion/withdrawal
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 86
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

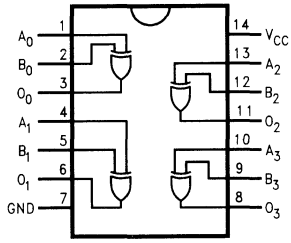
IEEE/IEC



TL/F/12415–1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12415–2

Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX86M 74LCX86MX	74LCX86SJ 74LCX86SJX	74LCX86MTC 74LCX86MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
(T_A)	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

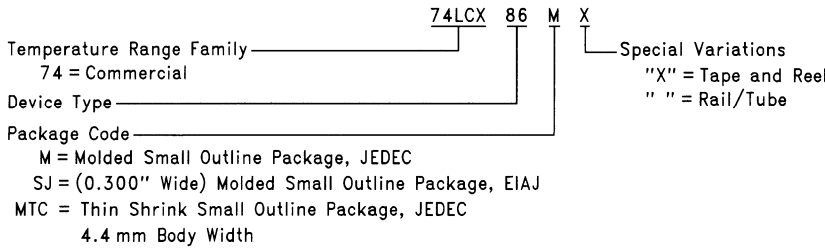
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX86 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12415–3

National Semiconductor

PRELIMINARY

74LCX109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

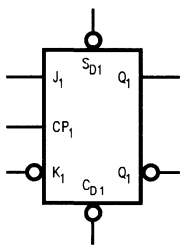
The 74LCX109 are dual J-$\overline{K}$ flip-flops. Each flip-flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX109 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

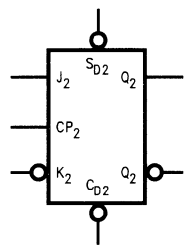
Features

- 5V tolerant inputs
- 7.0 ns tpd max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 109
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols

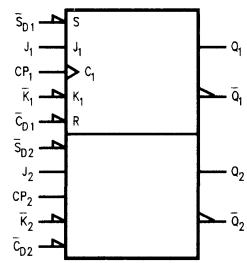


TL/F/12423–3



TL/F/12423–4

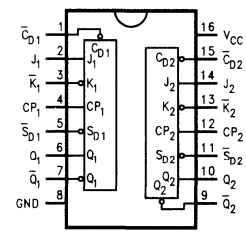
IEEE/IEC



TL/F/12423–6

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12423–5

Pin Names	Description
$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Information	74LCX109M 74LCX109MX	74LCX109SJ 74LCX109SJX	74LCX109MTC 74LCX109MTCX
See NS Package Number	M16A	M16D	MTC16

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Truth Table (each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level

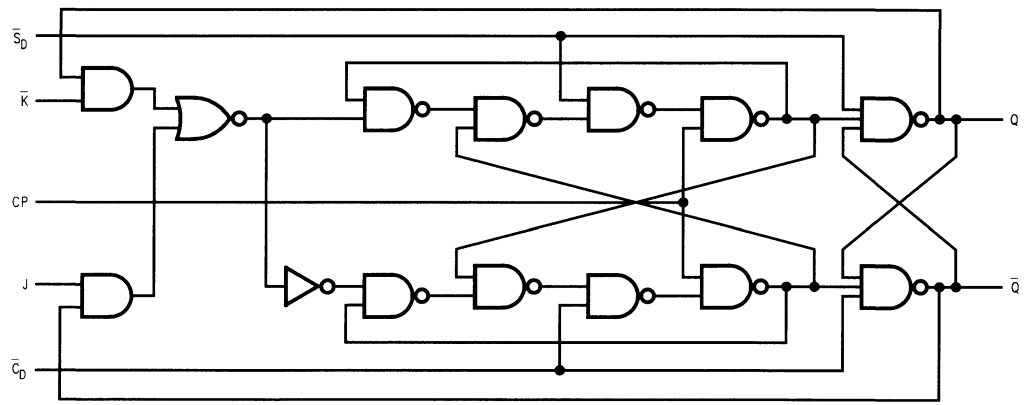
L = LOW Voltage Leel

⌐ = LOW-to-HIGH Transition

X = Immaterial

$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



TL/F/12423–7

Please note that this diagram is provided only for the understanding og logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	5.5 5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S/C	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width CP and S/C	3.3		3.3		ns
t_{rem}	Removal Time	2.0		2.5		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX112
Low Voltage Dual J-K Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

The 74LCX112 are dual J-K flip-flops. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

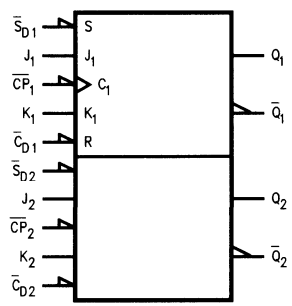
The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 7.0 ns tpd max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 112
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols

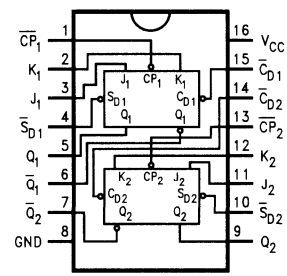
IEEE/IEC



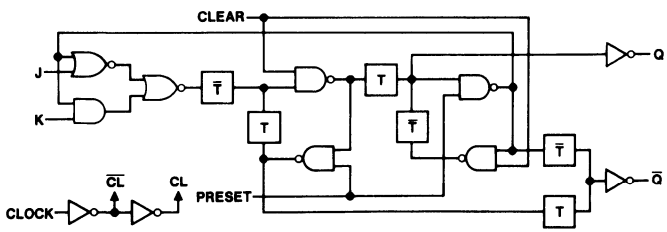
TL/F/12424–4

Connection Diagram

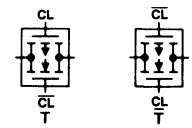
Pin Assignment for SOIC and TSSOP



TL/F/12424–5



TL/F/12424–2



TL/F/12424–3

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX112M 74LCX112MX	74LCX112SJ 74LCX112SJX	74LCX112MTC 74LCX112MTCX
See NS Package Number	M16A	M16D	MTC16

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	5.5 5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S/C	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width CP and S/C	3.3		3.3		ns
t_{rem}	Removal Time	2.0		2.5		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX125
Low-Voltage Quad Buffer with 5V Tolerant Inputs and Outputs

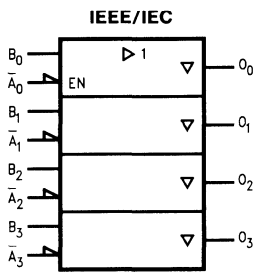
General Description

The LCX125 contains four independent non-inverting buffers with TRI-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

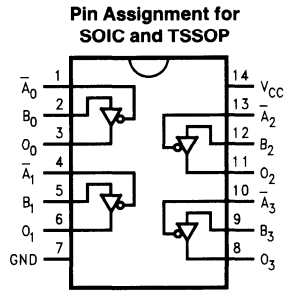
- 5V tolerant inputs and outputs
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 125
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 100V

Logic Symbol



TL/F/12416–1

Connection Diagram



TL/F/12416–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX125M 74LCX125MX	74LCX125SJ 74LCX125SJX	74LCX125MTC 74LCX125MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX138
Low Voltage 1-of-8 Decoder/Demultiplexer with 5V Tolerant Inputs

General Description

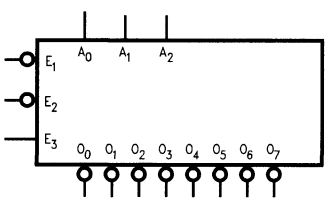
The LCX138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LCX138 devices or a 1-of-32 decoder using four LCX138 devices and one inverter.

The 74LCX138 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

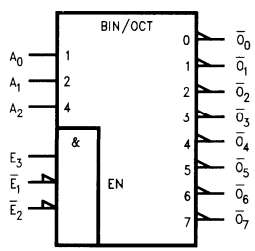
- 5V tolerant inputs
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 138
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12417–1

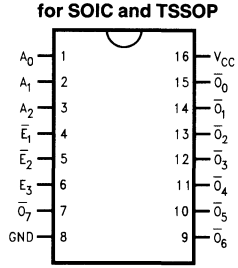
IEEE/IEC



TL/F/12417–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12417–3

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX138M 74LCX138MX	74LCX138SJ 74LCX138SJX	74LCX138MTC 74LCX138MTCX
See NS Package Number	M16A	M16D	MTC16

Functional Description

The LCX138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The LCX138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

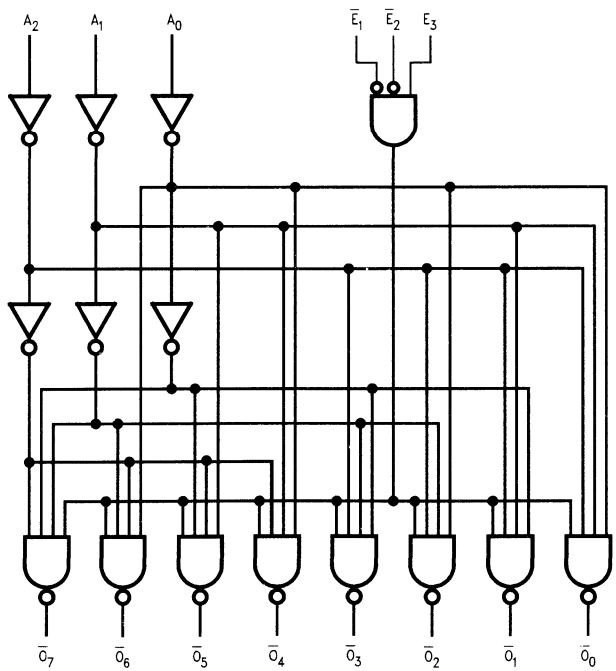
The LCX138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/12417–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to $\overline{Y}_n$	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay E_3 to $\overline{Y}_n$	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{Y}_n$	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX157
Low-Voltage Quad 2-Input Multiplexer with 5V Tolerant Inputs

General Description

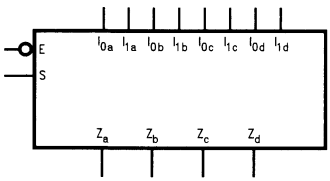
The LCX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LCX157 can also be used as a function generator.

The 74LCX157 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 157
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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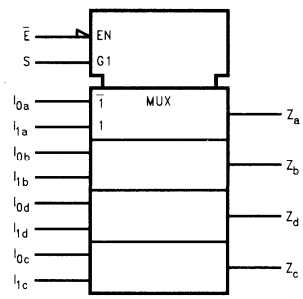
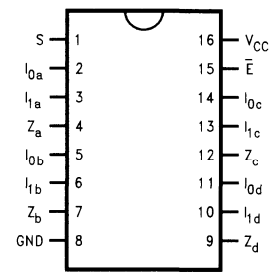
IEEE/IEC



TL/F/12465–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12465–3

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX157M 74LCX157MX	74LCX157SJ 74LCX157SJX	74LCX157MTC 74LCX157MTCX
See NS Package Number	M16A	M16D	MTC16

Functional Description

The LCX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LCX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

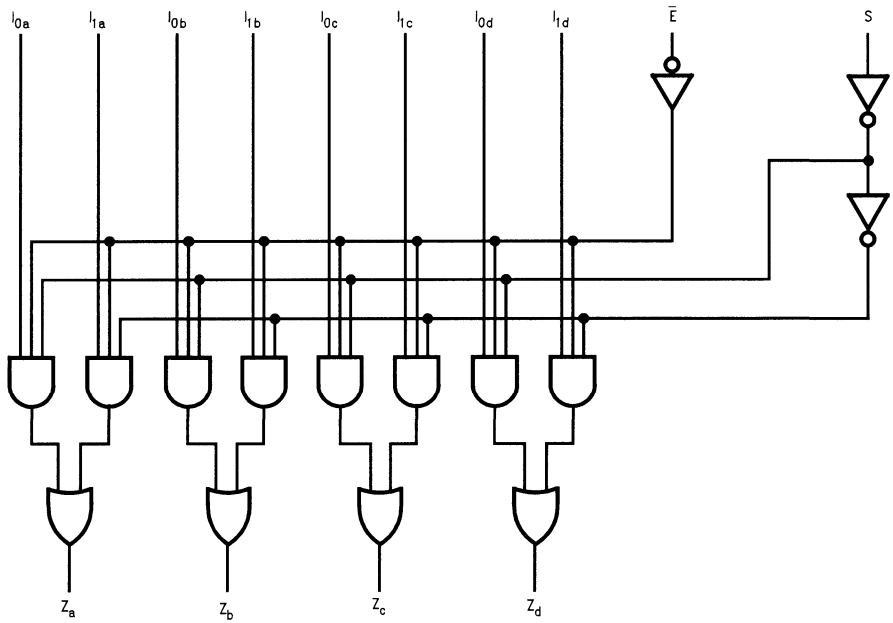
A common use of the LCX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LCX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/12465–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay $S \rightarrow Z_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay $Eb \rightarrow Z_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay $I_n \rightarrow Z_n$	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

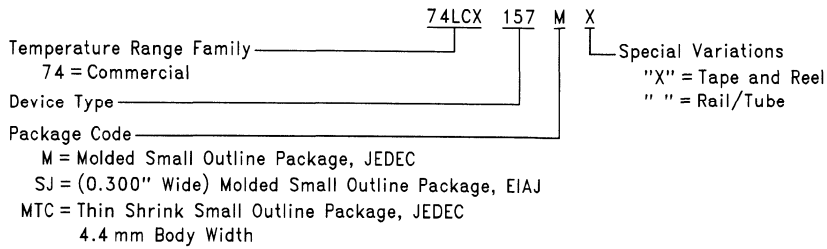
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX157 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12465–5

National Semiconductor

74LCX240
Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

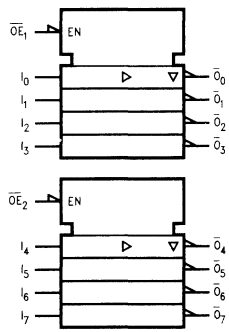
The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbol

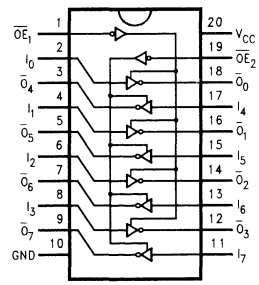
IEEE/IEC



TL/F/11993–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11993–2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE® Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP
Order Number	74LCX240WM 74LCX240WMX	74LCX240SJ 74LCX240SJX	74LCX240MSA 74LCX240MSAX	74LCX240MTC 74LCX240MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

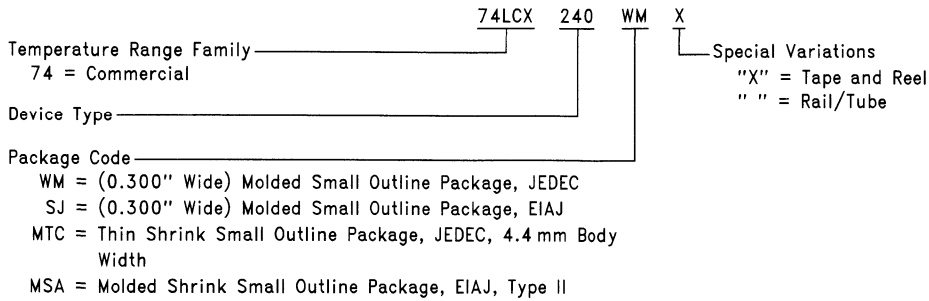
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX240 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11993–3

National Semiconductor

ADVANCE INFORMATION

74LCX241
Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

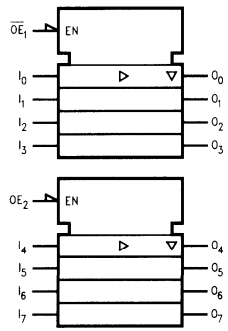
The LCX241 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 241
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbol

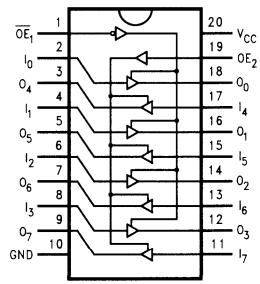
IEEE/IEC



TL/F/12639–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12639–2

Pin Names	Description
$\overline{OE}_1$, OE_2	TRI-STATE® Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I_n	
H	H	H
H	L	L
L	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP
Order Number	74LCX241WM 74LCX241WMX	74LCX241SJ 74LCX241SJX	74LCX241MSA 74LCX241MSAX	74LCX241MTC 74LCX241MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

Dynamic Switching Characteristics

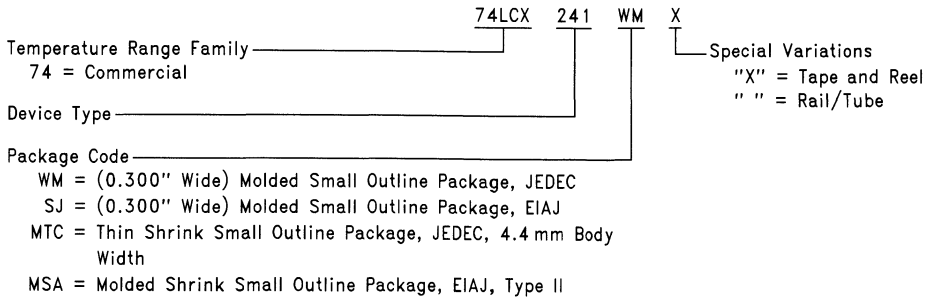
Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

74LCX241 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12639–3

National Semiconductor

74LCX244
Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX244 contains eight non-inverting buffers with TRI-STATE® outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

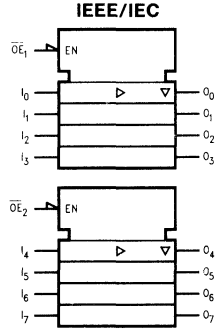
The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

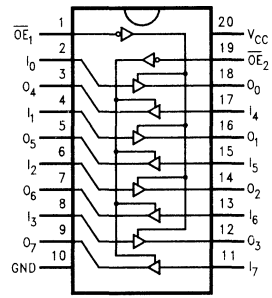
IEEE/IEC



TL/F/11994–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11994–2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX244WM 74LCX244WMX	74LCX244SJ 74LCX244SJX	74LCX244MSA 74LCX244MSAX	74LCX244MTC 74LCX244MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

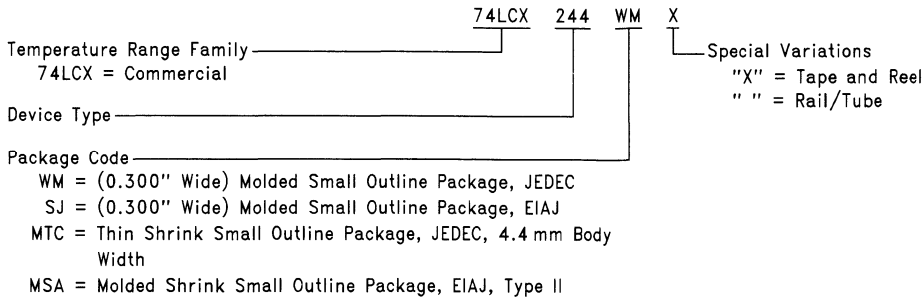
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX244 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11994–4

National Semiconductor

ADVANCE INFORMATION

74LCX2244
Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX2244 contains eight non-inverting buffers with TRI-STATE® outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX2244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 30Ω-series resistor helps reducing output overshoot and undershoot.

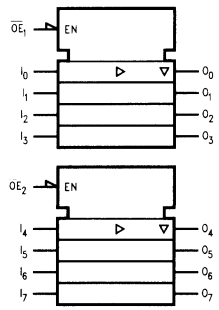
The LCX2244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 30Ω-series resistor on outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

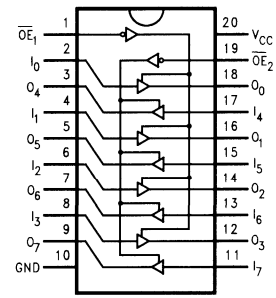
IEEE/IEC



TL/F/12569–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12569–2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level Z = High Impedance

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current			±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -12$ mA	3.0	2.0		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 12$ mA	3.0		0.8	V
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increases in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

National Semiconductor

74LCX245
Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

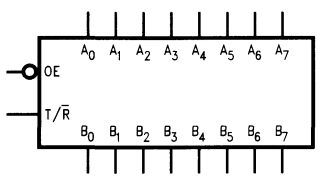
The LCX245 contains eight non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

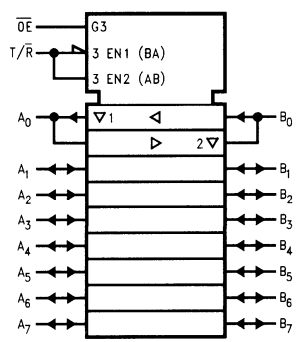
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12006–1

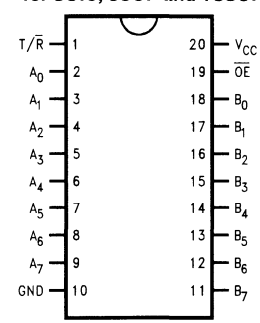
IEEE/IEC



TL/F/12006–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12006–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

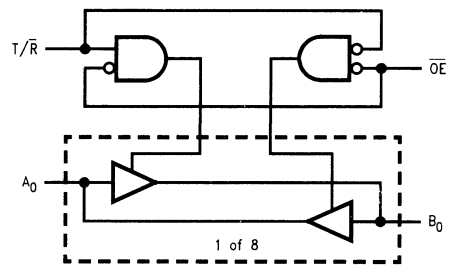
	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX245WM 74LCX245WMX	74LCX245SJ 74LCX245SJX	74LCX245MSA 74LCX245MSAX	74LCX245MTC 74LCX245MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12006–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

ADVANCE INFORMATION

74LCX2245
Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

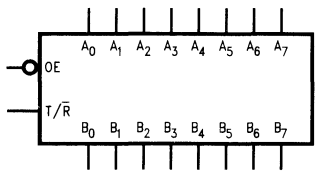
The LCX2245 contains eight non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state. The 30Ω-series resistor helps reducing output overshoot and undershoot.

The LCX2245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 30Ω-series resistor on outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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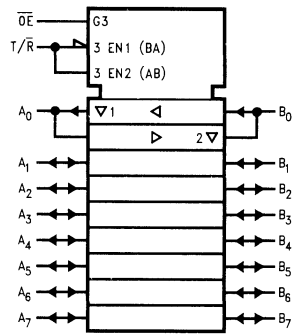
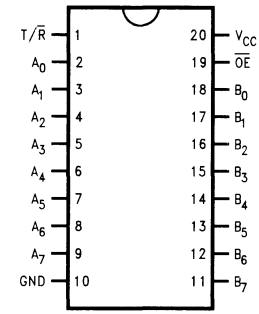
IEEE/IEC



TL/F/12573–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12573–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current			±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -12$ mA	3.0	2.0		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 12$ mA	3.0		0.8	V
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

National Semiconductor

74LCX257
Low-Voltage Quad 2-Input Multiplexer with 5V Tolerant Inputs and Outputs

General Description

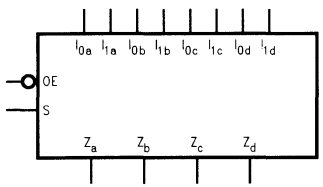
The LCX257 is a quad 2-input multiplexer with TRI-STATE® outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

The 74LCX257 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

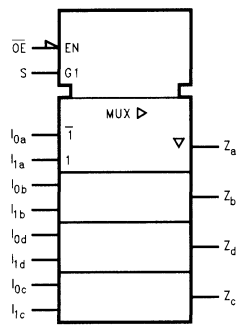
- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 257
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12466–1

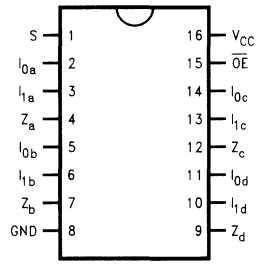
IEEE/IEC



TL/F/12466–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12466–3

Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Z_a–Z_d	TRI-STATE Multiplexer Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX257M 74LCX257MX	74LCX257SJ 74LCX257SJX	74LCX257MTC 74LCX257MTCX
See NS Package Number	M16A	M16D	MTC16

Functional Description

The LCX257 is quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

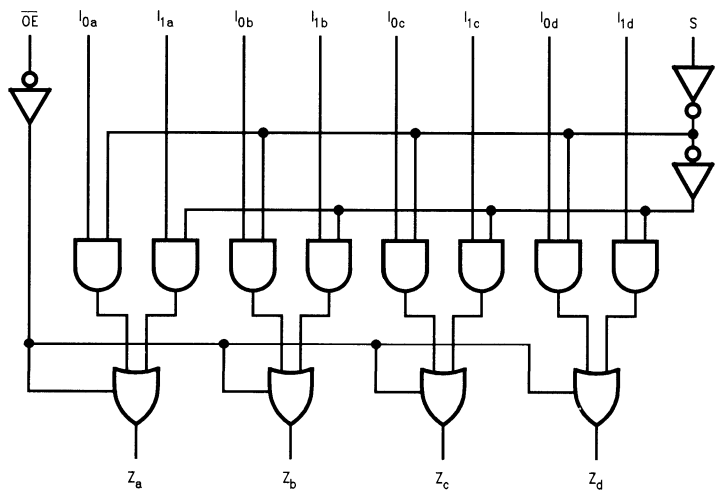
When the Output Enable ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12466–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay $S \rightarrow Z_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	ns
t_{PHL} t_{PLH}	Propagation Delay $I_n \rightarrow Z_n$	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE} \rightarrow Z_n$	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE} \rightarrow Z_n$	1.5 1.5	5.5 5.5	1.5 1.5	6.0 6.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

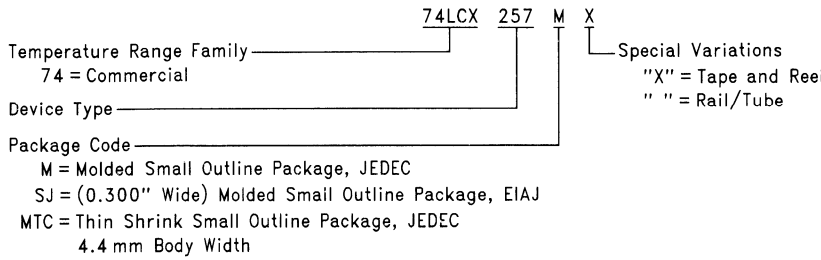
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX257 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12466–5

National Semiconductor

ADVANCE INFORMATION

74LCX273
Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

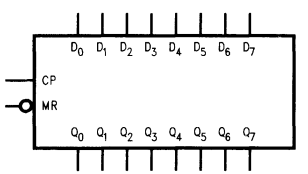
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX273 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

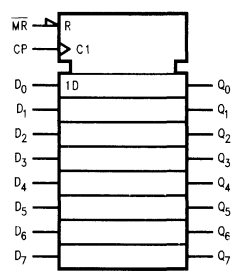
- 5V tolerant inputs and outputs
- 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 273
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/12640–1

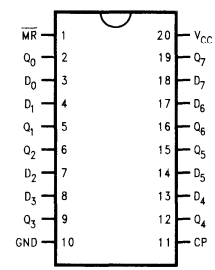
IEEE/IEC



TL/F/12640–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12640–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

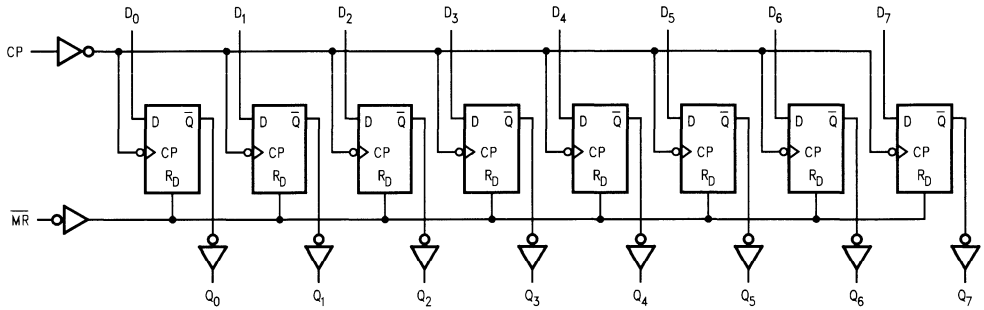
	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX273WM 74LCX273WMX	74LCX273SJ 74LCX273SJX	74LCX273MSA 74LCX273MSAX	74LCX273MTC 74LCX273MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/12604–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX373
Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

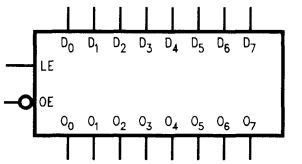
The LCX373 consists of eight latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

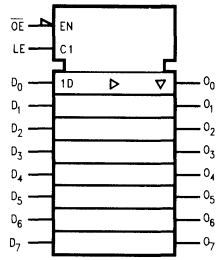
- 5V tolerant inputs and outputs
- 8.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 373
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/11995–1

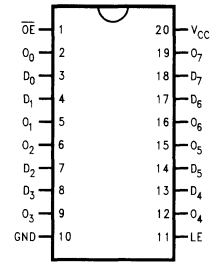
IEEE/IEC



TL/F/11995–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11995–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX373WM 74LCX373WMX	74LCX373SJ 74LCX373SJX	74LCX373MSA 74LCX373MSAX	74LCX373MTC 74LCX373MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

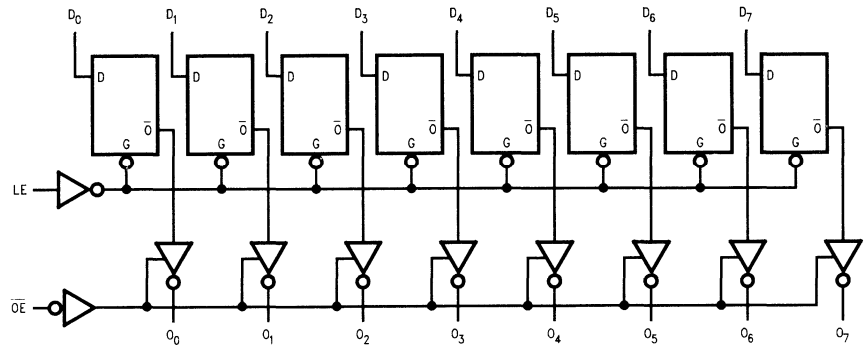
The LCX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



TL/F/11995–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

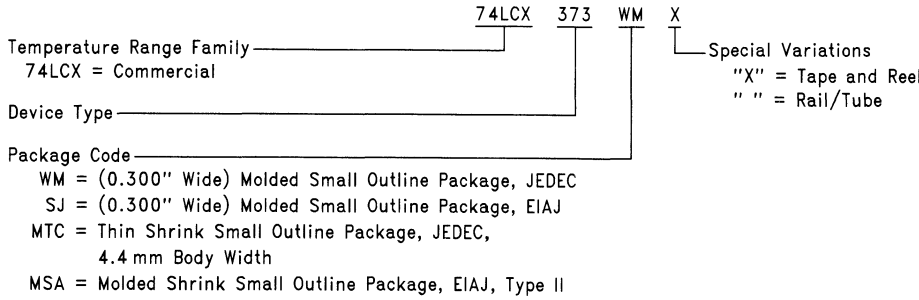
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX373 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11995–5

National Semiconductor

74LCX374
Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

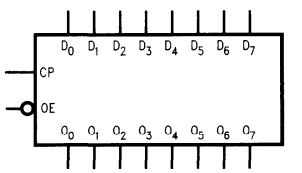
The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and TRI-STATE® outputs for bus-oriented applications. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

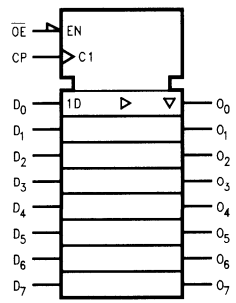
- 5V tolerant inputs and outputs
- 8.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/11996–1

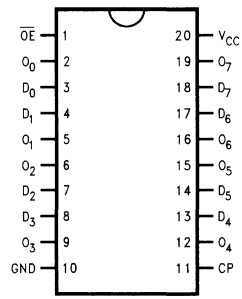
IEEE/IEC



TL/F/11996–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11996–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX374WM 74LCX374WMX	74LCX374SJ 74LCX374SJX	74LCX374MSA 74LCX374MSAX	74LCX374MTC 74LCX374MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

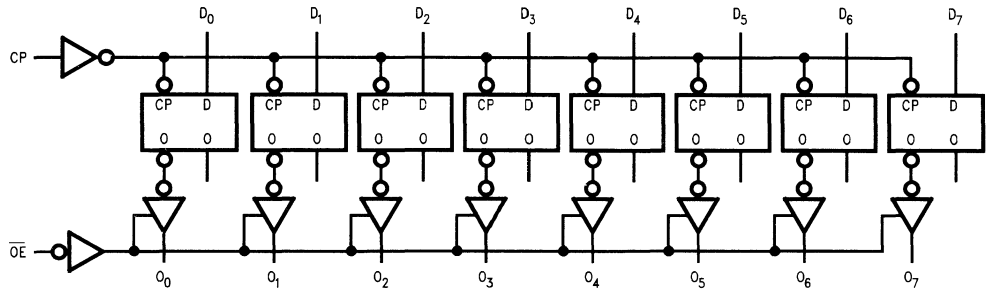
The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



TL/F/11996–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX540
Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

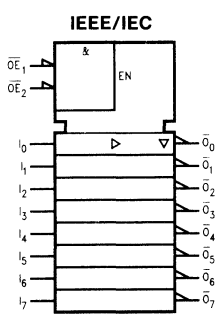
These devices are similar in function to the 'LCX240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

The LCX540 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX540 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

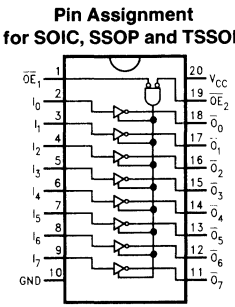
- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 540
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12403–1

Connection Diagram



TL/F/12403–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX540WM 74LCX540WMX	74LCX540SJ 74LCX540SJX	74LCX540MSA 74LCX540MSAX	74LCX540MTC 74LCX540MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.0	1.5 1.5	9.5 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

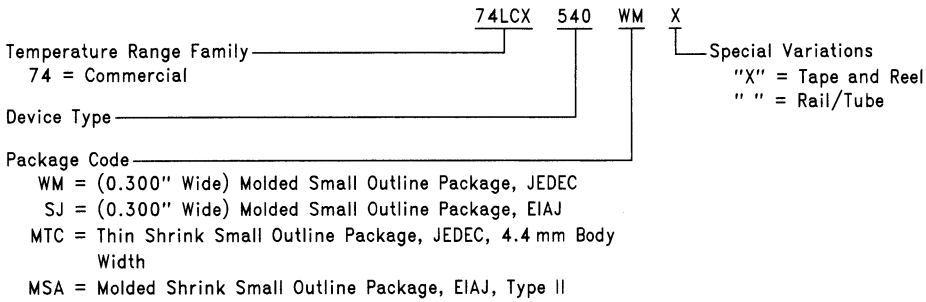
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX540 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12403–4

National Semiconductor

PRELIMINARY

74LCX541
Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 'LCX541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'LCX541 is a noninverting option of the 'LCX540.

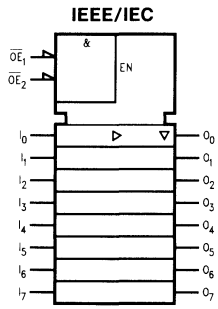
This device is similar in function to the 'LCX244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The 'LCX541 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 'LCX541 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

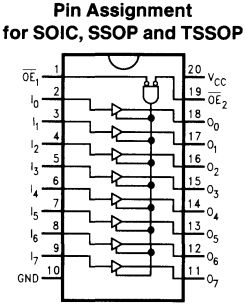
- 5V tolerant input and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/ EMI reduction circuitry
- Functionally compatible with 74 series 541
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12404–1

Connection Diagram



TL/F/12404–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX541WM 74LCX541WMX	74LCX541SJ 74LCX541SJX	74LCX541MSA 74LCX541MSAX	74LCX541MTC 74LCX541MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

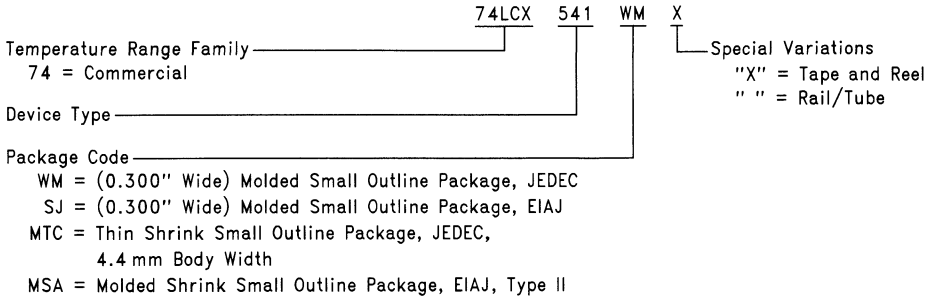
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX541 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12404–4

National Semiconductor

74LCX543
Low-Voltage Octal Registered Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

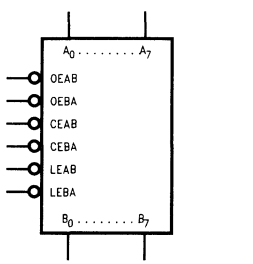
The LCX543 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX543 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

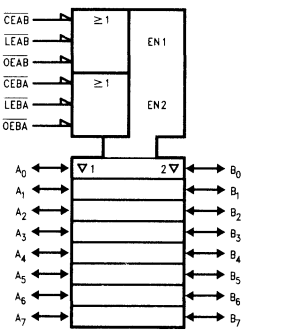
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 543
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12463–1

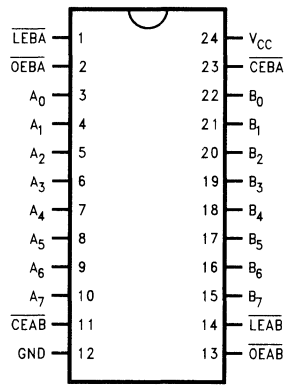
IEEE/IEC



TL/F/12463–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12463–3

	SOIC JEDEC	SSOP Type II	TSSOP
Order Number	74LCX543WM 74LCX543WMX	74LCX543MSA 74LCX543MSAX	74LCX543MTC 74LCX543MTCX
See NS Package Number	M24B	MSA24	MTC24

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0-A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0-B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Functional Description

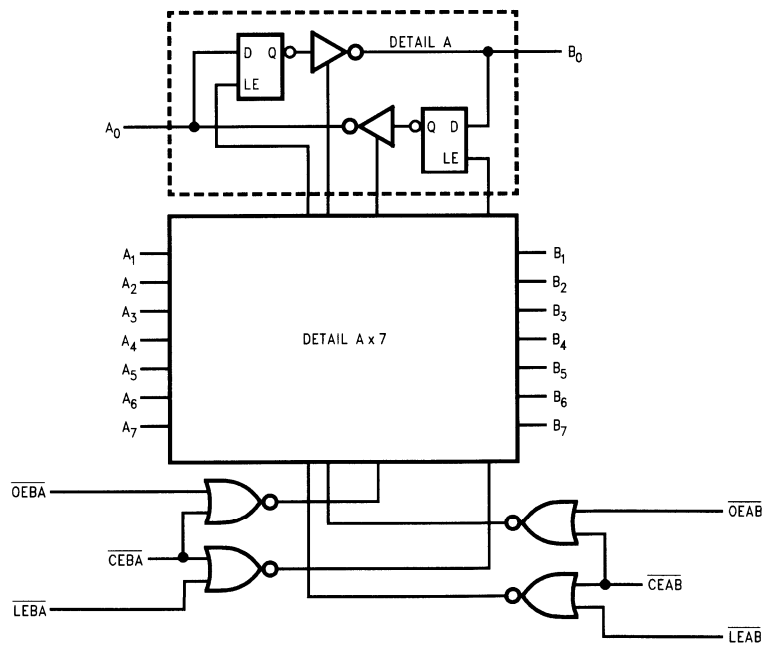
The LCX543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



TL/F/12463–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay An to Bn or Bn to An	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay $\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t_S	Setup Time, HIGH or LOW Data to $\overline{LEXX}$	2.5		2.5		ns
t_H	Hold Time, HIGH or LOW Data to $\overline{LEXX}$	1.5		1.5		ns
t_W	Pulse Width, Latch Enable, LOW	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

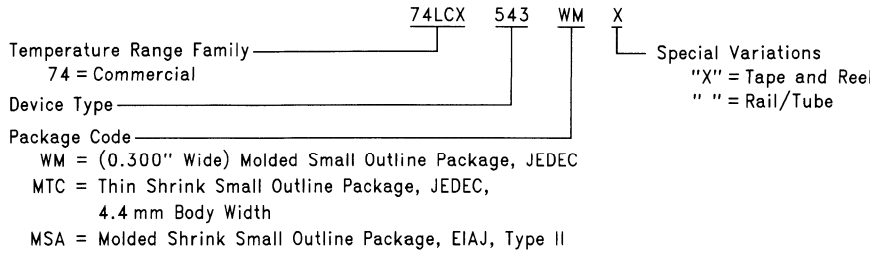
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX543 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12463-05

National Semiconductor

74LCX573
Low Voltage Octal Latch with 5V Tolerant Inputs and Outputs

General Description

The 'LCX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

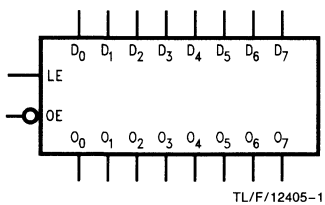
The 'LCX573 is functionally identical to the 'LCX373 but has inputs and outputs on opposite sides.

The 'LCX573 is designed for low voltage (3.3V) applications with capability of interfacing to a 5V signal environment. The 'LCX573 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

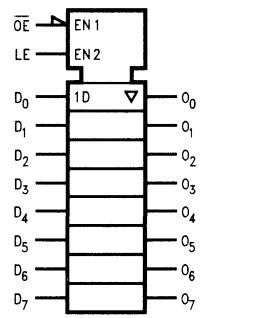
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 573
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12405–1

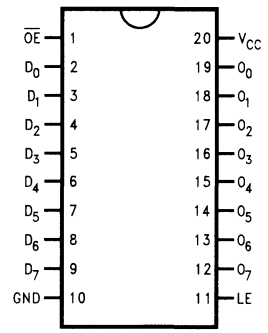
IEEE/IEC



TL/F/12405–2

Connection Diagrams

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12405–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE® Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE II	TSSOP JEDEC
Order Number	74LCX573WM 74LCX573WMX	74LCX573SJ 74LCX573SJX	74LCX573MSA 74LCX573MSAX	74LCX573MTC 74LCX573MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

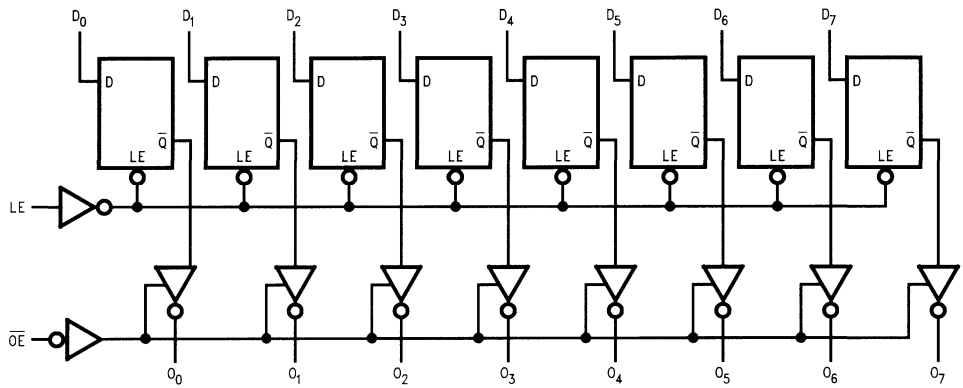
The 'LCX573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/12405–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V−3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V−2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX574
Low Voltage Octal D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The 'LCX574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

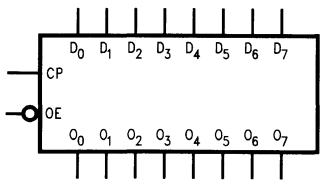
The 'LCX574 is functionally identical to the LCX374 except for the pinouts.

The 'LCX574 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 'LCX574 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

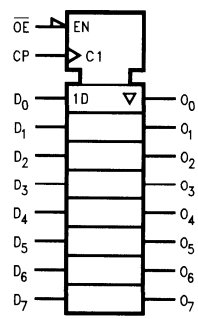
- 5V tolerant inputs and outputs
- 7.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 574
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12406–1

IEEE/IEC

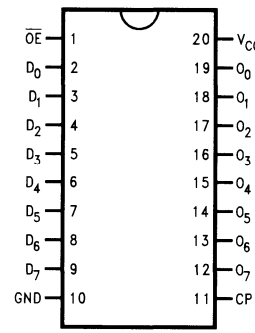


TL/F/12406–4

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE® Output Enable Input
O_0–O_7	TRI-STATE Outputs

Connection Diagrams

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12406–2

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX574WM 74LCX574WMX	74LCX574SJ 74LCX574SJX	74LCX574MSA 74LCX574MSAX	74LCX574MTC 74LCX574MTCX
See NS Package Number	M20A	M20D	MSA20	MTC20

Functional Description

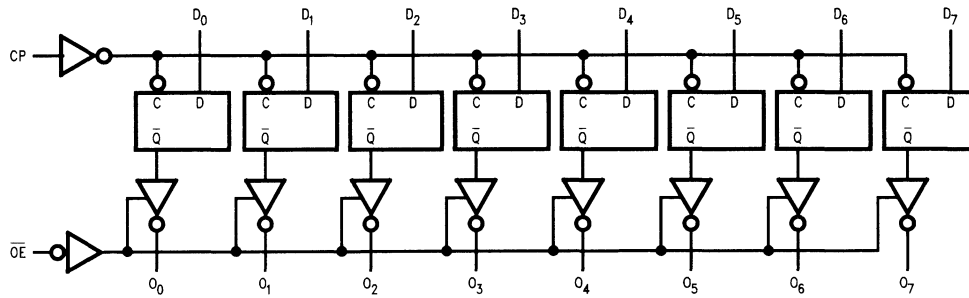
The 'LCX574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/12406–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V−3.6V V_{CC} = 2.7V		±24 ±12	mA
(T_A)	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX646
Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figure 1* through *Figure 4*.

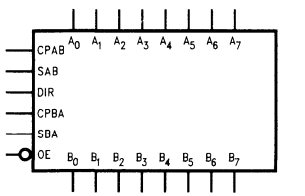
The LCX646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

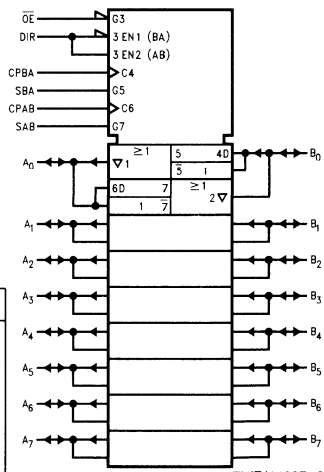
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±2.4 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/11997–1

IEEE/IEC

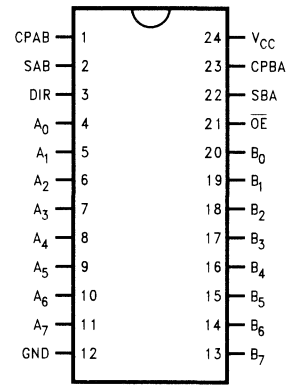


TL/F/11997–2

Pin Names	Description
A_0–A_7	Data Register A Inputs
	Data Register A Outputs
B_0–B_7	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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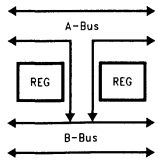
	SOIC JEDEC	SSOP Type II	TSSOP
Order Number	74LCX646WM 74LCX646WMX	74LCX646MSA 74LCX646MSAX	74LCX646MTC 74LCX646MTCX
See NS Package Number	M24B	MSA24	MTC24

Real Time Transfer A-Bus to B-Bus



TL/F/11997–4

FIGURE 1

Real Time Transfer B-Bus to A-Bus

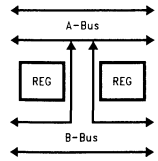


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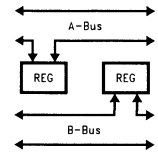
FIGURE 2

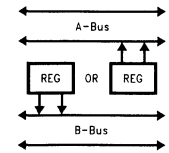
Storage from Bus to Register



TL/F/11997–6

FIGURE 3

Transfer from Register to Bus



TL/F/11997–7

FIGURE 4

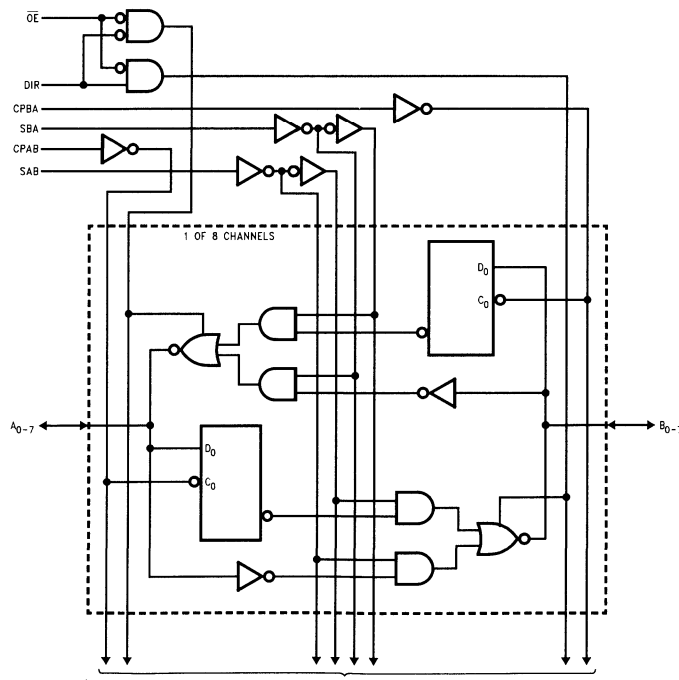
Function Table (Note)

Inputs						Data I/O		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

Note: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level ↑ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11997–8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

74LCX652
Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

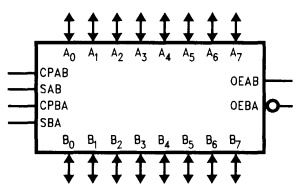
The LCX652 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 652
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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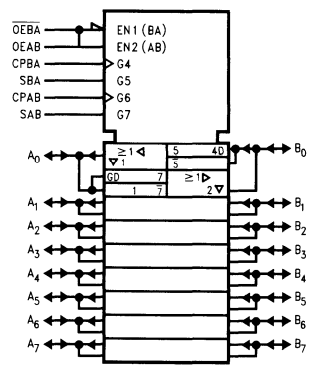
IEEE/IEC



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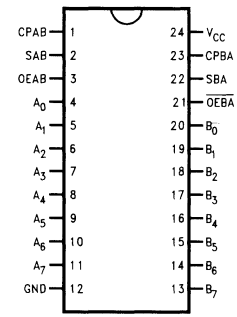
Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

	SOIC JEDEC	SSOP Type II	TSSOP JEDEC
Order Number	74LCX652WM 74LCX652WMX	74LCX652MSA 74LCX652MSAX	74LCX652MTC 74LCX652MTCX
See NS Package Number	M24B	MSA24	MTC24

Functional Description

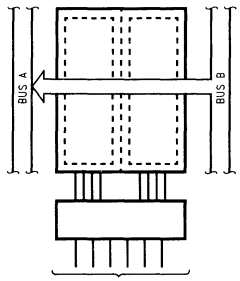
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Real-Time Transfer
Bus B to Bus A



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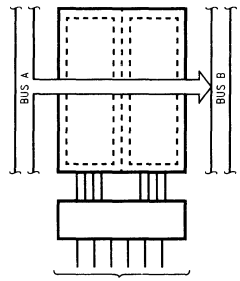
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B



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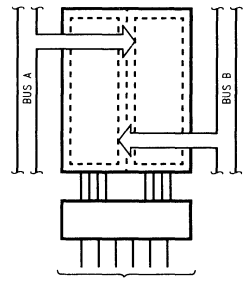
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Storage



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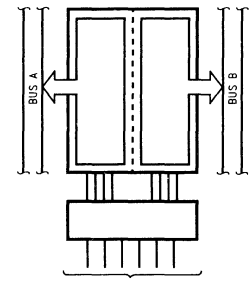
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Transfer Storage
Data to A or B



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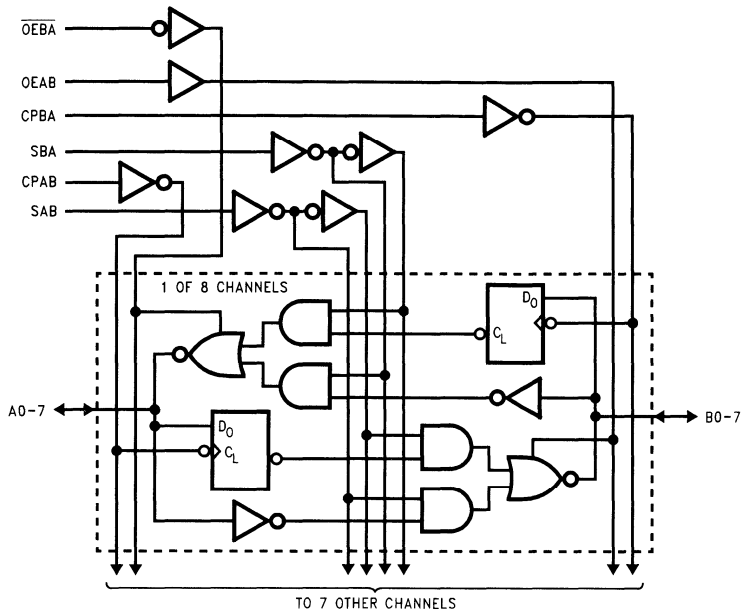
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX821
Low-Voltage 10-Bit D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

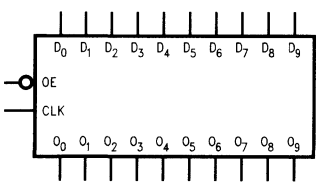
The LCX821 consists of ten D-type Flip-Flops with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 8.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 821
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



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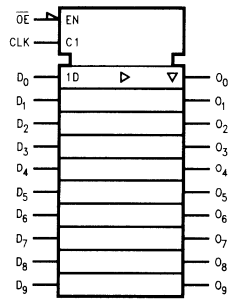
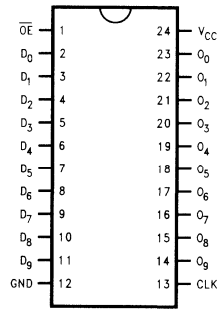
IEEE/IEC



TL/F/12635–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12635–3

Pin Names	Description
D_0–D_9	Data Inputs
CLK	Clock Input
$\overline{OE}$	Output Enable Input
O_0–O_9	TRI-STATE Latch Outputs

	SOIC JEDEC	SSOP Type II	TSSOP JEDEC
Order Number	74LCX821WM 74LCX821WMX	74LCX821MSA 74LCX821MSAX	74LCX821MTC 74LCX821MTCX
See NS Package Number	M24B	MSA24	MTC24

Functional Description

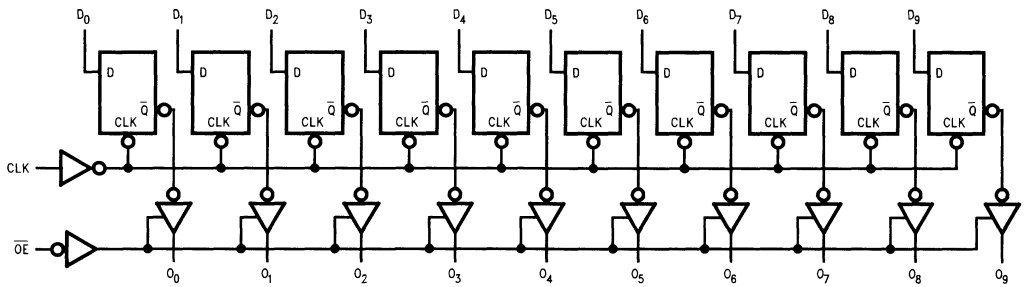
The 'LCX821 consists of ten edge-triggered flip-flops with individual D-type inputs with TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The ten flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the ten flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CLK	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impendance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/12635–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 1)	Min	Max Note 1	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CLK to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns
t_S	Setup Time, D_n to CLK	2.5		2.5		ns
t_H	Hold Time, D_n to CLK	1.5		1.5		ns
t_W	CLK Pulse Width	3.3		3.3		ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX841
Low-Voltage 10-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

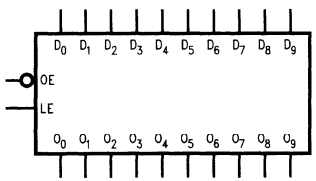
The LCX841 consists of ten latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

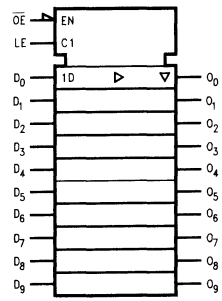
- 5V tolerant inputs and outputs
- 8.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 841
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/12575–1

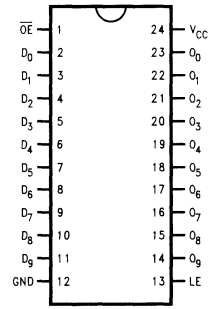
IEEE/IEC



TL/F/12575–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12575–3

Pin Names	Description
D_0–D_9	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_9	TRI-STATE Latch Outputs

	SOIC JEDEC	SSOP Type II	TSSOP JEDEC
Order Number	74LCX841WM 74LCX841WMX	74LCX841MSA 74LCX841MSAX	74LCX841MTC 74LCX841MTCX
See NS Package Number	M24B	MSA24	MTC24

Functional Description

The LCX841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

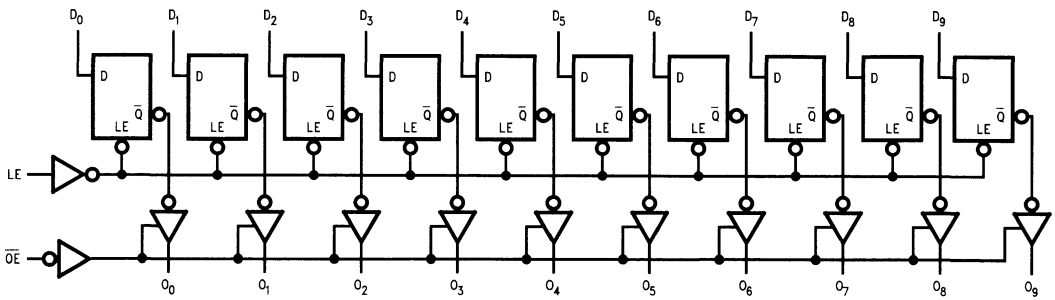
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impendance
NC = No Change

Logic Diagram



TL/F/12575–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 1)	Min	Max Note 1	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

National Semiconductor

ADVANCE INFORMATION

74LCX2952
Low-Voltage Octal Registered Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register.

The LCX2952 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX2952 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

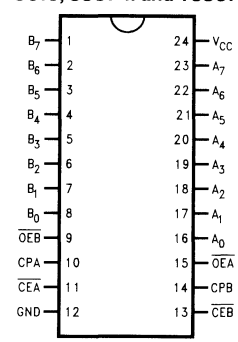
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 2952
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Connection Diagrams

Pin Assignment for SOIC, SSOP II and TSSOP



TL/F/12650–1

	SOIC JEDEC	SSOP Type II	TSSOP
Order Number	74LCX2952WM 74LCX2952WMX	74LCX2952MSA 74LCX2952MSAX	74LCX2952MTC 74LCX2952MTCX
See NS Package Number	M24B	MSA24	MTC24

Pin Descriptions (Continued)

Output Control

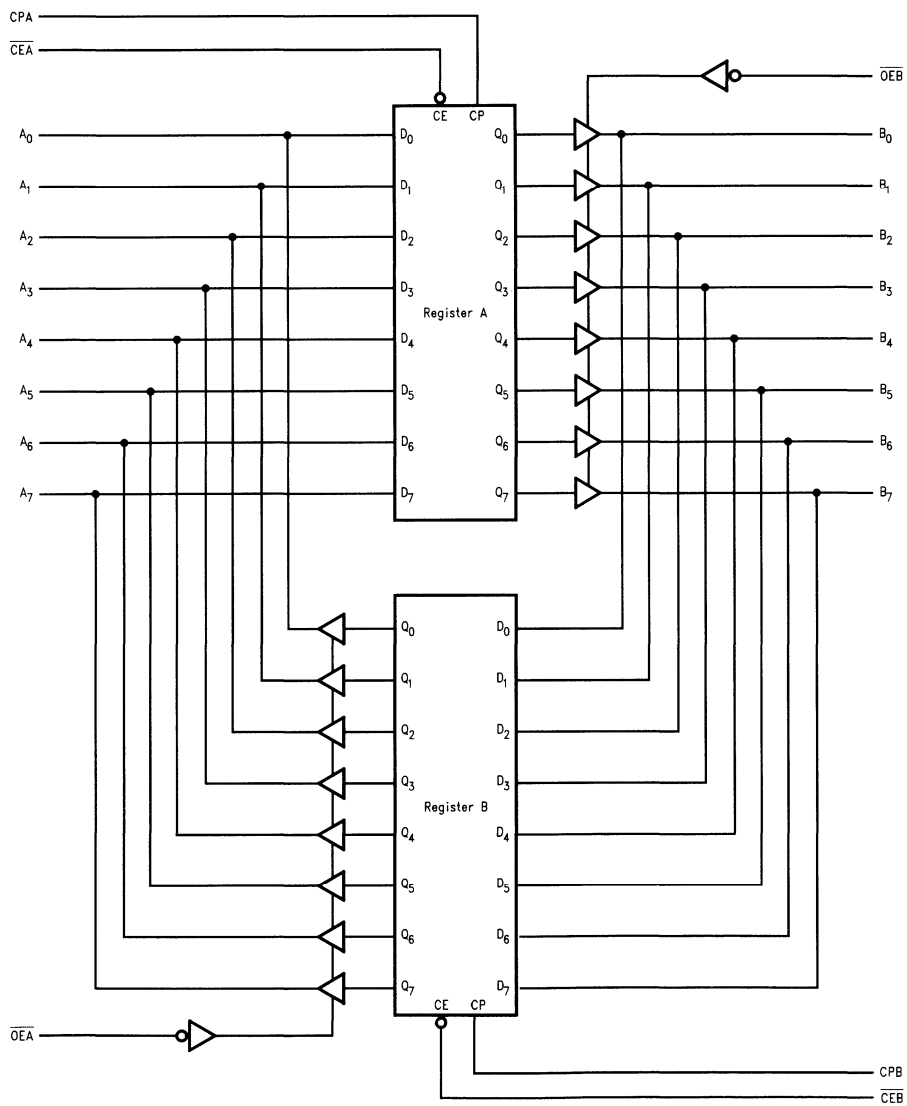
$\overline{OE}$	Internal Q	Output LCX2952	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

Block Diagram



TL/F/12650–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

National Semiconductor

74LCX16240
Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

General Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

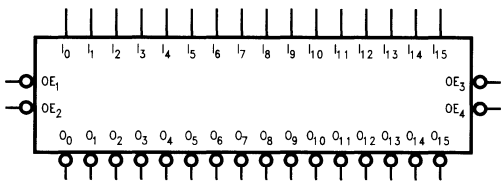
The LCX16240 is designed for low voltage (3.3V) V_{CC} applications with capacity of interfacing to a 5V signal environment.

The LCX16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 4.5 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2500V
  Machine model > 200V

Logic Symbol



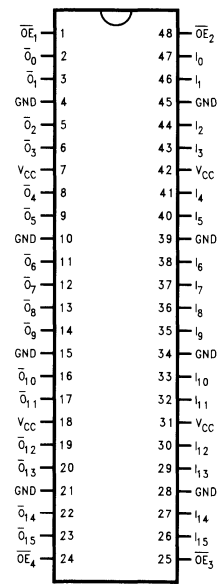
TL/F/11999–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	Outputs

	SSOP	TSSOP
Order Number	74LCX16240MEA 74LCX16240MEAX	74LCX16240MTD 74LCX16240MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

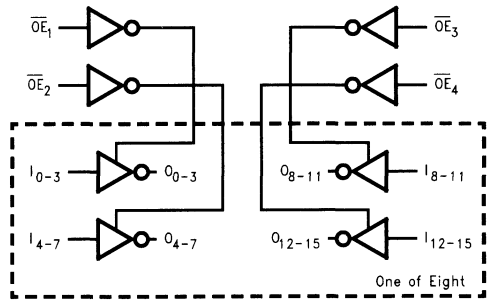


TL/F/11999–2

Functional Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/11999–3

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	4.5 4.5	1.5 1.5	5.3 5.3	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.4 5.4	1.5 1.5	6.0 6.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.3 5.3	1.5 1.5	5.4 5.4	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagaton delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

74LCX16244
Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

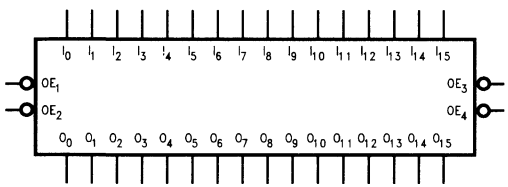
The LCX16244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 4.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



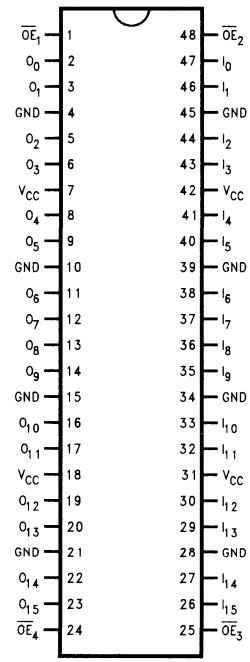
TL/F/12000–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16244MEA 74LCX16244MEAX	74LCX16244MTD 74LCX16244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12000–2

Functional Description

The LCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

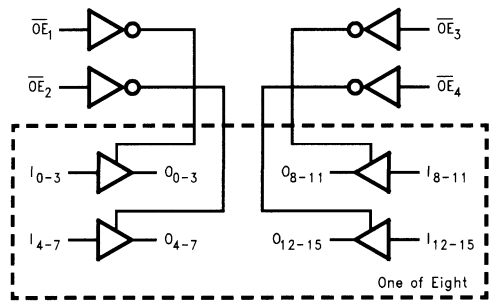
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12000–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.5 5.5	1.5 1.5	6.3 6.3	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.4 5.4	1.5 1.5	5.7 5.7	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

74LCX16245
Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

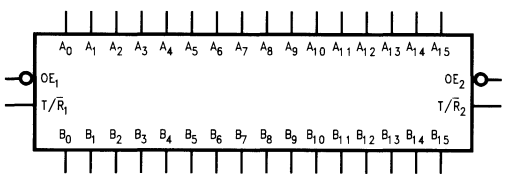
The 74LCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 4.5 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



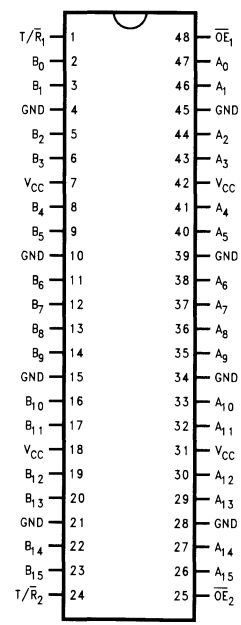
TL/F/12001–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or TRI-STATE Outputs
B_0–B_{15}	Side B Inputs or TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LCX16245MEA 74LCX16245MEAX	74LCX16245MTD 74LCX16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12001–2

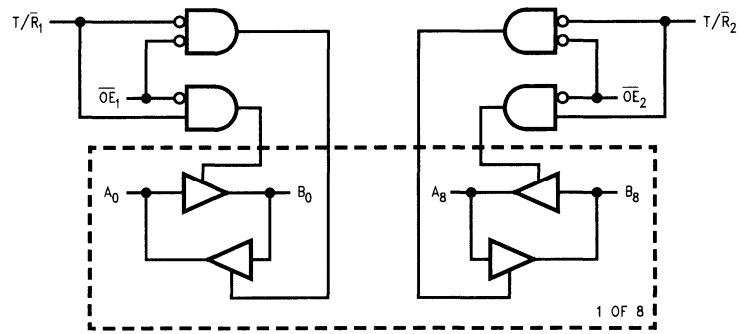
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12001–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.4 6.4	1.5 1.5	6.9 6.9	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

74LCX16373
Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

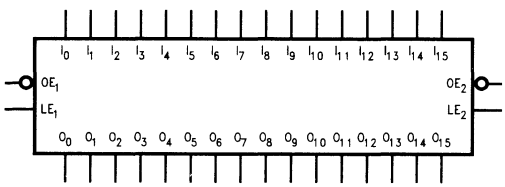
The LCX16373 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.4 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



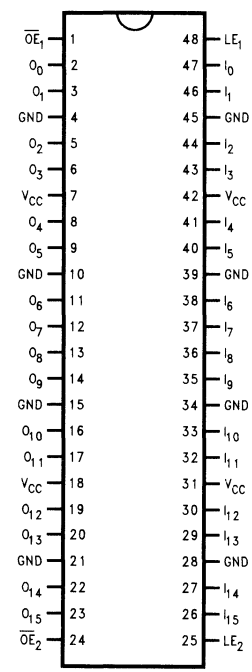
TL/F/12002–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16373MEA 74LCX16373MEAX	74LCX16373MTD 74LCX16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12002–2

Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

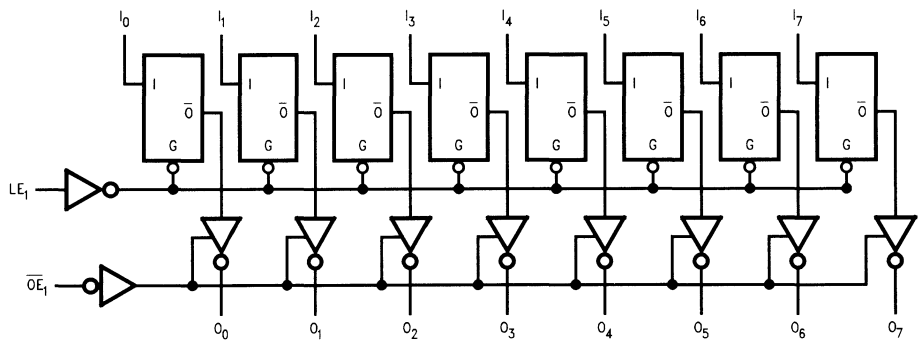
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

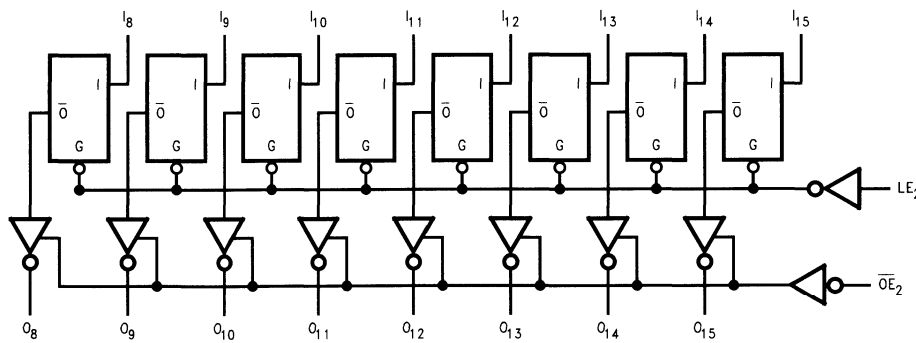
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



TL/F/12002–3



TL/F/12002–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	5.4 5.4	1.5 1.5	5.9 5.9	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.4 6.4	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.1 6.1	1.5 1.5	6.5 6.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.3 6.3	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

74LCX16374
Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (CE) are common to each byte and can be shorted together for full 16-bit operation.

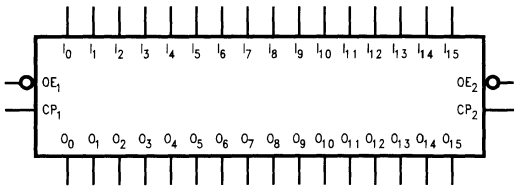
The LCX16374 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 6.2 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



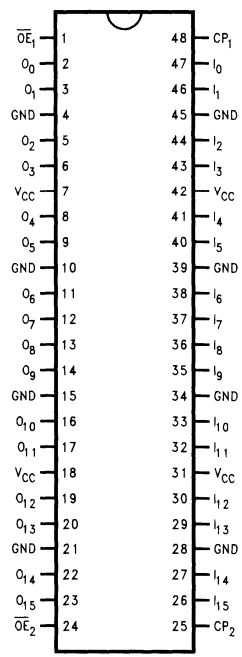
TL/F/12003–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16374MEA 74LCX16374MEAX	74LCX16374MTD 74LCX16374MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12003–2

Functional Description

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

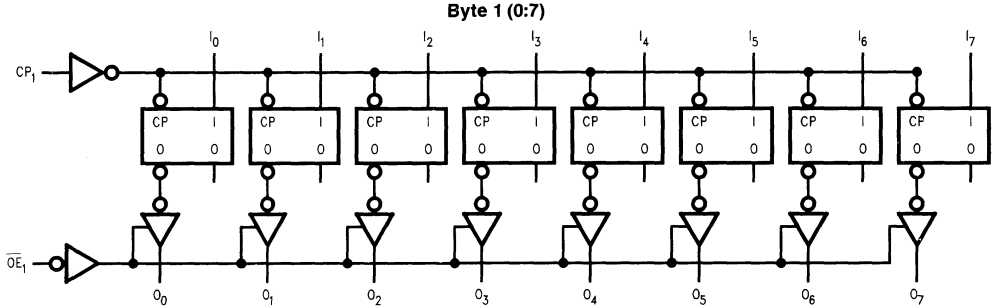
Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW of CP

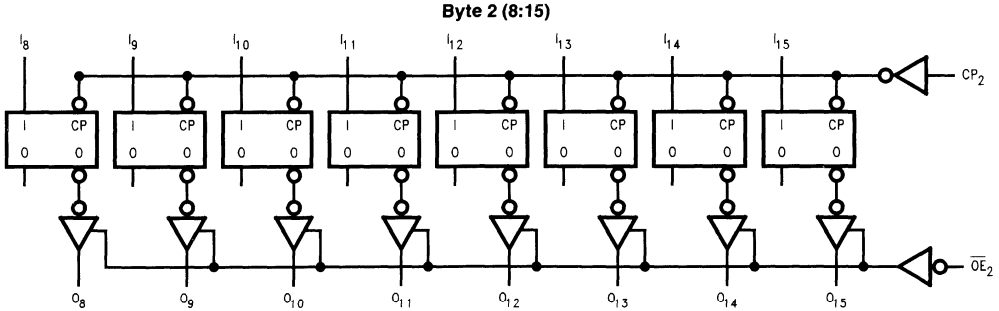
Logic Diagrams

Byte 1 (0:7)



TL/F/12003–3

Byte 2 (8:15)



TL/F/12003–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	6.2 6.2	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.1 6.1	1.5 1.5	6.3 6.3	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.2 6.2	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two seperate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16500
Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

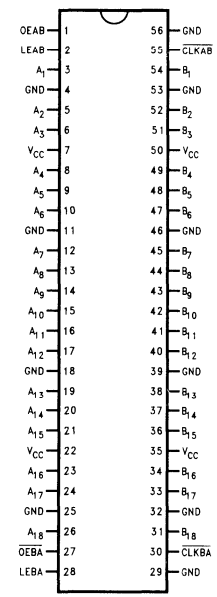
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- 6.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16500
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12407–1

	SSOP	TSSOP
Order Number	74LCX16500MEA 74LCX16500MEAX	74LCX16500MTD 74LCX16500MTDX
See NS Package Number	MS56A	MTD56

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Function Table†

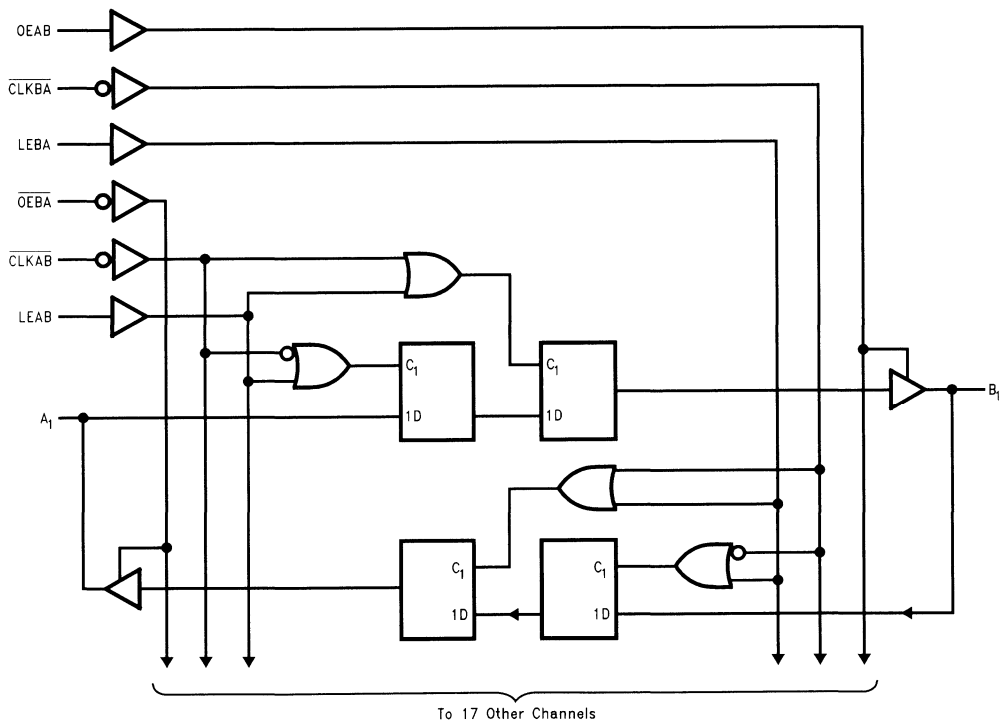
Inputs				Output
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

Logic Diagram



TL/F/12407–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 3)	Min	Max (Note 3)	
f_{max}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 4)		1.0 1.0			ns

Note 3: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16501
18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

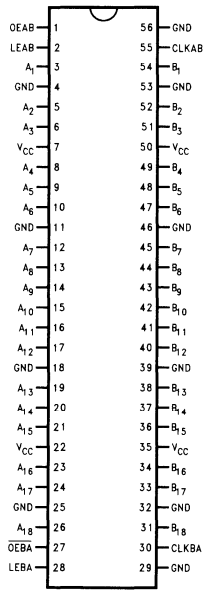
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- 6.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- $\pm$24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16501
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12550–1

Function Table†

Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

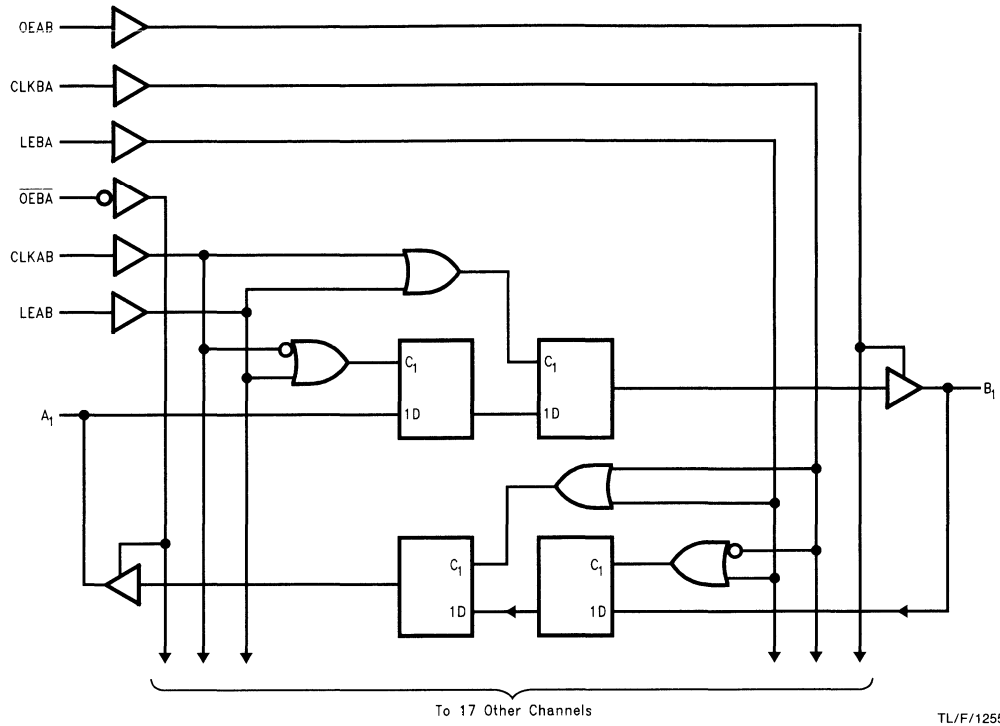
†A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

‡Output level before the indicated steady-state input conditions were established.

§Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Logic Diagram



TL/F/12550–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 3)	Min	Max (Note 3)	
f_{max}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

74LCX16543
Low-Voltage 16-Bit Registered Transceiver with 5V-Tolerant Inputs and Outputs

General Description

The LCX16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

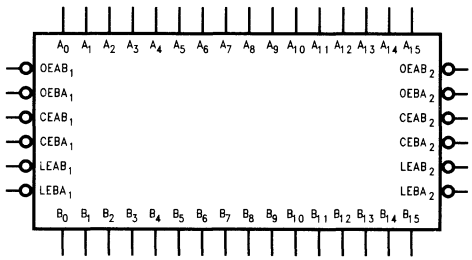
The LCX16543 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16543 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.2 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16543
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbol



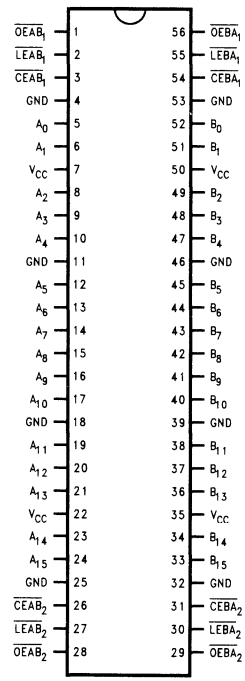
TL/F/12464–1

Pin Names	Description
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LCX16543MEA 74LCX16543MEAX	74LCX16543MTD 74LCX16543MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12464–2

Functional Description

The 'LCX16543 contains sixteen non-inverting transceivers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}_n$) input must be LOW in order to enter data from A_0–A_{15} or take data from B_0–B_{15}, as indicated in the Data I/O Control Table. With $\overline{CEAB}_n$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}_n$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}_n$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}_n$ and $\overline{OEAB}_n$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$ inputs.

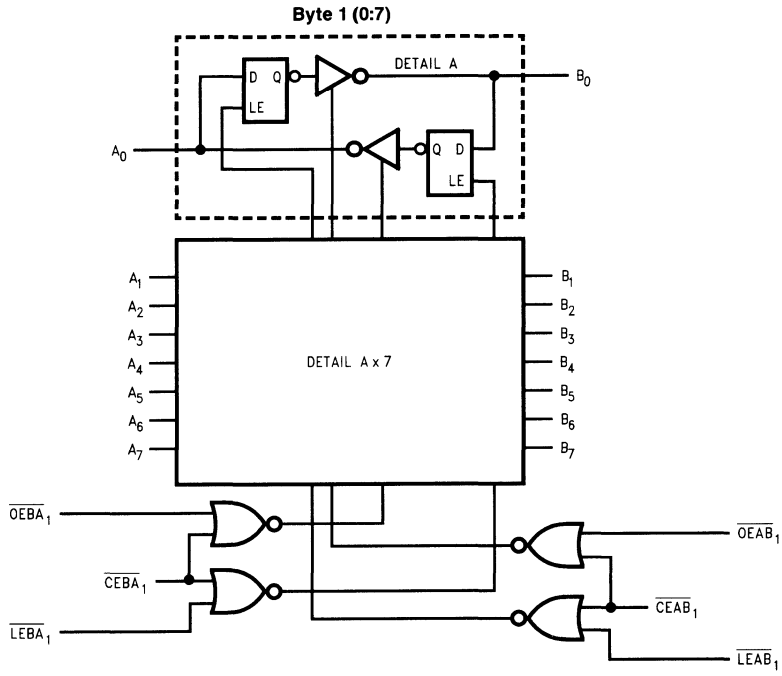
Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

Logic Diagrams

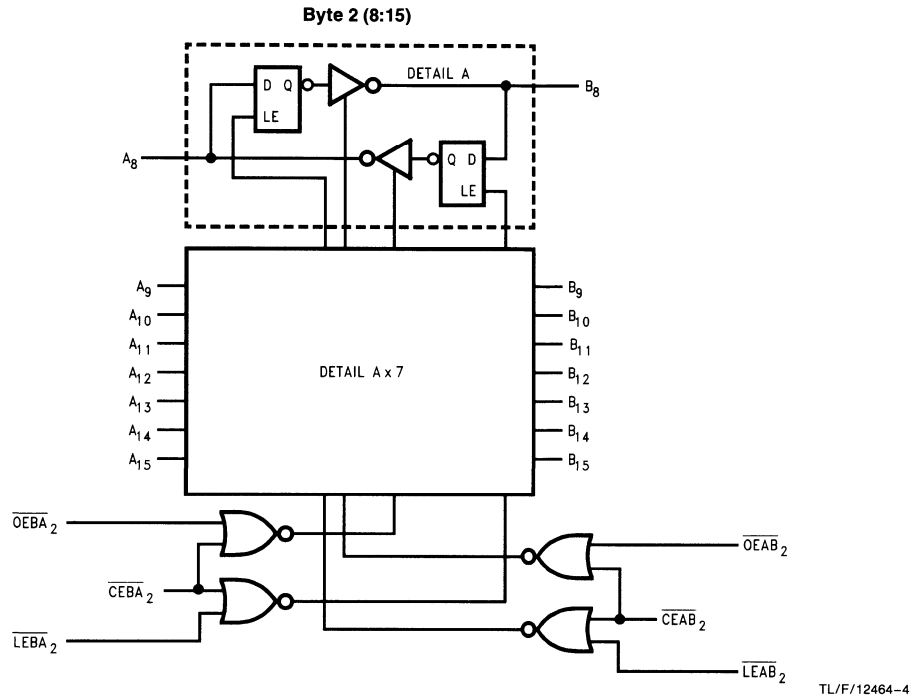
Byte 1 (0:7)



TL/F/12464–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay $\overline{LEBA}_n$ to A_n or $\overline{LEAB}_n$ to B_n	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	 1.5 1.5	 6.5 6.5	 1.5 1.5	 7.0 7.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	 1.5 1.5	 6.5 6.5	 1.5 1.5	 7.0 7.0	ns
t_S	Setup Time, HIGH or LOW, Data to $\overline{LExx}_n$	2.5		2.5		ns
t_H	Hold Time, HIGH or LOW, Data to $\overline{LExx}_n$	1.5		1.5		ns
t_W	Pulse Width, Latch Enable, LOW	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3)		1.0 1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16646
Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16646 contains sixteen non-inverting bidirectional registered bus transceivers with TRI-STATE® outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The four fundamental handling functions available are illustrated in *Figure 1* thru *Figure 4*.

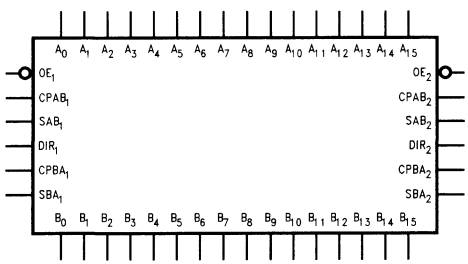
The LCX16646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbol

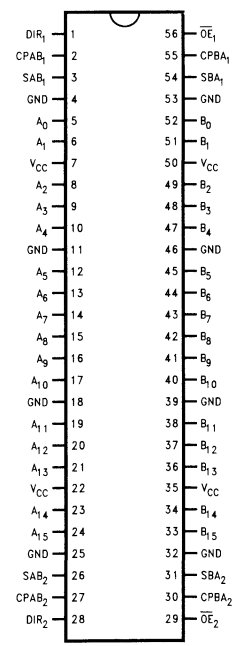


TL/F/12004–1

	SSOP	TSSOP
Order Number	74LCX16646MEA 74LCX16646MEAX	74LCX16646MTD 74LCX16646MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

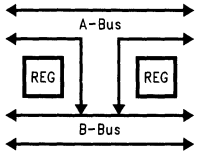
Pin Assignment for SSOP and TSSOP



TL/F/12004–2

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

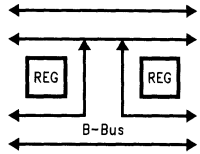
Real Time Transfer A-Bus to B-Bus



TL/F/12004–3

FIGURE 1

Real Time Transfer B-Bus to A-Bus



TL/F/12004–4

FIGURE 2

Storage from Bus to Register

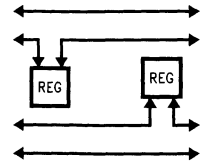


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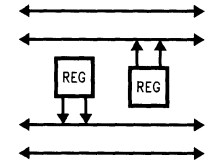
FIGURE 3

Transfer from Register to Bus



TL/F/12004–6

FIGURE 4

Function Table (Note)

Inputs						Data I/O		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock An Data into A Register
H	X	X	↑	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↑	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↑	X	H			Clock Bn into B Register and Output to An

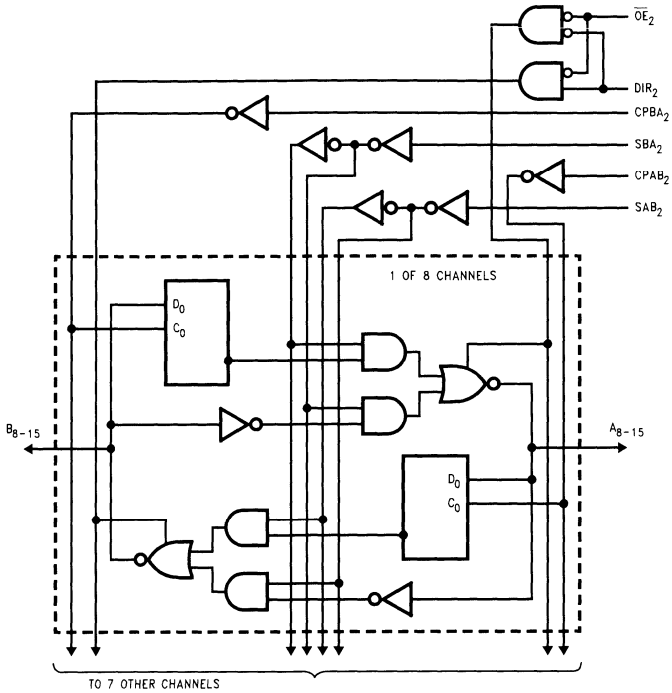
Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial

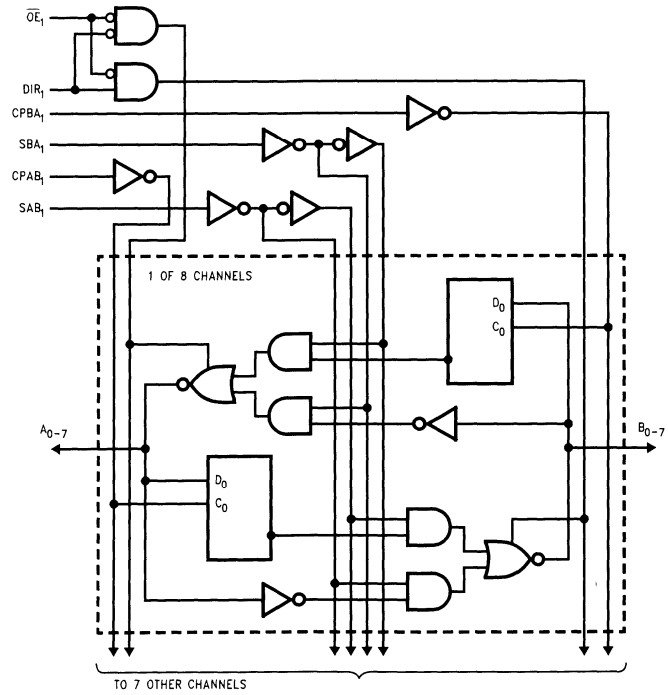
L = LOW Voltage Level ↑ = LOW-to-HIGH Transition.

4

Logic Diagrams



TL/F/12004–7



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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170				ns
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16652
Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16652 contains sixteen non-inverting bidirectional bus transceivers with TRI-STATE® outputs providing multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

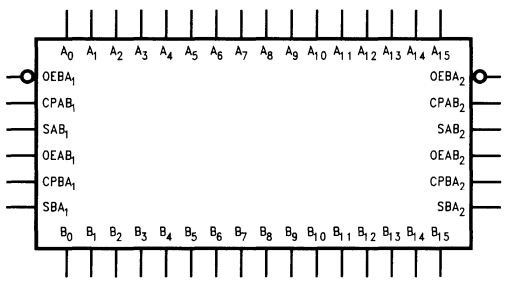
The LCX16652 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16652
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

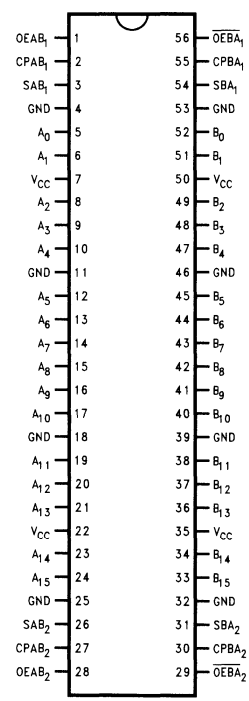


TL/F/12005–1

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_{15}	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12005–2

	SSOP	TSSOP
Order Number	74LCX16652MEA 74LCX16652MEAX	74LCX16652MTD 74LCX16652MTDX
See NS Package Number	MS56A	MTD56

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 74LCX16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

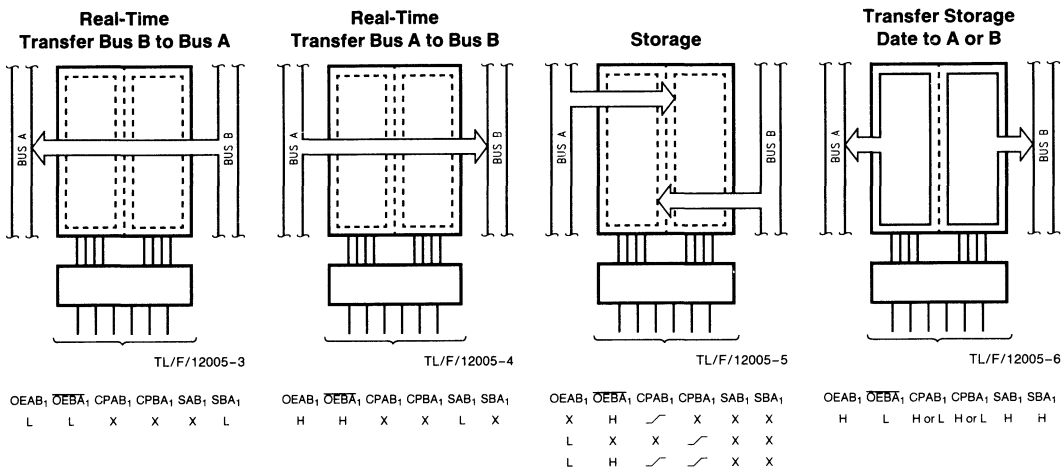


FIGURE 1

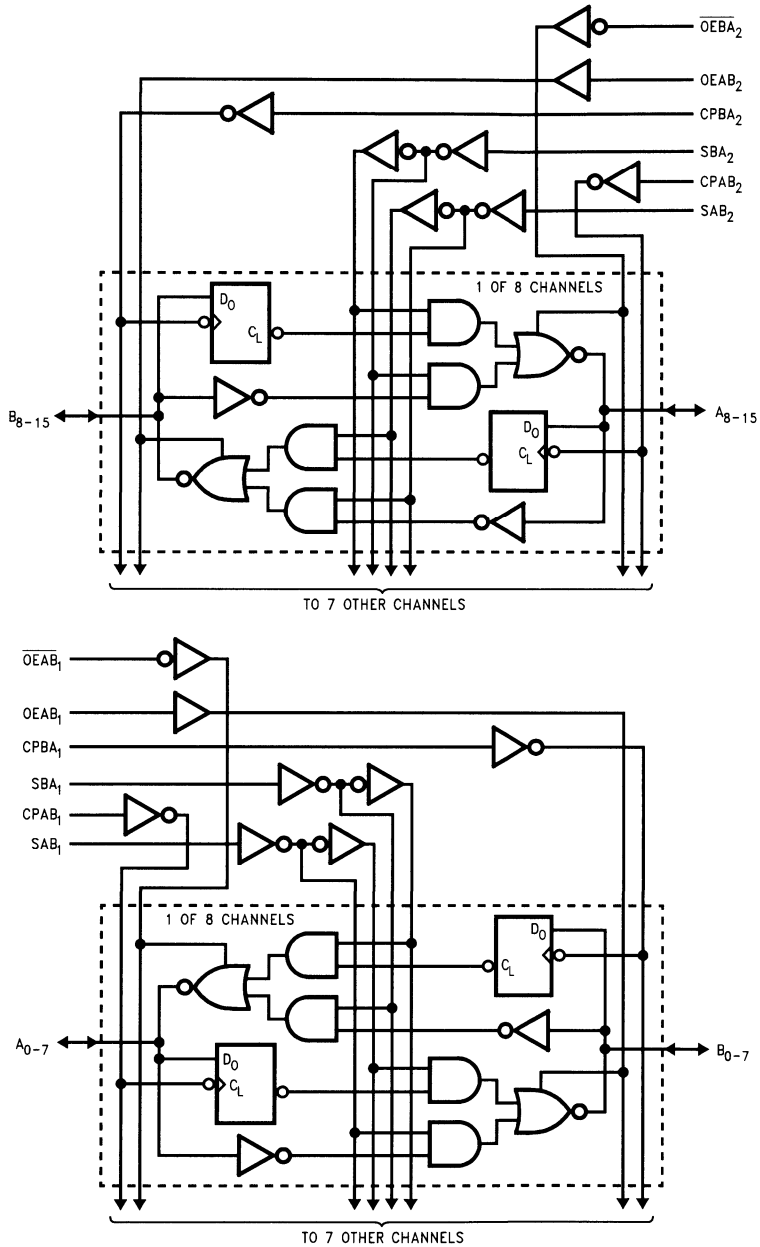
Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Not Specified	State A, Hold B
H	H	⌐	⌐	X	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Not Specified	Input	Hold A, Store B
L	L	⌐	⌐	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

Logic Diagram



TL/F/12005–7

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	5.7 5.7	1.5 1.5	6.2 6.2	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.2 6.2	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16821
Low-Voltage 20-Bit D-Type Flip-Flops with 5V Tolerant Inputs and Outputs

General Description

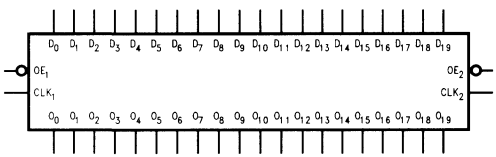
The LCX16821 contains twenty non-inverting D-type Flip-Flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 6.2 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16821
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



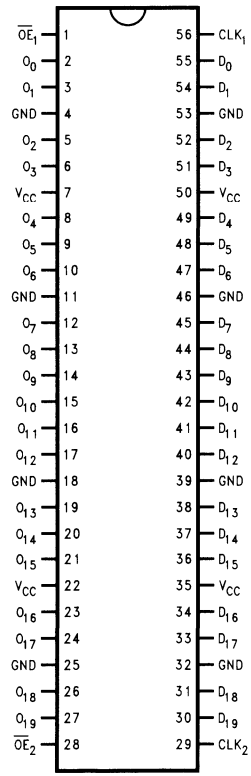
TL/F/12634–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
CLK_n	Clock Input
D_0–D_{19}	Inputs
O_0–O_{19}	Outputs

	SSOP	TSSOP
Order Number	74LCX16821MEA 74LCX16821MEAX	74LCX16821MTD 74LCX16821MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12634–2

Functional Description

The LCX16821 contains twenty D-type flip-flops with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the flip-flops.

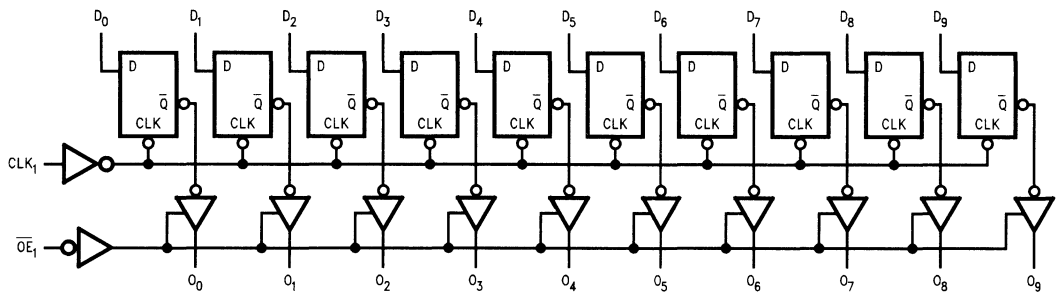
Truth Tables

Inputs			Outputs
CLK_1	$\overline{OE}_1$	D_0–D_9	O_0–O_9
X	H	X	Z
↗	L	L	L
↗	L	H	H
L or H	L	X	O_0

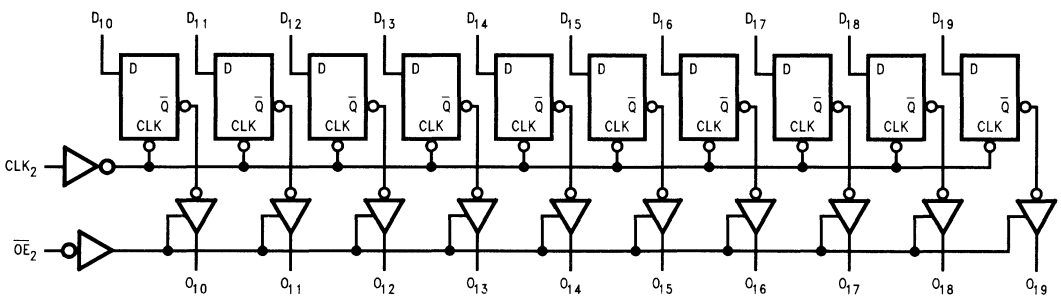
Inputs			Outputs
CLK_2	$\overline{OE}_2$	D_{10}–D_{19}	O_{10}–O_{19}
X	H	X	Z
↗	L	L	L
↗	L	H	H
L or H	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before LOW to HIGH transition of Clock
↗ = LOW-to-HIGH transition

Logic Diagrams



TL/F/12634–3



TL/F/12634–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 1)	Min	Max (Note 1)	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CLK to O_n	1.5 1.5	6.2 6.2	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns
t_S	Setup Time, D_n to CLK	2.5		2.5		ns
t_H	Hold Time, D_n to CLK	1.5		1.5		ns
t_W	CLK Pulse Width	3.3		3.3		ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX16841
Low-Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16841 contains twenty non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

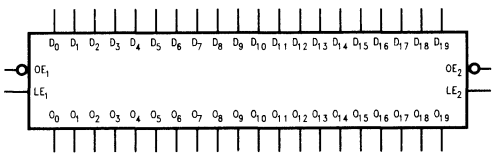
The LCX16841 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.5 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16841
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



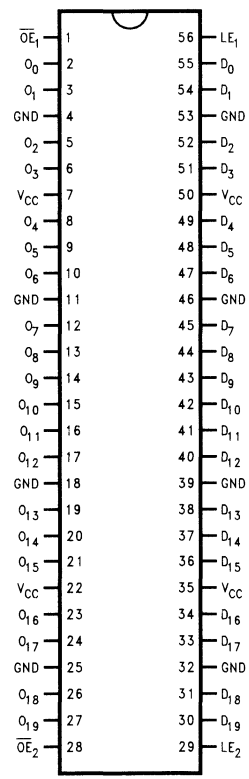
TL/F/12578–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
D_0–D_{19}	Inputs
O_0–O_{19}	Outputs

	SSOP	TSSOP
Order Number	74LCX16841MEA 74LCX16841MEAX	74LCX16841MTD 74LCX16841MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12578–2

Functional Description

The LCX16841 contains twenty D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

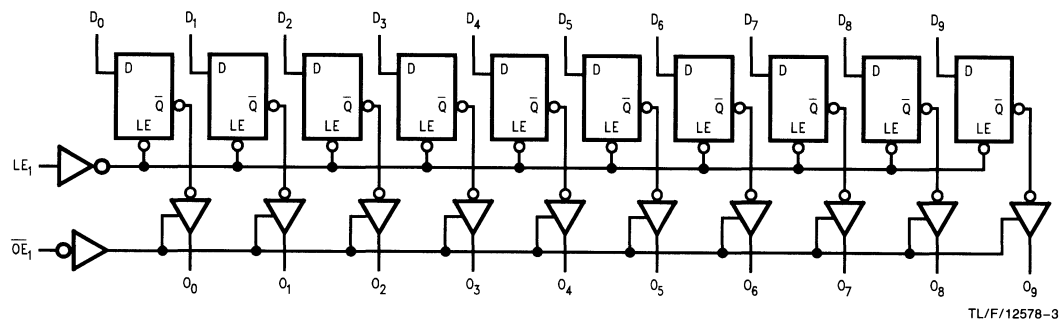
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	D_0–D_9	O_0–O_9
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

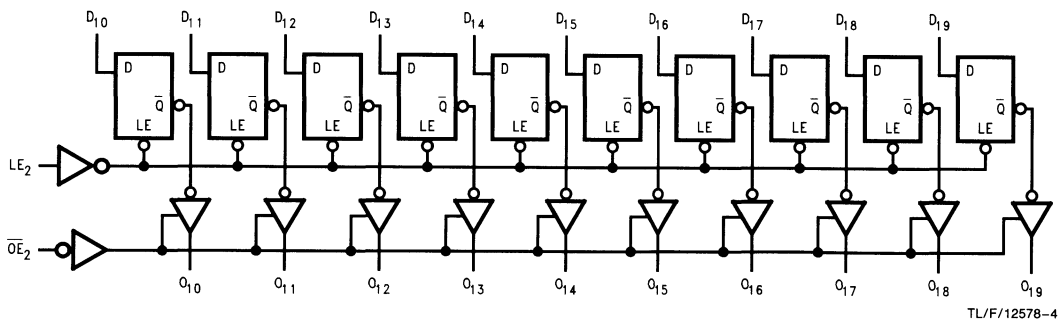
Inputs			Outputs
LE_2	$\overline{OE}_2$	D_{10}–D_{19}	O_{10}–O_{19}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



TL/F/12578–3



TL/F/12578–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 1)	Min	Max (Note 1)	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

PRELIMINARY

74LCX162841
Low-Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX162841 contains twenty non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state. The 30Ω-series resistor helps reducing output overshoot and undershoot.

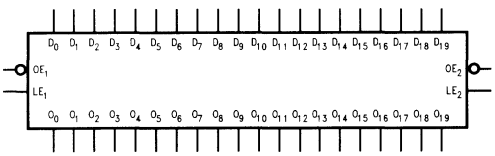
The LCX162841 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX162841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 30Ω-series resistor on outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 162841
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



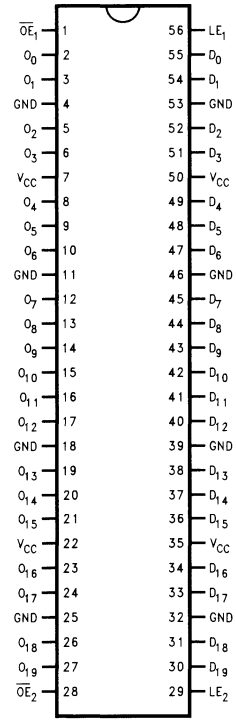
TL/F/12632–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
D_0–D_{19}	Inputs
O_0–O_{19}	Outputs

	SSOP	TSSOP
Order Number	74LCX162841MEA 74LCX162841MEAX	74LCX162841MTD 74LCX162841MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12632–2

Functional Description

The LCX162841 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

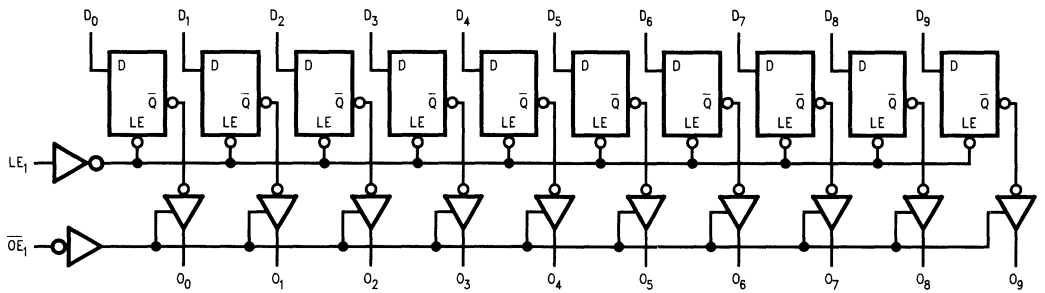
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	D_0–D_9	O_0–O_9
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

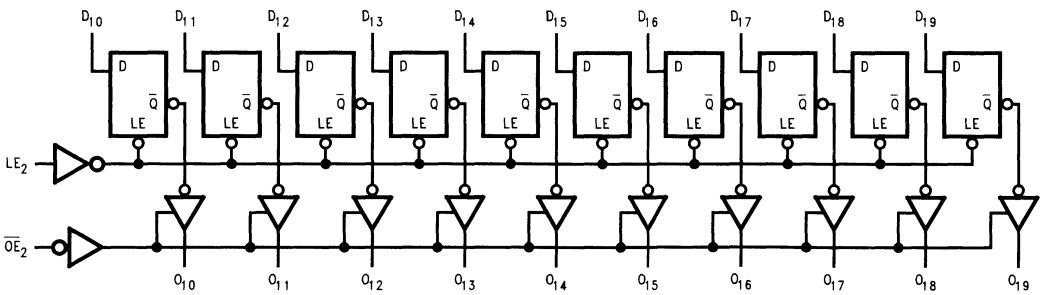
Inputs			Outputs
LE_2	$\overline{OE}_2$	D_{10}–D_{19}	O_{10}–O_{19}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



TL/F/12632–3



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±12 ±6	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −12 mA	3.0	2.0		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 12 mA	3.0		0.8	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

Section 5

LVX Translator Family

Section 5 Contents

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National Semiconductor

LVX Translator Family
Low Voltage Dual Supply CMOS Translating Transceivers

Features	Advantages
Dual supplies, converts 3V signal swing to 5V signal swing and vice-versa	Interfaces to 5V non-TTL compatible full CMOS swing devices and buses pulled up to 5V
Dynamically configurable V_{CCB} to 3V or 5V (LVXC versions)	Talks to 3V and 5V modules
Floating B-port and V_{CCB} (LVXC versions)	Allows modules to be inserted and removed freely
'245 style pinout	Easy migration to pure 3V '245 function without board re-layout
High speed (7.0 ns max t_{PD} for LVXC4245)	High speed bus interface
Very low static (50 μA max I_{CCQ}) and dynamic power	Saves power, extends battery life
Extended 2.7V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Balanced $\pm$24 mA output drive	Drives transmission lines down to 50Ω
Patented Quiet Series™ noise reduction circuitry	Low ground bounce, overshoot, undershoot, and EMI
SOIC, QSOP, and TSSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

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74LVX3245
8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

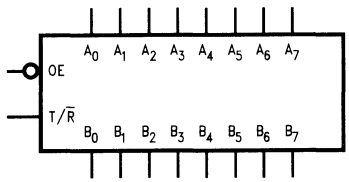
The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

Features

- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

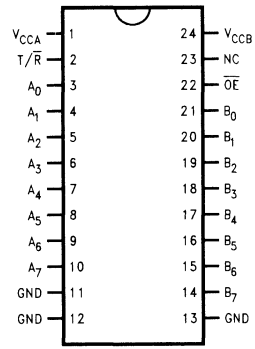
Logic Symbol



TL/F/11620–1

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/11620–2

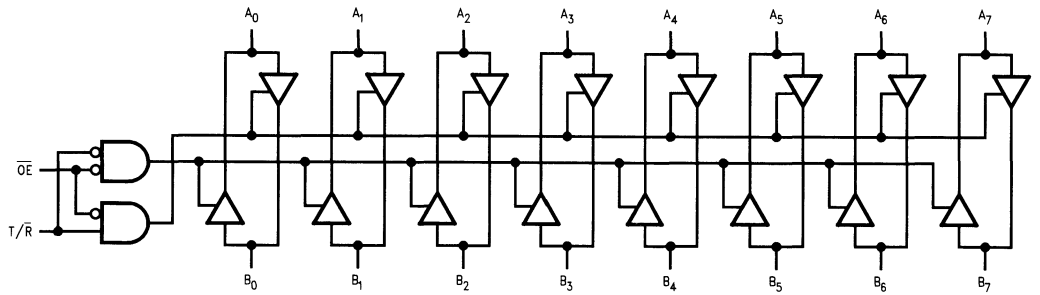
Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3245WM 74LVX3245WMX	74LVX3245QSC 74LVX3245QSCX	74LVX3245MTC 74LVX3245MTCX
See NS Package Number	M24B	MQA24	MTC24

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



T/F/11620–4

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCB} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A(n)	−0.5V to V_{CCA} + 0.5V
@ B(n)	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±100 mA
@ I_{CCB}	±200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions

Supply Voltage	
V_{CCA}	2.7V to 3.6V
V_{CCB}	4.5V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCB}
Input/Output Voltage ($V_{I/O}$)	
@ A(n)	0V to V_{CCA}
@ B(n)	0V to V_{CCB}
Free Air Operating Temperature (T_A)	
74LVX	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVX3245 T_A = +25°C	74LVX3245 T_A = −40°C to +85°C		Units	Conditions
					Typ	Guaranteed Limits			
V_{IHA}	Minimum High Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.0		2.0	2.0	V	$V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ − 0.1V
			2.7	5.0		2.0	2.0		
V_{IHB}		B(n)	3.3	4.5		2.0	2.0		
			3.3	5.5		2.0	2.0		
V_{ILA}	Maximum Low Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.0		0.8	0.8	V	$V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ −0.1V
			2.7	5.0		0.8	0.8		
V_{ILB}		B(n)	3.3	4.5		0.8	0.8		
			3.3	5.5		0.8	0.8		
V_{OHA}	Minimum High Level Output Voltage		3.0	4.5	2.99	2.9	2.9	V	I_{OUT} = −100 μA
			3.0	4.5	2.65	2.35	2.25		I_{OH} = −24 mA
			2.7	4.5	2.5	2.3	2.2		I_{OH} = −12 mA
			2.7	4.5	2.3	2.1	2.0		I_{OH} = −24 mA
V_{OHB}			3.0	4.5	4.5	4.4	4.4	V	I_{OUT} = −100 μA
			3.0	4.5	4.25	3.86	3.76		I_{OH} = −24 mA
V_{OLA}	Maximum Low Level Output Voltage		3.0	4.5	0.002	0.1	0.1	V	I_{OUT} = 100 μA
			3.0	4.5	0.21	0.36	0.44		I_{OL} = 24 mA
			2.7	4.5	0.11	0.36	0.44		I_{OL} = 12 mA
			2.7	4.5	0.22	0.42	0.5		I_{OL} = 24 mA
V_{OLB}			3.0	4.5	0.002	0.1	0.1	V	I_{OUT} = 100 μA
			3.0	4.5	0.18	0.36	0.44		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		3.6	5.5		±0.1	±1.0	μA	$V_I = V_{CCB}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A(n)		3.6	5.5		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVX3245 $T_A = +25°C$	74LVX3245 $T_A = -40°C$ to $+85°C$		Units	Conditions
					Typ	Guaranteed Limits			
I_{OZB}	Maximum TRI-STATE Output Leakage @ B(n)		3.6	5.5		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CCT}/Input @	B(n)	3.6	5.5	1.0	1.35	1.5	mA	$V_I = V_{CCB} - 2.1V$
		A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.5		0.35	0.5	mA	$V_I = V_{CCA} - 0.6V$
I_{CCA}	Quiescent V_{CCA} Supply Current		3.6	5.5		5	50	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6	5.5		8	80	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CCA}
V_{OLPA} V_{OLPB}	Quiet Output Maximum Dynamic V_{OL}		3.3 3.3	5.0 5.0		0.8 1.5		V	(Notes 1, 2)
V_{OLVA} V_{OLVB}	Quiet Output Minimum Dynamic V_{OL}		3.3 3.3	5.0 5.0		−0.8 −1.2		V	(Notes 1, 2)
V_{IHDA} V_{IHDB}	Minimum High Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		2.0 2.0		V	(Notes 1, 3)
V_{ILDA} V_{ILDB}	Maximum Low Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		0.8 0.8		V	(Notes 1, 3)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n−1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameters	74LVX3245 $T_A = +25°C$, $C_L = 50$ pF, **$V_{CCA} = 3.3V$, *$V_{CCB} = 5.0V$			74LVX3245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, **$V_{CCA} = 3.3V$, *$V_{CCB} = 5.0V$		74LVX3245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V$, *$V_{CCB} = 5.0V$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
t_{PLH}	A to B	1.0	5.6	7.5	1.0	8.0	1.0	8.5	
t_{PHL}	Propagation Delay	1.0	5.1	7.5	1.0	8.0	1.0	8.5	ns
t_{PLH}	B to A	1.0	5.7	7.5	1.0	8.0	1.0	8.5	
t_{PZL}	Output Enable	1.0	4.8	8.0	1.0	8.5	1.0	9.0	ns
t_{PZH}	Time $\overline{OE}$ to B	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
t_{PZL}	Output Enable	1.0	6.3	8.5	1.0	9.0	1.0	9.5	ns
t_{PZH}	Time $\overline{OE}$ to A	1.0	6.8	9.0	1.0	9.5	1.0	10.0	
t_{PHZ}	Output Disable	1.0	5.3	7.5	1.0	8.0	1.0	8.5	ns
t_{PLZ}	Time $\overline{OE}$ to B	1.0	4.2	7.0	1.0	7.5	1.0	8.0	
t_{PHZ}	Output Disable	1.0	5.3	8.0	1.0	8.5	1.0	9.0	ns
t_{PLZ}	Time $\overline{OE}$ to A	1.0	3.7	6.5	1.0	7.0	1.0	7.5	
t_{OSHL}	Output to Output								ns
t_{OSLH}	Skew***		1.0	1.5		1.5		1.5	
	Data to Output								

*Voltage Range 5.0V is 5.0V ±0.5V.
**Voltage Range 3.3V is 3.3V ±0.3V.

***Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

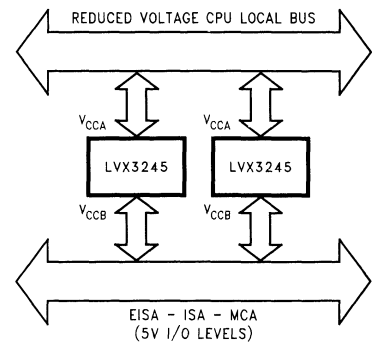
Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		15	pF	$V_{CCA} = 3.3V$, $V_{CCB} = 5.0V$
C_{PD}	Power Dissipation Capacitance	A → B	55	pF	$V_{CCB} = 5.0V$
		B → A	40		$V_{CCA} = 3.3V$

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



TL/F/11620–3

National Semiconductor

74LVX4245
8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

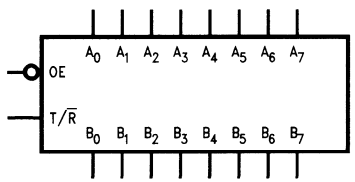
The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

Features

- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A port and 3V data flow at B port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements patented Quiet Series™ EMI reduction circuitry
- Functionally compatible with the 74 series 245

Logic Symbol

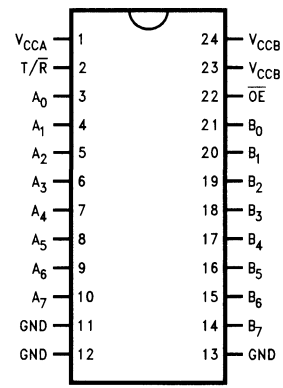


TL/F/11540–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/11540–2

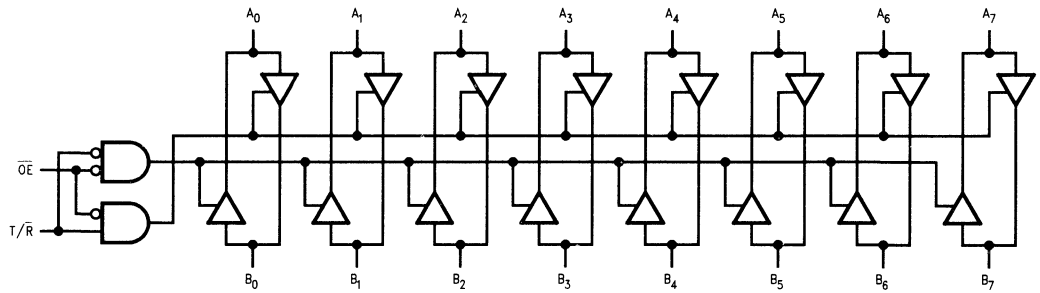
	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX4245WM 74LVX4245WMX	74LVX4245QSC 74LVX4245QSCX	74LVX4245MTC 74LVX4245MTCX
See NS Package Number	M24B	MQA24	MTC24

5

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



TL/F/11540–6

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A(n)	−0.5V to V_{CCA} + 0.5V
@ B(n)	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±200 mA
@ I_{CCB}	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage	
V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 3.6V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@ A(n)	0V to V_{CCA}
@ B(n)	0V to V_{CCB}
Free Air Operating Temperature (T_A)	
74LVX	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVX4245 T_A +25°C	74LVX4245 T_A = −40°C to +85°C		Units	Conditions
					Typ	Guaranteed Limits			
V_{IHA}	Minimum High Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.3		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			4.5	3.3		2.0	2.0		
V_{IHB}		B(n)	5.0	3.6		2.0	2.0		
			5.0	2.7		2.0	2.0		
V_{ILA}	Maximum Low Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.3		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			4.5	3.3		0.8	0.8		
V_{ILB}		B(n)	5.0	2.7		0.8	0.8		
			5.0	3.6		0.8	0.8		
V_{OHA}	Minimum High Level Output Voltage		4.5	3.0	4.5	4.4	4.4	V	$I_{OUT} = -100\ \mu A$
			4.5	3.0	4.25	3.86	3.76		$I_{OH} = -24$ mA
V_{OHB}			4.5	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100\ \mu A$
			4.5	3.0	2.8	2.4	2.4		$I_{OH} = -12$ mA
			4.5	2.7	2.5	2.4	2.4		$I_{OL} = -8$ mA
V_{OLA}	Maximum Low Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			4.5	3.0	0.18	0.36	0.44		$I_{OL} = 24$ mA
V_{OLB}			4.5	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			4.5	3.0	0.1	0.31	0.4		$I_{OL} = 12$ mA
			4.5	2.7	0.1	0.31	0.4		$I_{OL} = 8$ mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		5.5	3.6		±0.1	±1.0	μA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A(n)		5.5	3.6		±0.5	±5.0	μA	$V_I = V_{IL}$, V_{IH} $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	74LVX4245 $T_A = +25°C$ Typ	74LVX4245 $T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{OZB}	Maximum TRI-STATE Output Leakage @ B(n)	5.5	3.6		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CCT}/Input @ A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.6	1.0	1.35	1.5	mA	$V_I = V_{CCA} - 2.1V$
	Input @ B(n)	5.5	3.6		0.35	0.5	mA	$V_I = V_{CCB} - 0.6V$
I_{CCA}	Quiescent V_{CCA} Supply Current	5.5	3.6		8	80	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current	5.5	3.6		5	50	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = V_{CCA}
V_{OLPA} V_{OLPB}	Quiet Output Maximum Dynamic V_{OL}	5.0 5.0	3.3 3.3		1.5 0.8		V	(Notes 1, 2)
V_{OLVA} V_{OLVB}	Quiet Output Minimum Dynamic V_{OL}	5.0 5.0	3.3 3.3		−1.2 −0.8		V	(Notes 1, 2)
V_{IHDA} V_{IHDB}	Minimum High Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		2.0 2.0		V	(Notes 1, 3)
V_{ILDA} V_{ILDB}	Maximum Low Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		0.8 0.8		V	(Notes 1, 3)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), OV to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameters	74LVX4245 $T_A = +25°C$, $C_L = 50$ pF, *$V_{CCA} = 5V$, **$V_{CCB} = 3.3V$			74LVX4245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, *$V_{CCA} = 5V$, **$V_{CCB} = 3.3V$		74LVX4245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, *$V_{CCA} = 5V$, $V_{CCB} = 2.7V$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	5.1	8.5	1.0	9.0	1.0	10.0	ns
t_{PLH}	A to B	1.0	5.3	8.5	1.0	9.0	1.0	10.0	
t_{PHL}	Propagation Delay	1.0	5.4	8.5	1.0	9.0	1.0	10.0	ns
t_{PLH}	B to A	1.0	5.5	8.5	1.0	9.0	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	6.5	10.0	1.0	10.5	1.0	11.5	ns
t_{PZH}	$\overline{OE}$ to B	1.0	6.7	10.0	1.0	10.5	1.0	11.5	
t_{PZL}	Output Enable Time	1.0	5.2	9.0	1.0	9.5	1.0	10.0	ns
t_{PZH}	$\overline{OE}$ to A	1.0	5.8	9.0	1.0	9.5	1.0	10.0	
t_{PHZ}	Output Disable Time	1.0	6.0	9.5	1.0	10.0	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to B	1.0	3.3	6.5	1.0	7.0	1.0	7.5	
t_{PHZ}	Output Disable Time	1.0	3.9	7.0	1.0	7.5	1.0	7.5	ns
t_{PLZ}	$\overline{OE}$ to A	1.0	2.9	6.5	1.0	7.0	1.0	7.5	
t_{OSHL}	Output to Output								ns
t_{OSLH}	Skew***		1.0	1.5		1.5		1.5	
	Data to Output								

*Voltage Range 5.0V is 5.0V ±0.5V.
**Voltage Range 3.3V is 3.3V ±0.3V.
***Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

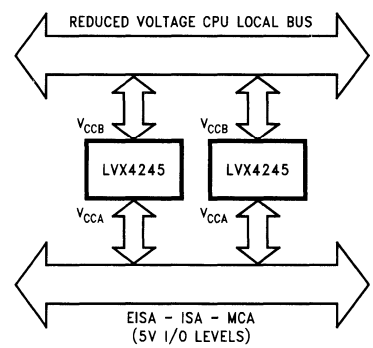
Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		15	pF	$V_{CCA} = 5.0V$, $V_{CCB} = 3.3V$
C_{PD}	Power Dissipation Capacitance	B → A	55	pF	$V_{CCA} = 5.0V$
		A → B	40	pF	$V_{CCB} = 3.3V$

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



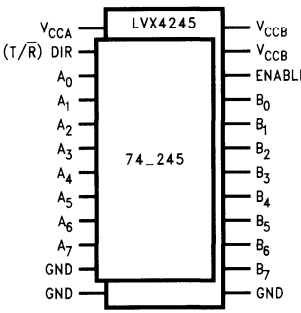
TL/F/11540–3

Applications: Mixed Mode Dual Supply Interface Solution

LVX4245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latch-up effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

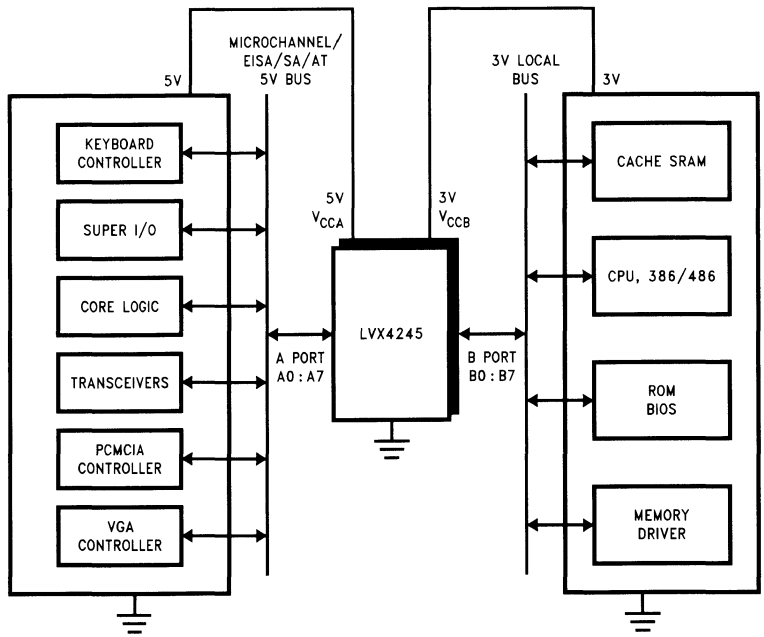
In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 5V port to interface 5V ICs. The "B" port is a dedicated port to interface 3V ICs. *Figure 1* shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

This device is also configured as an 8-bit 245 transceiver, giving the designer TRI-STATE capabilities and the ability to select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 74 series 245, as shown in *Figure 2*, the designer could use this device in either a 3V system or a 5V system without any further work to re-layout the board.



TL/F/11540–4

FIGURE 2. LVX4245 Pin Arrangement is Compatible to 20-Pin 74 Series 245



TL/F/11540–5

FIGURE 1. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem

National Semiconductor

74LVXC3245
8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs for 3V System

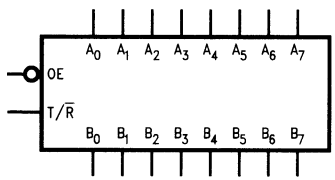
General Description

The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 3V supply level. The A port is a dedicated 3V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The B port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. The A port should interface with a 3V host system and the B port to the card slots. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP, and TSSOP packages
- Implements patented Quiet Series™ EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 74 series 245

Logic Symbol

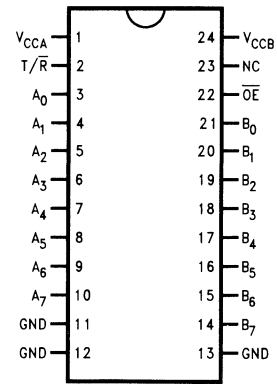


TL/F/12008–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, QSOP, and TSSOP



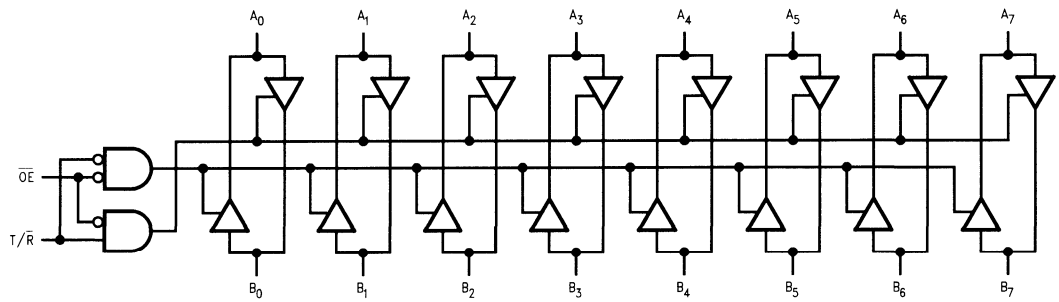
TL/F/12008–2

	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVXC3245WM 74LVXC3245WMX	74LVXC3245QSC 74LVXC3245QSCX	74LVXC3245MTC 74LVXC3245MTCX
See NS Package Number	M24B	MQA24	MTC24

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



TL/F/12008–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} +0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	−0.5V to V_{CCA} +0.5V
@ B_n	−0.5V to V_{CCB} +0.5V
DC Input Diode Curr. (I_{IK}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current(I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current	±200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions

Supply Voltage V_{CCA}	2.7V to 3.6V ($V_{CCA} \leq V_{CCB}$)
V_{CCB}	3.0V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input Output Voltage ($V_{I/O}$)	
@ A_n	0V to V_{CCA}
@ B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	8 ns/V

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC3245 T_A = 25°C	74LVXC3245 T_A = −40°C to +85°C		Units	Conditions
					Typ	Guaranteed Limits			
V_{IHA}	Minimum High Level Input Voltage	A_n, $\overline{OE}$ T/$\overline{R}$	2.7	3.0		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			3.0	3.6		2.0	2.0		
			3.6	5.5		2.0	2.0		
V_{IHB}		B_n	2.7	3.0		2.0	2.0		
			3.0	3.6		2.0	2.0		
			3.6	5.5		3.85	3.85		
V_{ILA}	Maximum Low Level Input Voltage	A_n, $\overline{OE}$ T/$\overline{R}$	2.7	3.0		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			3.0	3.6		0.8	0.8		
			3.6	5.5		0.8	0.8		
V_{ILB}		B_n	2.7	3.0		0.8	0.8		
			3.0	3.6		0.8	0.8		
			3.6	5.5		1.65	1.65		
V_{OHA}	Minimum High Level Output Voltage		3.0	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100\ \mu A$
			3.0	3.0	2.85	2.56	2.46		$I_{OH} = -12$ mA
			3.0	3.0	2.65	2.35	2.25		$I_{OH} = -24$ mA
			2.7	3.0	2.5	2.3	2.2		$I_{OH} = -12$ mA
			2.7	4.5	2.3	2.1	2.0		$I_{OH} = -24$ mA
V_{OHB}			3.0	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100\ \mu A$
			3.0	3.0	2.85	2.56	2.46		$I_{OH} = -12$ mA
			3.0	3.0	2.65	2.35	2.25		$I_{OH} = -24$ mA
			3.0	4.5	4.25	3.86	3.76		$I_{OH} = -24$ mA
V_{OLA}	Maximum Low Level Output Voltage		3.0	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			3.0	3.0	0.21	0.36	0.44		$I_{OL} = 24$ mA
			2.7	3.0	0.11	0.36	0.44		$I_{OL} = 12$ mA
			2.7	4.5	0.22	0.42	0.5		$I_{OL} = 24$ mA
V_{OLB}			3.0	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			3.0	3.0	0.21	0.36	0.44		$I_{OL} = 24$ mA
			3.0	4.5	0.18	0.36	0.44		$I_{OL} = 24$ mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC3245 $T_A = +25°C$ Typ	74LVXC3245 $T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A_n		3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND
I_{OZB}	Maximum TRI-STATE Output Leakage @ B_n		3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CC}/Input	B_n	3.6	5.5	1.0	1.35	1.5	mA	$V_I = V_{CCB}-2.1V$
		All Inputs	3.6	3.6		0.35	0.5		$V_I = V_{CC}-0.6V$
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		3.6	Open		5	50	μA	$A_n = V_{CCA}$ or GND B_n = Open, $\overline{OE} = V_{CCA}$, T/$\overline{R} = V_{CCA}$, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		3.6 3.6	3.6 5.5		5 5	50 50	μA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6 3.6	3.6 5.5		5 8	50 80	μA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, T/$\overline{R} = V_{CCA}$
V_{OLPA}	Quiet Output Maximum Dynamic V_{OL}		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 2, 3)
V_{OLPB}			3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 2, 3)
V_{OLVA}	Quiet Output Minimum Dynamic V_{OL}		3.3 3.3	3.3 5.0		−0.8 −0.8		V	(Notes 2, 3)
V_{OLVB}			3.3 3.3	3.3 5.0		−0.8 −1.2		V	(Notes 2, 3)
V_{IHDA}	Minimum High Level Dynamic Input Voltage		3.3 3.3	3.3 5.0		2.0 2.0		V	(Notes 2, 4)
V_{IHDB}			3.3 3.3	3.3 5.0		2.0 3.5		V	(Notes 2, 4)
V_{ILDA}	Maximum Low Level Dynamic Input Voltage		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 2, 4)
V_{ILDB}			3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 2, 4)

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	74LVXC3245 $T_A = +25°C$ $C_L = 50$ pF $V_{CCA} = 2.7V–3.6V$ $V_{CCB} = 4.5V–5.5V$			74LVXC3245 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF $V_{CCA} = 2.7V–3.6V$ $V_{CCB} = 4.5V–5.5V$		74LVXC3245 $T_A = +25°C$ $C_L = 50$ pF $V_{CCA} = 2.7V–3.6V$ $V_{CCB} = 3.0V–3.6V$			74LVXC3245 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF $V_{CCA} = 2.7V–3.6V$ $V_{CCB} = 3.0V–3.6V$		Units
		Min	Typ (Note 5)	Max	Min	Max	Min	Typ (Note 6)	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
t_{PLH}	A to B	1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
t_{PHL}	Propagation Delay	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
t_{PLH}	B to A	1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
t_{PZL}	Output Enable Time	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
t_{PZH}	$\overline{OE}$ to B	1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
t_{PZH}	$\overline{OE}$ to A	1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to B	1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
t_{PHZ}	Output Disable Time	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to A	1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
t_{OSHL}	Output to Output											
t_{OSLH}	Skew*		1.0	1.5		1.5		1.0	1.5		1.5	ns
	Data to Output											

Note 5: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 5.0V$ @ 25°C.

Note 6: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 3.3V$ @ 25°C.

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

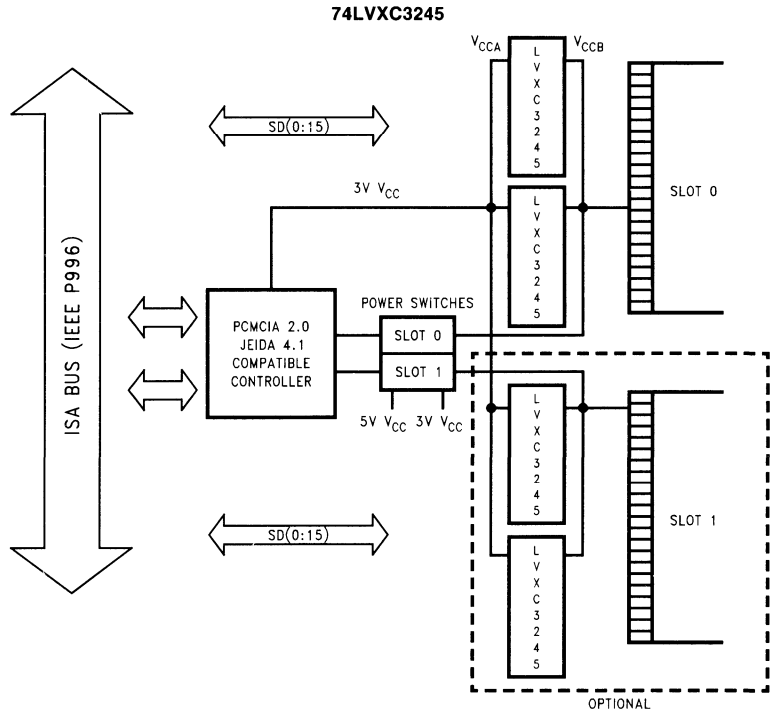
Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		10	pF	$V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$
C_{PD}	Power Dissipation Capacitance	A → B	50	pF	$V_{CCB} = 5.0V$
		B → A	40	pF	$V_{CCA} = 3.3V$

C_{PD} is measured at 10 MHz.

5

Configurable I/O Application for PCMCIA Cards

Block Diagram



TL/F/12008–3

The LVXC3245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC3245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC3245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC3245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

National Semiconductor

74LVXC4245
8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

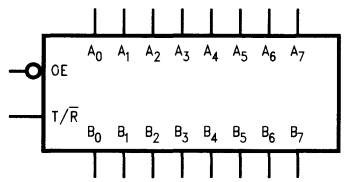
General Description

The LVXC4245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 5V supply level. The "A" port is a dedicated 5V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The "B" port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. This device will allow the V_{CCB} voltage source pin and I/O pins on the "B" port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 5V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements patented Quiet Series™ EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 74 series 245

Logic Symbol

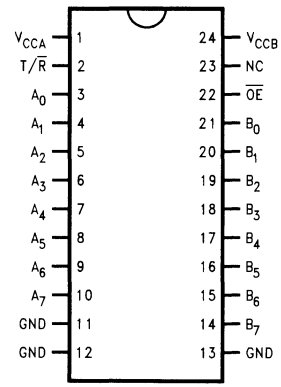


TL/F/12009–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/12009–2

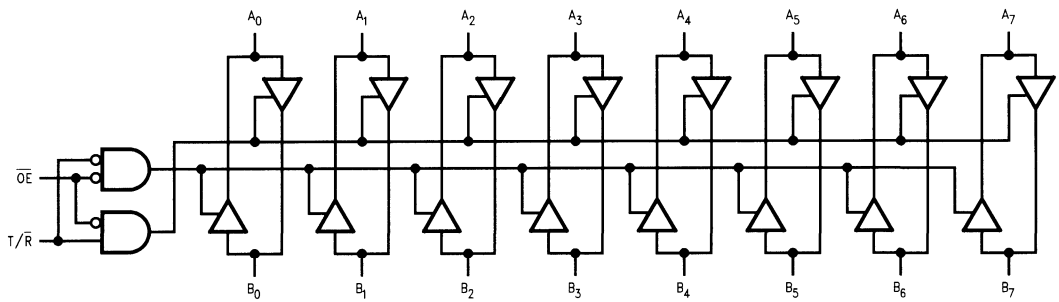
	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVXC4245WM 74LVXC4245WMX	74LVXC4245QSC 74LVXC4245QSCX	74LVXC4245MTC 74LVXC4245MTCX
See NS Package Number	M24B	MQA24	MTC24

5

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



TL/F/12009–4

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA},V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} +0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	−0.5V to V_{CCA} +0.5V
@ B_n	−0.5V to V_{CCB} +0.5V
DC Input Diode Current (I_{IK}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current	±200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions

Supply Voltage V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@A_n	0V to V_{CCA}
@B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3V, 4.5V, 5.5V	

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC4245 T_A = +25°C Typ	74LVXC4245 T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IHA}	Minimum High Level Input Voltage	A_n	4.5	2.7		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6		2.0	2.0		
		T/$\overline{R}$	5.5	5.5		2.0	2.0		
V_{IHB}		B_n	4.5	2.7		2.0	2.0		
			4.5	3.6		2.0	2.0		
			4.5	5.5		3.85	3.85		
V_{ILA}	Maximum Low Level Input Voltage	A_n	4.5	2.7		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6		0.8	0.8		
		T/$\overline{R}$	5.5	5.5		0.8	0.8		
V_{ILB}		B_n	4.5	2.7		0.8	0.8		
			4.5	3.6		0.8	0.8		
			4.5	5.5		1.65	1.65		
V_{OHA}	Minimum High Level Output Voltage		4.5	3.0	4.49	4.4	4.4	V	I_{OUT} = −100 μA
			4.5	3.0	4.25	3.86	3.76		I_{OH} = −24 mA
V_{OHB}			4.5	3.0	2.99	2.9	2.9	V	I_{OUT} = −100 μA
			4.5	3.0	2.85	2.56	2.46		I_{OH} = −12 mA
			4.5	3.0	2.65	2.35	2.25		I_{OH} = −24 mA
			4.5	2.7	2.5	2.3	2.2		I_{OH} = −12 mA
			4.5	2.7	2.3	2.1	2.0		I_{OH} = −24 mA
			4.5	4.5	4.25	3.86	3.76		I_{OH} = −24 mA
V_{OLA}	Maximum Low Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	I_{OUT} = 100 μA
			4.5	3.0	0.21	0.36	0.44		I_{OL} = 24 mA
V_{OLB}			4.5	3.0	0.002	0.1	0.1	V	I_{OUT} = 100 μA
			4.5	3.0	0.21	0.36	0.44		I_{OL} = 24 mA
			4.5	2.7	0.11	0.36	0.44		I_{OL} = 12 mA
			4.5	2.7	0.22	0.42	0.5		I_{OL} = 24 mA
			4.5	4.5	0.18	0.36	0.44		I_{OL} = 24 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC4245 $T_A = +25°C$ Typ	74LVXC4245 $T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		5.5 5.5	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A_n		5.5 5.5	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND
I_{OZB}	Maximum TRI-STATE Output Leakage @ B_n		5.5 5.5	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CC}/Input	All Inputs	5.5	5.5	1.0	1.35	1.5	mA	$V_I = V_{CC} - 2.1V$
		B_n	5.5	3.6		0.35	0.5	mA	$V_I = V_{CCB} - 0.6V$
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		5.5	Open		8	80	μA	$A_n = V_{CCA}$ or GND B_n = Open, $\overline{OE} = V_{CCA}$ T/$\overline{R}$ = V_{CCA}, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		5.5 5.5	3.6 5.5		8 8	80 80	μA	$A_n = V_{CCA}$ or GND $B_n = V_{CCB}$ or GND $\overline{OE}$ = GND, T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current		5.5 5.5	3.6 5.5		5 8	50 80	μA	$A_n = V_{CCA}$ or GND $B_n = V_{CCB}$ or GND $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CCA}
V_{OLPA}	Quiet Output Maximum Dynamic V_{OL}		5.0 5.0	3.3 5.0		1.5 1.5		V	(Notes 1 and 2)
V_{OLPB}			5.0 5.0	3.3 5.0		0.8 1.5		V	(Notes 1 and 2)
V_{OLVA}	Quiet Output Minimum Dynamic V_{OL}		5.0 5.0	3.3 5.0		−1.2 −1.2		V	(Notes 1 and 2)
V_{OLVB}			5.0 5.0	3.3 5.0		−0.8 −1.2		V	(Notes 1 and 2)
V_{IHDA}	Minimum High Level Dynamic Input Voltage		5.0 5.0	3.3 5.0		2.0 2.0		V	(Notes 1 and 3)
V_{IHDB}			5.0 5.0	3.3 5.0		2.0 3.5		V	(Notes 1 and 3)
V_{ILDA}	Maximum Low Level Dynamic Input Voltage		5.0 5.0	3.3 5.0		0.8 0.8		V	(Notes 1 and 3)
V_{ILDB}			5.0 5.0	3.3 5.0		0.8 1.5		V	(Notes 1 and 3)

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n−1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	74LVXC4245 C_L = 50 pF, V_{CCA} = 4.5V to 5.5V, V_{CCB} = 4.5V to 5.5V					74LVXC4245 C_L = 50 pF, V_{CCA} = 4.5V to 5.5V, V_{CCB} = 2.7V to 3.6V					Units
		T_A = +25°C			T_A = −40°C to +85°C		T_A = +25°C			T_A = −40°C to +85°C		
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	4.9 4.0	6.5 5.5	1.0 1.0	7.0 6.0	1.0 1.0	5.5 5.0	7.5 7.0	1.0 1.0	8.0 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	4.7 3.9	6.5 5.0	1.0 1.0	7.0 5.5	1.0 1.0	5.6 4.3	7.5 6.0	1.0 1.0	8.0 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	5.6 5.7	7.5 7.5	1.0 1.0	8.0 8.0	1.0 1.0	6.7 6.9	9.0 9.5	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	7.4 6.1	9.0 7.5	1.0 1.0	10.0 8.5	1.0 1.0	8.0 6.3	10.0 8.0	1.0 1.0	11.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.8 3.8	7.0 5.5	1.0 1.0	7.5 6.0	1.0 1.0	6.0 4.2	9.0 6.5	1.0 1.0	9.5 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	3.4 2.9	5.5 4.5	1.0 1.0	6.0 5.0	1.0 1.0	3.4 2.9	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3) Data to Output		1.0	1.5		1.5		1.0	1.5		1.5	ns

Note 1: Typical values at V_{CCA} = 5V, V_{CCB} = 5V @25°C.

Note 2: Typical values at V_{CCA} = 5V, V_{CCB} = 3.3V @25°C.

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

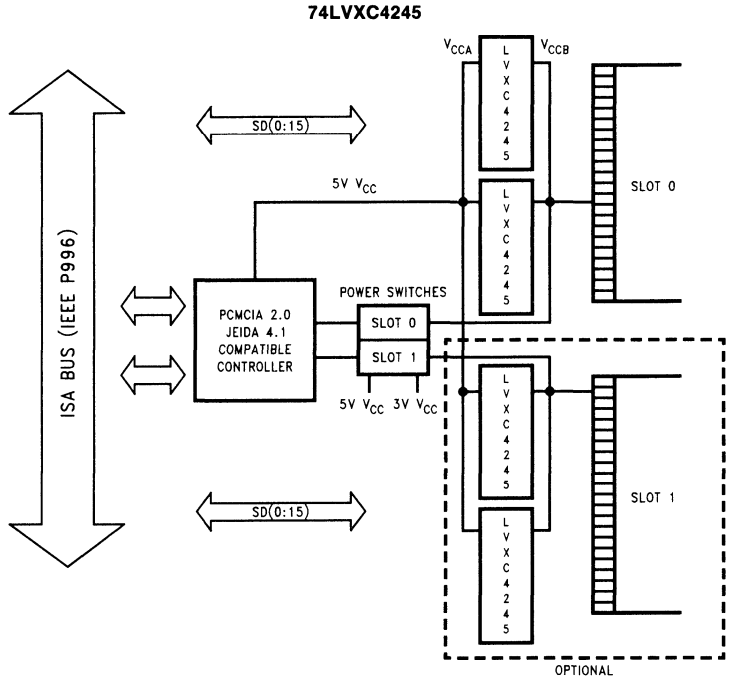
Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		10	pF	V_{CCA} = 5V, V_{CCB} = 3.3V
C_{PD}	Power Dissipation Capacitance	A → B	45	pF	V_{CCA} = 5V
		B → A	50	pF	V_{CCB} = 3.3V

Note: C_{PD} is measured at 10 MHz.

Configurable I/O Application for PCMCIA Cards

Block Diagram



TL/F/12009–3

The LVXC4245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC4245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC4245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC4245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC4245 must always be tied to a 5V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the block diagram above, the LVXC4245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

National Semiconductor

ADVANCE INFORMATION

74LVXC164245
16-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

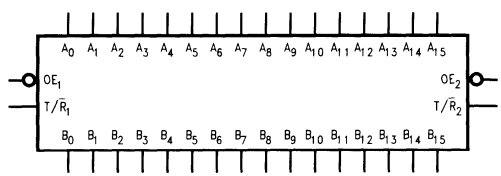
General Description

The LVXC164245 is a 48-pin dual-supply, 16-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCB} pin accepts a 5V supply level. The "B" port is a dedicated 5V port. The V_{CCA} pin accepts a 3V-to-5V supply level. The "A" port is configured to track the V_{CCA} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. This device will allow the V_{CCA} voltage source pin and I/O pins on the "A" port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Power up/down high impedance provides glitch-free bus loading
- Allows A port and V_{CCA} to float simultaneously when $\overline{OE}$ is HIGH
- Bidirectional interface between 5V and 3V-to-5V buses
- Inputs compatible with TTL level
- Allow dual V_{CC} supplies power up/down easily when $\overline{OE}$ is HIGH
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SSOP and TSSOP packages
- Implements patented Quiet Series™ EMI reduction circuitry
- Flexible V_{CCA} operating range
- Functionally compatible with the 74 series 16245

Logic Symbol



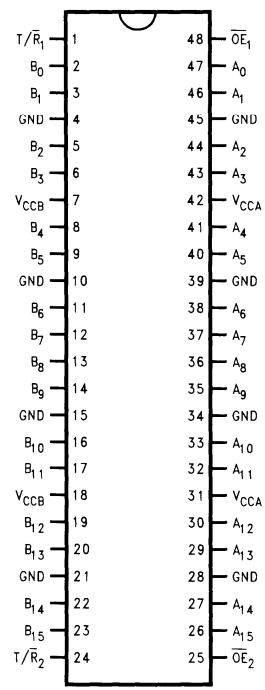
TL/F/12535–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/TRI-STATE Outputs
B_0–B_{15}	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVXC164245MEA 74LVXC164245MEAX	74LVXC164245MTD 74LVXC164245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12535–2

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Functional Description

The LVXC164245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

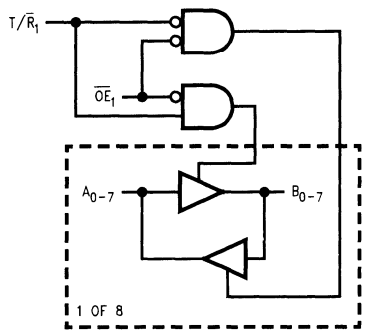
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

H = High Voltage Level L = Low Voltage Level

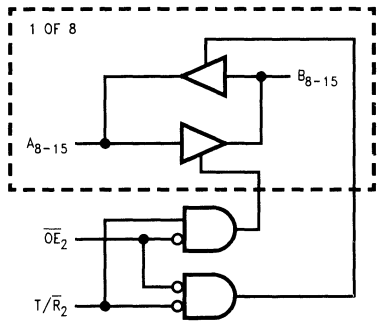
Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

X = Immaterial Z = High Impedance

Logic Diagrams



TL/F/12535–3



TL/F/12535–4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

PRELIMINARY

74LVX161284
Low Voltage IEEE 161284 Transceiver

General Description

The 74LVX161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE P1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in an Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

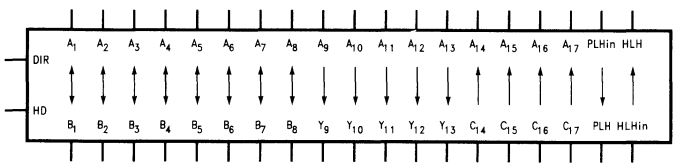
Outputs on the cable side can be configured to be either open drain or high drive (± 14 mA) and are connected to a separate power supply pin (V_{CC}_cable) to allow these outputs to be driven by a higher supply voltage than the A-side. The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the V_{CC}_cable supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs designed to interface with 3V logic. The DIR input controls data flow on the A_1–A_8/B_1–B_8 transceiver pins.

Features

- Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Replaces the function of two (2) 74ACT1284 devices
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- Inputs and outputs on cable side have internal pull-up resistors
- Flow-through pin configuration allows easy interface between the Peripheral and Host

Logic Symbol

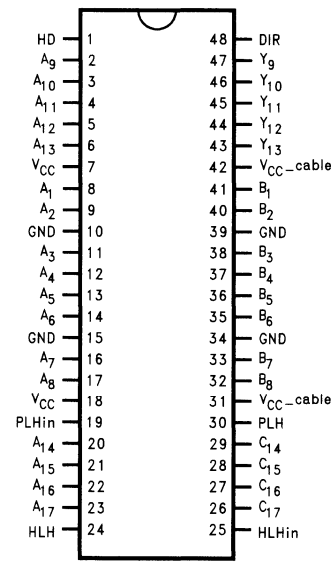


TL/F/12145–2

	SSOP JEDEC
Order Number	74LVX161284MEA 74LVX161284MEAX
See NS Package Number	MS48A

Connection Diagram

Pin Assignment for SSOP



TL/F/12145–1

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Pin Descriptions

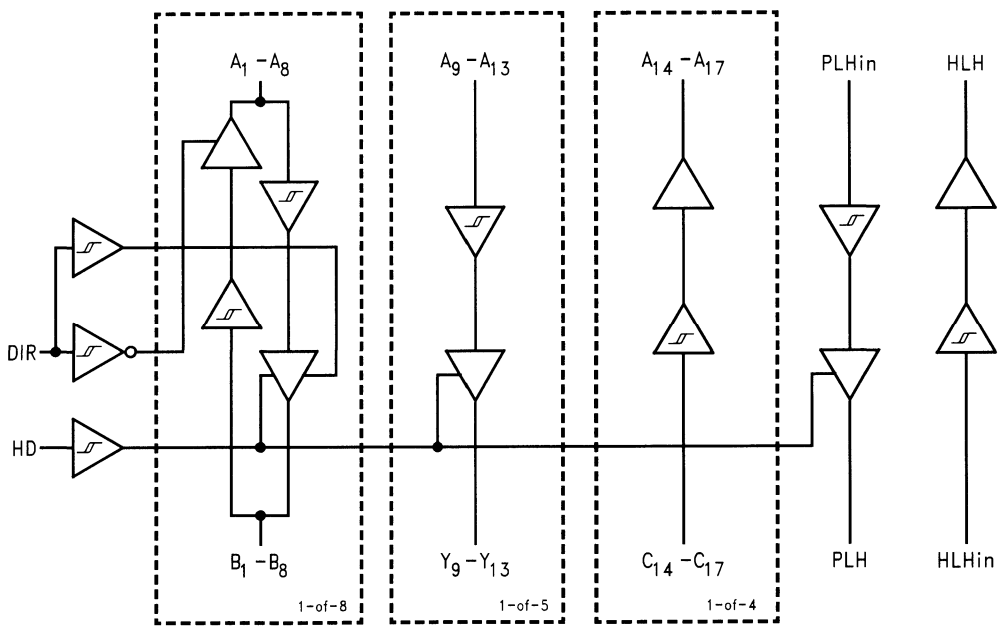
Pin Names	Description
HD	High Drive Enable Input (Active High)
DIR	Direction Control Input
A_1–A_8	Inputs or Outputs
B_1–B_8	Inputs or Outputs
A_9–A_{13}	Inputs
Y_9–Y_{13}	Outputs
A_{14}–A_{17}	Outputs
C_{14}–C_{17}	Inputs
PLH_{IN}	Peripheral Logic High Input
PLH	Peripheral Logic High Output
HLH_{IN}	Host Logic High Input
HLH	Host Logic High Output

Truth Table

Inputs		Outputs
DIR	HD	
L	L	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
L	H	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}
H	L	A_1–A_8 Data to B_1–B_8** A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
H	H	A_1–A_8 Data to B_1–B_8 A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}

Note: *Y_9–Y_{13} Open Drain Outputs
**B_1–B_8 Open Drain Outputs

Logic Diagram



TL/F/12145–3

Absolute Maximum Ratings (Note 1)

Supply Voltage
- V_{CC} −0.5V to +5.5V
- $V_{CC-Cable}$ −0.5V to +7.0V
- $V_{CC-Cable}$ Must Be ≥ V_{CC}

Input Voltage (V_I)—(Note 2)
- A_1-A_{13}, PLH_{IN}, DIR, HD −0.5V to V_{CC} + 0.5V
- B_1-B_8, $C_{14}-C_{17}$, HLH_{IN} −0.5V to +5.5V (DC)
- B_1-B_8, $C_{14}-C_{17}$, HLH_{IN} −2.0V to +7.0V*
  *40 ns Transient

Output Voltage (V_O)
- A_1-A_8, $A_{14}-A_{17}$, HLH −0.5V to V_{CC} +0.5V
- B_1-B_8, Y_9-Y_{13}, PLH −0.5V to +5.5V (DC)
- B_1-B_8, Y_9-Y_{13}, PLH −2.0V to +7.0V*
  *40 ns Transient

DC Output Current (I_O)
- A_1-A_8, HLH ±25 mA
- B_1-B_8, Y_9-Y_{13} ±50 mA
- PLH (Output LOW) 84 mA
- PLH (Output HIGH) −50 mA

Input Diode Current (I_{IK})—(Note 2)
- DIR, HD, A_9-A_{13}, PLH, HLH, $C_{14}-C_{17}$ −20 mA

Output Diode Current (I_{OK})
- A_1-A_8, $A_{14}-A_{17}$, HLH ±50 mA
- B_1-B_8, Y_9-Y_{13}, PLH −50 mA

DC Continuous V_{CC} or Ground Current ±200 mA

Storage Temperature −65°C to +150°C

ESD (HBM) Last Passing Voltage 2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. National does not recommend operation outside the databook specifications.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Supply Voltage
- V_{CC} 3.0V to 3.6V
- $V_{CC-Cable}$ 3.0V to 5.5V

DC Input Voltage (V_I) 0V to V_{CC}

Open Drain Voltage (V_O) 0V to 5.5V

Operating Temperature (T_A) −40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$V_{CC-Cable}$ (V)	74LVX161284 T_A = 0°C to +70°C	74LVX161284 T_A = −40°C to +85°C	Units	Conditions
					Guaranteed Limits			
V_{IK}	Input Clamp Diode Voltage		3.0	3.0	−1.2	−1.2	V	I_i = −18 mA
V_{IH}	Minimum High Level Input Voltage	A_n, B_n, PLH_{IN}, DIR, HD	3.0–3.6	3.0–5.5	2.0	2.0	V	V_T(Pos) ≥ 2.0V V_T(Pos) ≥ 2.4V
		C_n	3.0–3.6	3.0–5.5	2.3	2.3		
		HLH_{IN}	3.0–3.6	3.0–5.5	2.6	2.6		
V_{IL}	Maximum High Level Input Voltage	A_n, B_n, PLH_{IN}, DIR, HD	3.0–3.6	3.0–5.5	0.8	0.8	V	V_T(Neg) ≤ 1.2V V_T(Neg) ≤ 1.9V
		C_n	3.0–3.6	3.0–5.5	0.8	0.8		
		HLH_{IN}	3.0–3.6	3.0–5.5	1.6	1.6		
ΔV_T	Minimum Input Hysteresis	A_n, B_n, PLH_{IN} DIR, HD	3.3	3.0–5.5	0.4	0.4	V	$V_T^+ - V_T^-$ $V_T^+ - V_T^-$
		C_n	3.0–3.6	3.0–5.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	A_n, HLH	3.0 3.0	3.0 3.0	2.8 2.4	2.8 2.4	V	I_{OH} = −50 μA I_{OH} = −4 mA
		B_n, Y_n	3.0	3.0	2.23	2.23	V	I_{OH} = −14 mA I_{OH} = −500 μA
		PLH	3.15	3.15	3.1	3.1		
V_{OL}	Maximum Low Level Output Voltage	A_n, HLH	3.0 3.0	3.0 3.0	0.2 0.4	0.2 0.4	V	I_{OL} = 50 μA I_{OL} = 4 mA
		B_n, Y_n	3.0	3.0	0.77	0.77	V	I_{OL} = 14 mA I_{OL} = 84 mA
		PLH	3.0	3.0	0.8	0.8		
RD	Maximum Output Impedance	B_1-B_8, Y_9-Y_{13}	3.3 3.3	3.3 5.0	55 55	55 55	Ω	(Notes 1, 2)
	Minimum Output Impedance	B_1-B_8, Y_9-Y_{13}	3.3 3.3	3.3 5.0	35 35	35 35	Ω	(Notes 1, 2)

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DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	V_{CC_Cable} (V)	74LVX161284 $T_A = 0°C$ to $+70°C$ Guaranteed Limits	74LVX161284 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
RP	Maximum Pull-Up Resistance	B_1-B_8, Y_9-Y_{13}, $C_{14}-C_{17}$	3.3 3.3	3.3 5.0	1650 1650	1650 1650	Ω	(Note 2)
	Minimum Pull-Up Resistance	B_1-B_8, Y_9-Y_{13} $C_{14}-C_{17}$	3.3 3.3	3.3 5.0	1150 1150	1150 1150	Ω	(Note 2)
I_{IH}	Maximum Input Current in High State	A_9-A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	1.0	1.0	μA	$V_I = 3.6V$
		$C_{14}-C_{17}$	3.6	3.6	50.0	50.0	μA	$V_I = 3.6V$
		$C_{14}-C_{17}$	3.6	5.5	100	100	μA	$V_I = 5.5V$
I_{IL}	Maximum Input Current in Low State	A_9-A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	−1.0	−1.0	μA	$V_I = 0.0V$
		$C_{14}-C_{17}$	3.6	3.6	−3.5	−3.5	mA	$V_I = 0.0V$
		$C_{14}-C_{17}$	3,6	5.5	−5.0	−5.0	mA	$V_I = 0.0V$
I_{OZH}	Maximum Output Disable Current (High)	A_1-A_8	3.6	3.6	20	20	μA	$V_O = 3.6V$
		B_1-B_8	3.6	3.6	50	50	μA	$V_O = 3.6V$
		B_1-B_8	3.6	5.5	100	100	μA	$V_O = 5.5V$
I_{OZL}	Maximum Output Disable Current (Low)	A_1-A_8	3.6	3.6	−20	−20	μA	$V_O = 0.0V$
		B_1-B_8	3.6	3.6	−3.5	−3.5	mA	
		B_1-B_8	3.6	5.5	−5.0	−5.0	mA	
I_{OFF}	Power Down Output Leakage	B_1-B_8, Y_9-Y_{13}, PLH	0.0	0.0	100	100	μA	$V_O = 5.5V$
I_{OFF}	Power Down Input Leakage	$C_{14}-C_{17}$, HLH_{IN}	0.0	0.0	100	100	μA	$V_I = 5.5V$
I_{OFF}—I_{CC}	PowerDown Leakage to V_{CC}		0.0	0.0	250	250	μA	(Note 3)
I_{OFF}—I_{CC2}	Power Down Leakage to V_{CC_Cable}		0.0	0.0	250	250	μA	(Note 3)
I_{CC}	Maximum Supply Current		3.6 3.6	3.6 5.5	45 70	45 70	mA mA	$V_I = V_{CC}$ or GND $V_I = V_{CC}$ or GND

Note 1: Output impedance is measured with the output active low and active high (HD = high).

Note 2: Resistance is calculated using the following formula:

$$\text{Resistance} = \frac{1V}{(\text{Current at 2V on pin}) - (\text{Current at 1V on pin})}$$

Note 3: Power-down leakage to V_{CC} or V_{CC_Cable} is tested by simultaneously forcing all pins on the cable-side (B_1-B_8, Y_9-Y_{13}, PLH, $C_{14}-C_{17}$ and HLH_{IN}) to 5.5V and measuring the resulting I_{CC} or I_{CC_Cable}.

AC Electrical Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.0V-3.6V$, $V_{CC\_Cable} = 3.0V-5.5V$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V-3.6V$, $V_{CC\_Cable} = 3.0V-5.5V$		Units	Fig. No.
		Min	Max	Min	Max		
t_{PHL}	A_1-A_8 to B_1-B_8	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	A_1-A_8 to B_1-B_8	2.0	40.0	2.0	44.0	ns	2
t_{PHL}	B_1-B_8 to A_1-A_8	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	B_1-B_8 to A_1-A_8	2.0	40.0	2.0	44.0	ns	3
t_{PHL}	A_9-A_{13} to Y_9-Y_{13}	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	A_9-A_{13} to Y_9-Y_{13}	2.0	40.0	2.0	44.0	ns	2

AC Electrical Characteristics (Continued)

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.0V-3.6V$, $V_{CC\_Cable} = 3.0V-5.5V$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V-3.6V$, $V_{CC\_Cable} = 3.0V-5.5V$		Units	Fig. No.
		Min	Max	Min	Max		
t_{PHL}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	40.0	2.0	44.0	ns	3
t_{SKEW}	LH-LH or HL-HL		10.0		12.0	ns	(Note 1)
t_{PHL}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	2
t_{PHL}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	3
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A_1-A_8	2.0 2.0	15.0 15.0	2.0 2.0	18.0 18.0	ns	7
t_{PZH} t_{PZL}	Output Enable Time DIR to A_1-A_8	2.0 2.0	50.0 50.0	2.0 2.0	50.0 50.0	ns	8
t_{PHZ} t_{PLZ}	Output Disable Time DIR to B_1-B_8	2.0 2.0	50.0 50.0	2.0 2.0	50.0 50.0	ns	9
t_{pEN}	Output Enable Time HD to B_1-B_8, Y_9-Y_{13}	2.0 2.0	25.0 25.0	2.0 2.0	28.0 28.0	ns	2
t_{pDis}	Output Disable Time HD to B_1-B_8, Y_9-Y_{13}	2.0 2.0	25.0 25.0	2.0 2.0	28.0 28.0	ns	2
$t_{pEn}-t_{pDis}$	Output Enable- Output Disable		10.0		12.0	ns	
t_{SLEW} t_{PLH} t_{PHL}	Output Slew Rate B_1-B_8, Y_9-Y_{13}	 0.05 0.05	 0.40 0.40	 0.05 0.05	 0.40 0.40	V/ns	 5 4
t_r, t_f	t_{RISE} and t_{FALL} B_1-B_8*, Y_9-Y_{13}*		120 120		120 120	ns	6 (Note 2)

*Open Drain

Note 1: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type:

(i) A_1-A_8 to B_1-B_8, A_9-Y_{13} to Y_9-Y_{13}

(ii) B_1-B_8 to A_1-A_8

(iii) $C_{14}-C_{17}$ to $A_{14}-A_{17}$

Note 2: This parameter is guaranteed but not tested, characterized only.

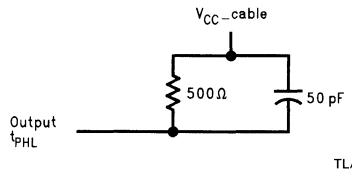
Note: Pulse Generator for all pulses; Rate $\leq$1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

Capacitance

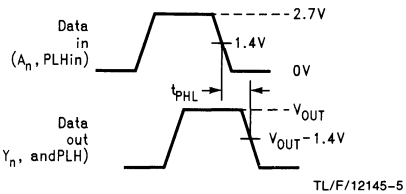
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0.0V (HD, DIR, A_9-A_{13}, $C_{14}-C_{17}$, PLH_{IN} and HLH_{IN})
$C_{I/O}$ (Note)	I/O Pin Capacitance	12	pF	V_{CC} = 3.3V

Note: $C_{I/O}$ is measured at frequency = 1 MHz, per MIL-STD-883B, Method 3012

AC Loading and Waveforms



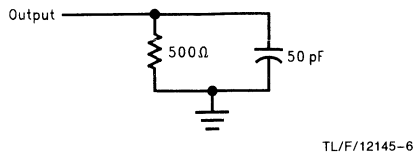
TL/F/12145–4



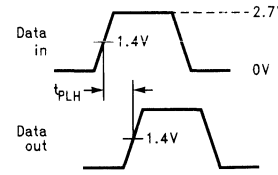
TL/F/12145–5

FIGURE 1. t_{PHL} Test Load and Waveforms
A_1-A_8 to B_1-B_8
A_9-A_{13} to Y_9-Y_{13}
PLHin to PLH

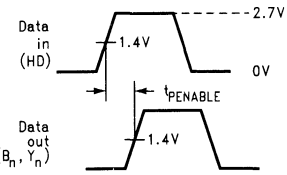
AC Loading and Waveforms (Continued)



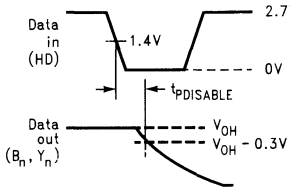
TL/F/12145-6



TL/F/12145-7

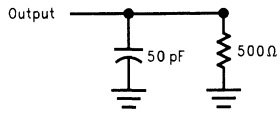


TL/F/12145-8

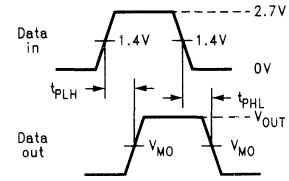


TL/F/12145-9

FIGURE 2. t_{PLH}, t_{PEn}, t_{PDis} Test Load and Waveforms
A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}
PLHin to PLH, HD to B_1–B_8, Y_9–Y_{13}, PLH



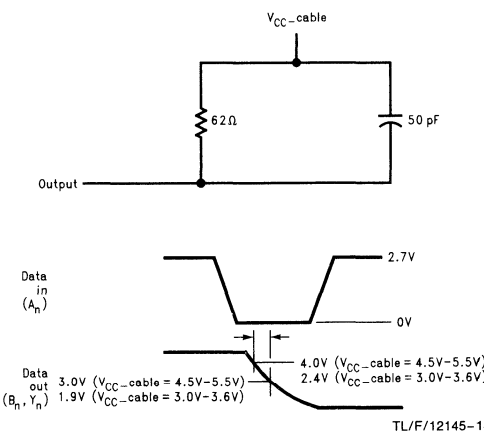
TL/F/12145-10



TL/F/12145-11

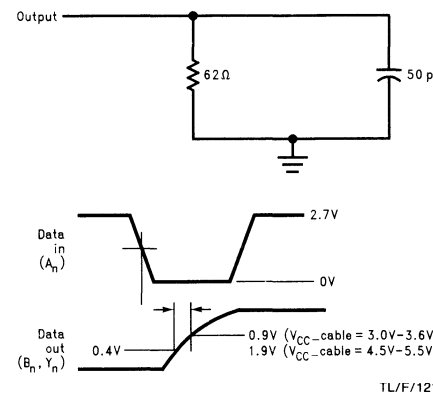
V_{MO} = 50% V_{CC}

FIGURE 3. t_{PHL}, t_{PLH} Test Load and Waveforms
B_1–B_8 to A_1–A_8, C_{14}–C_{17} to A_{14}–A_{17}, HLHin to HLH



TL/F/12145-14

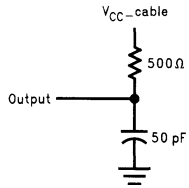
FIGURE 4. t_{SLEW} HL Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}



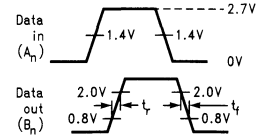
TL/F/12145-15

FIGURE 5. t_{SLEW} LH Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}

AC Loading and Waveforms (Continued)



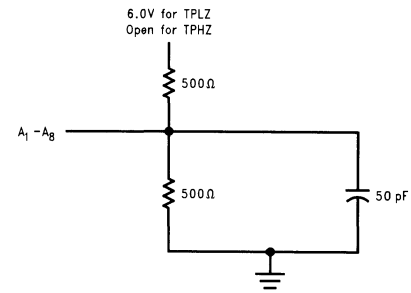
TL/F/12145–12



TL/F/12145–13

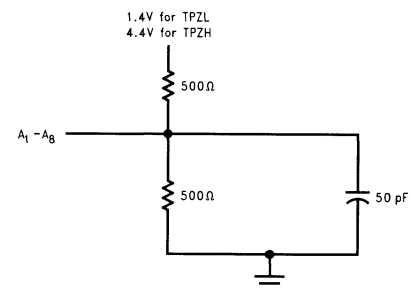
t_r = Output Rise Time, Open Drain
t_f = Output Fall Time, Open Drain

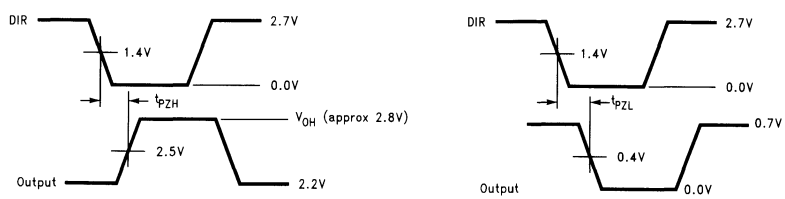
FIGURE 6. t_{RISE} and t_{FALL} Test Load and Waveforms for Open Drain Outputs A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}



TL/F/12145–16

FIGURE 7. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1–A_8





TL/F/12145–17

FIGURE 8. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to to A_1–A_8

AC Loading and Waveforms (Continued)

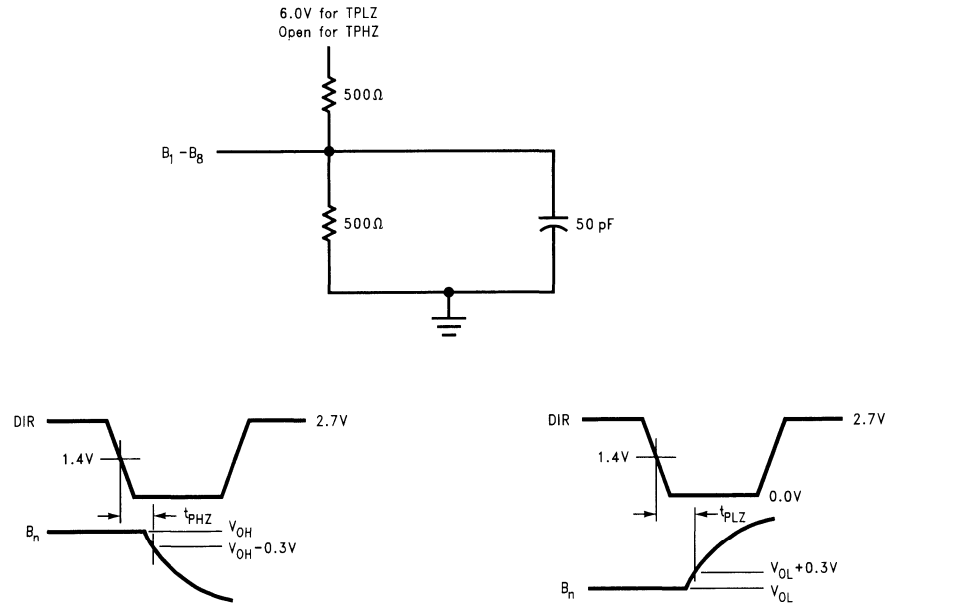
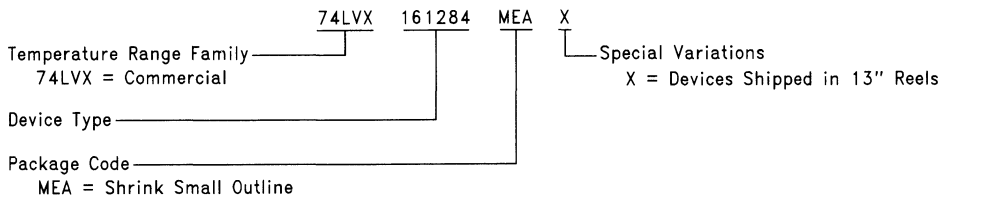


FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms DIR to to B_1–B_8

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Section 6

LVX Bus Switch Family

Section 6 Contents

LVX Bus Switch Family Features 6-3
NC7LVX384 1-Bit Low Power Bus Switch 6-4
74LVX3L383 10-Bit Low Power Bus-Exchange Switch 6-7
74LVX3L384 10-Bit Low Power Bus Switch 6-10
74LVX3L384A 10-Bit Low Power Extended Input Voltage Bus Switch 6-13
74LVX16212 24-Bit Bus Exchange Switch 6-16
AN-996 Using the Bus Switch as a 5V to 3V Translator 6-19
AN-997 Bus Switches in the Presence of Undershoot 6-20

National Semiconductor

LVX Bus Switch Family
Low Voltage CMOS Bus Switches

Features	Advantages
Near zero propagation delay (250 ps max)	High performance bus switching, bus exchanging, multiplexing, etc.
Low power (10 μA max I_{CCQ})	Saves power, extends battery life
Low ON resistance and input capacitance	Minimizes bus loading
74LVX3L384/A can be used as a 5V to 3V translator	Near zero delay translation
Undershoot hardened 74LVX3L384A	Isolates noisy bus connectors from the rest of the system
SOIC, QSOP, and TSSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

National Semiconductor

NC7LVX384
1-Bit Low Power Bus Switch

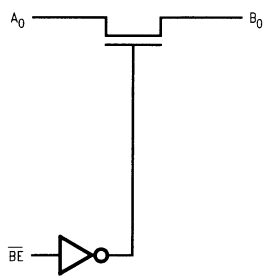
General Description

The LVX384 provides 1-bit of high-speed CMOS TTL-compatible bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as a 1-bit switch with a bus enable ($\overline{BE}$) signal. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

Features

- 5Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 μA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOT23-5 TinyPak™ package

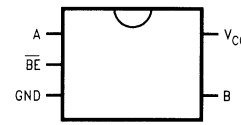
Logic Diagram



TL/F/12663–1

Connection Diagram

Pin Assignment for TinyPak



TL/F/12663–2

Truth Table

$\overline{BE}$	B_0	Function
L	A_0	Connect
L	A_0	Connect
H	HIGH-Z State	Connect
H	HIGH-Z State	Disconnect

Pin Names	Description
$\overline{BE}$	Bus Switch Enable
A_0	Bus A
B_0	Bus B

	5-Pin SOT23-5	Supplied As
Order Number	NC7LVX384M5 NC7LVX384M5X	250 Units in Tape and Reel 3000 Units in Tape and Reel
See NS Package Number	MA05B	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with (V_I < 0)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX0384 T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	I_{IN} = −18 mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	0 ≤ V_{IN} ≤ 5.25V
		5.25			±1	μA	
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	0 ≤ A, B ≤ V_{CC}
I_{OS}	Short Circuit Current	4.75	100			mA	V_I(A), V_I(B) = 0V, V_I(B), V_I(A) = 4.75V
R_{ON}	Switch On Resistance (Note 3)	4.75		5	7	Ω	V_I = 0V, I_{ON} = 30 mA
				10	15	Ω	V_I = 2.4V, I_{ON} = 15 mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	V_I = V_{CC}, GND I_O = 0
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	V_{IN} = 3.15V, I_O = 0 Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input (V_{IN} = 3.15V, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	NC7LVX384 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
T_{PLH} T_{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 6)	4.75			0.25	ns
T_{PZL} T_{PZH}	Switch Enable Time $\overline{BE}$ to A_0, B_0	4.75	1.5		6.5	ns
T_{PLZ} T_{PHZ}	Switch Disable Time $\overline{BE}$ to A_0, B_0	4.75	1.5		5.5	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

National Semiconductor

74LVX3L383
10-Bit Low Power Bus-Exchange Switch

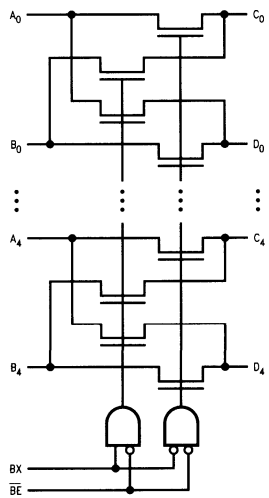
General Description

The LVX3L383 provides two sets of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device operates as a 10-bit bus switch or a 5-bit bus exchanger. The bus exchange (BX) signal provides nibble swapping of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters. The bus enable ($\overline{BE}$) signal turns the switches on.

Features

- 5Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 μA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC, TSSOP and QSOP (SSOP, 0.15" body width) packages

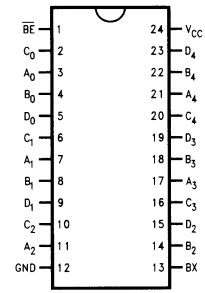
Logic Diagram



TL/F/11652–1

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/11652–2

Pin Names	Description
$\overline{BE}$	Bus Switch Enable
BX	Bus Exchange
A_0–A_4, B_0–B_4	Buses A, B
C_0–C_4, D_0–D_4	Buses C, D

Truth Table

$\overline{BE}$	BX	A_0–A_4	B_0–B_4	Function
H	X	High-Z State	High-Z State	Disconnect
L	L	C_0–C_4	D_0– D_4	Connect
L	H	D_0–D_4	C_0–C_4	Exchange

	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3L383WM 74LVX3L383WMX	74LVX3L383QSC 74LVX3L383QSCX	74LVX3L383MTC 74LVX3L383MTCX
See NS Package Number	M24B	MQA24	MTC24

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_I) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IN}) with $V_I < 0$	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX3L383 $T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	$I_{IN} = -18$ mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	$0 \le V_{IN} \le 5.25V$
		5.25			±1	μA	
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	$0 \le A, B \le V_{CC}$
I_{OS}	Short Circuit Current	4.75	100			mA	$V_I(A), V_I(B) = 0V$, $V_I(B), V_I(A) = 4.75V$
R_{ON}	Switch On Resistance (Note 3)	4.75		5	7	Ω	$V_I = 0V, I_{ON} = 30$ mA
				10	15	Ω	$V_I = 2.4V, I_{ON} = 15$ mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	$V_I = V_{CC}$, GND $I_O = 0$
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	$V_{IN} = 3.15V, I_O = 0$ Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven input ($V_{IN} = 3.15V$, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX3L383 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
t_{PLH} t_{PHL}	Data Propagation Delay A_n to B_n or B_n to A_n (Note 6)	4.75			0.25	ns
t_{PLH} t_{PHL}	Switch Exchange Time BX to A_n or B_n	4.75	1.5		6.5	ns
t_{PZL} t_{PZH}	Switch Enable Time $\overline{BE}$ to A_n, B_n	4.75	1.5		6.5	ns
t_{PLZ} t_{PHZ}	Switch Disenable Time $\overline{BE}$ to A_n, B_n	4.75	1.5		5.5	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

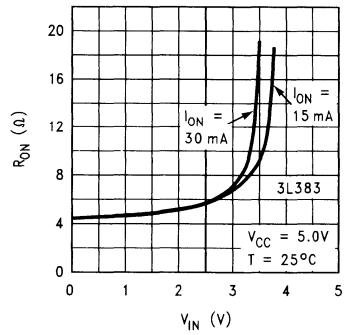
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

74LVX3L383 V_{IN} vs R_{ON} (Typ)



TL/F/11652–4

National Semiconductor

74LVX3L384
10-Bit Low Power Bus Switch

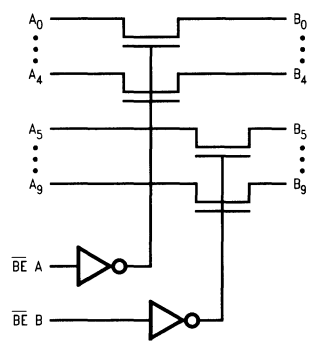
General Description

The LVX3L384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{BE}$) signals. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

Features

- 5Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 μA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC, TSSOP and QSOP (SSOP 0.15" Body width)

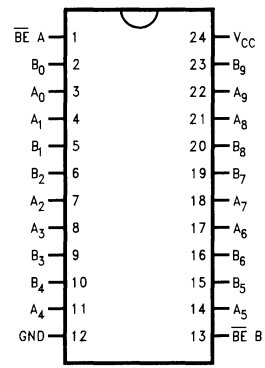
Logic Diagram



TL/F/11653–1

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/11653–2

Truth Table

$\overline{BE}$ A	$\overline{BE}$ B	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Pin Names	Description
$\overline{BE}$ A, $\overline{BE}$ B	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3L384WM 74LVX3L384WMX	74LVX3L384QSC 74LVX3L384QSCX	74LVX3L384MTC 74LVX3L384MTCX
See NS Package Number	M24B	MQA24	MTC24

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with (V_I < 0)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX3L384 T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	I_{IN} = −18 mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	0 ≤ V_{IN} ≤ 5.25V
		5.25			±1	μA	0 ≤ V_{IN} ≤ 5.25V
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	0 ≤ A, B ≤ V_{CC}
I_{OS}	Short Circuit Current	4.75	100			mA	V_I(A), V_I(B) = 0V, V_I(B), V_I(A) = 4.75V
R_{ON}	Switch On Resistance (Note 3)	4.75		5	7	Ω	V_I = 0V, I_{ON} = 30 mA
				10	15	Ω	V_I = 2.4V, I_{ON} = 15 mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	V_I = V_{CC}, GND I_O = 0
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	V_{IN} = 3.15V, I_O = 0 Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input (V_{IN} = 3.15V, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX3L384 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
T_{PLH} T_{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 6)	4.75			0.25	ns
T_{PZL} T_{PZH}	Switch Enable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		6.5	ns
T_{PLZ} T_{PHZ}	Switch Disable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		5.5	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

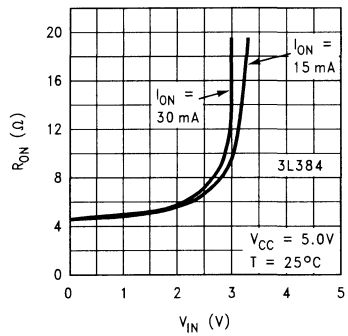
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

74LVX3L384 V_{IN} vs R_{ON} (Typ)



TL/F/11653–3

National Semiconductor

74LVX3L384A
10-Bit Low Power Extended Input Voltage Bus Switch

General Description

The LVX3L384A provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{BE}$) signals. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The 74LVX3L384A 10-bit bus switch is pin-for-pin and function compatible with the 74LVX3L384 device. It has the added feature of allowing extended negative input voltages on the I/O pins. The 74LVX3L384A bus switch, unlike most bus switches on the market, will not falsely turn on when $\overline{BE}$ is high and negative undershoot voltages are encountered on the I/O pins. Thus it is "undershoot hardened" (see related application note) tolerating undershoots up to −1.5V.

Typical applications include IDE bus connector interfaces, PCI card interfaces, backplane card interfaces, and other noisy environments where switches are needed.

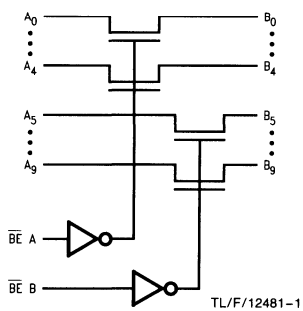
Features

- Extended input voltage design tolerates input undershoots up to −1.5V
- 10Ω switch connection between two ports
- Ultra low power with 2 μA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC, QSOP and TSSOP

Truth Table

$\overline{BE}$ A	$\overline{BE}$ B	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Logic Diagram

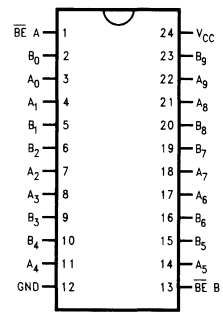


TL/F/12481–1

Pin Names	Description
$\overline{BE}$ A, $\overline{BE}$ B	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



TL/F/12481–2

	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3L384AWM 74LVX3L384AWMX	74LVX3L384AQSC 74LVX3L384AQSCX	74LVX3L384AMTC 74LVX3L384AMTCX
See NS Package Number	M24B	MQA24	MTC24

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with ($V_I < 0$)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX3L384A $T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	$I_{IN} = -18$ mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	$0 \le V_{IN} \le 5.25V$
		5.25			±1	μA	
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	$0 \le A, B \le V_{CC}$
I_{OS}	Short Circuit Current	4.75	100			mA	$V_I(A), V_I(B) = 0V$, $V_I(B), V_I(A) = 4.75V$
R_{ON}	Switch On Resistance (Note 3)	4.75		6	12	Ω	$V_I = 0V$, $I_{ON} = 30$ mA
				15	25	Ω	$V_I = 2.4V$, $I_{ON} = 15$ mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	$V_I = V_{CC}$, GND $I_O = 0$
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	$V_{IN} = 3.15V$, $I_O = 0$ Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input ($V_{IN} = 3.15V$, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX3L384A $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
T_{PLH} T_{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 6)	4.75			0.50	ns
T_{PZL} T_{PZH}	Switch Enable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		6.8	ns
T_{PLZ} T_{PHZ}	Switch Disable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		6.0	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

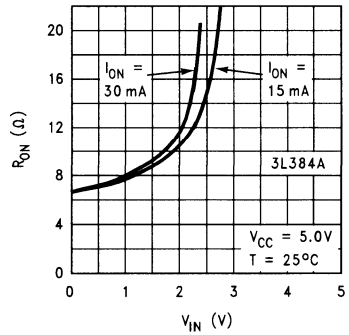
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.5 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

74LVX3L384A V_{IN} vs R_{ON} (Typ)



TL/F/12481–3

National Semiconductor

ADVANCE INFORMATION

74LVX16212
24-Bit Bus-Exchange Switch

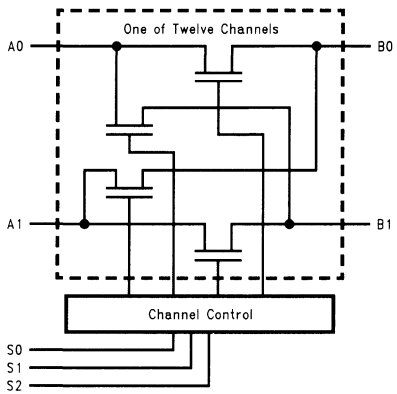
General Description

The LVX16212 provides 24 bits of high-speed CMOS TTL-compatible bus switches or bus exchangers. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device provides data exchanging between the four signal ports (A0 B0, A1 and B1) through the data-select (S0, S1 and S2) inputs.

Features

- 5Ω switch connection between two ports
- Zero propagation delay
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SSOP and TSSOP

Logic Symbol



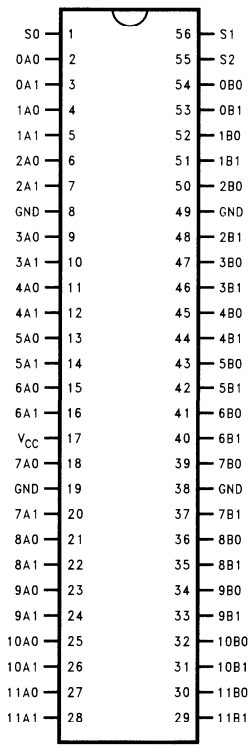
TL/F/12641–1

Truth Table

S2	S1	S0	A0	A1	Function
L	L	L	Z	Z	Disconnect
L	L	H	B0	Z	A0 to B0
L	H	L	B1	Z	A0 to B1
L	H	H	Z	B0	A1 to B0
H	L	L	Z	B1	A1 to B1
H	L	H	Z	Z	Disconnect
H	H	L	B0	B1	A0 to B0, A1 to B1
H	H	H	B1	B0	A0 to B1, A1 to B0

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12641–2

	SSOP	TSSOP
Order Number	74LVX16212MEA 74LVX16212MEAX	74LVX16212MTD 74LVX16212MTDX
See NS Package Number	MS56A	MTD56

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with ($V_I < 0$)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX16212 $T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	$I_{IN} = -18$ mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	$0 \le V_{IN} \le 5.25V$
		5.25			±1	μA	
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	$0 \le A, B \le V_{CC}$
I_{OS}	Short Circuit Current	4.75	100			mA	$V_I(A), V_I(B) = 0V$, $V_I(B), V_I(A) = 4.75V$
R_{ON}	Switch On Resistance (Note 3)	4.75		5	7	Ω	$V_I = 0V$, $I_{ON} = 30$ mA
				10	15	Ω	$V_I = 2.4V$, $I_{ON} = 15$ mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	20	μA	$V_I = V_{CC}$, GND $I_O = 0$
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	$V_{IN} = 3.15V$, $I_O = 0$ per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input ($V_{IN} = 3.15V$, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX16212 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
T_{PLH} T_{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 6)	4.75			0.25	ns
T_{PLH} T_{PHL}	Switch Exchange Time S0, S1, S2 to An or Bn	4.75	1.5		6.5	ns
T_{PZL} T_{PZH}	Switch Enable Time S0, S1, S2 to An, Bn	4.75	1.5		6.5	ns
T_{PLZ} T_{PHZ}	Switch Disable Time S0, S1, S2 to An, Bn	4.75	1.5		5.5	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

Using the Bus Switch* as a 5V to 3V Translator

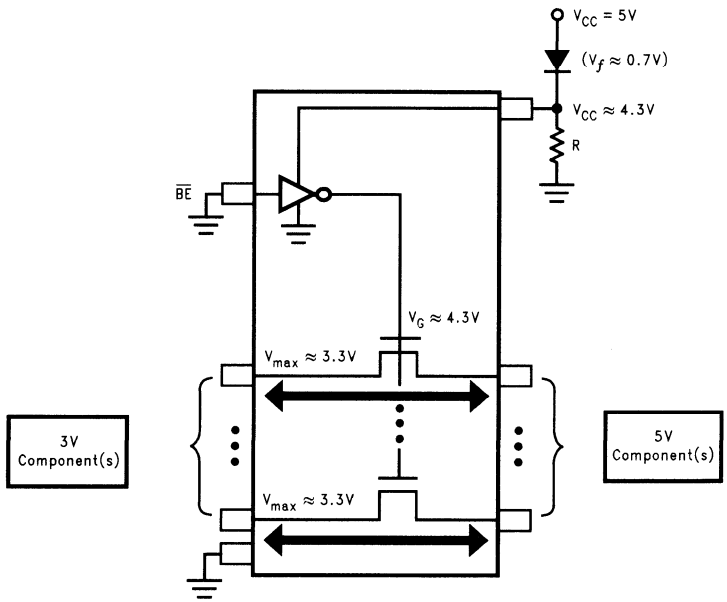
National Semiconductor
Application Note 996

The Bus Switch can be used as a bi-directional translator. It will interface 5V component(s) to 3V component(s), with negligible propagation delay ($T_{PD} \leq 250$ ps) and minimal power dissipation ($I_{CCQ} \leq 10\ \mu A$).

When the input voltage is equal to V_{CC}, the output voltage will be approximately 1V below V_{CC}. Increasing or decreasing V_{CC} will proportionally increase or decrease the output voltage by the same amount. This output limiting characteristic is the mechanism by which the Bus Switch can be used as a very efficient 5V-to-3V translator. To accomplish this, a diode is connected between the 5V power supply and the V_{CC} pin of the Bus Switch device. To preserve the low power design of the Bus Switch and provide optimal operation, select a low current turn on diode with a forward turn on voltage (V_f) of at least 0.7V. A resistor (R) is added, from V_{CC} to GND, to provide foward turn on current (I_f) for the diode. This is necessary to help the diode maintain a constant voltage drop. The value of R is dependent on the diode characteristics.

By dropping 0.7V down from the 5V power supply, $\approx$4.3V will be applied to the V_{CC} pin of a Bus Switch (5V − 0.7V = 4.3V). The gate of the switch will also therefore be at $\approx$4.3V. This coupled with the gate-to-source voltage drop of 1V, limits V_{OUT} to about 3.3V that can be used to interface signals in a 3V environment.

Simplified Diagram of a Bus Switch



TL/F/12461–1

*Bus Switch products include: 74LVX3L383—10-bit Low Power Bus-Exchange Switch
74LVX3L384—10-bit Low Power Bus Switch
74LVX3L384A—10-bit Low Power Extended Input Voltage Bus Switch

Bus Switches in the Presence of Undershoot

National Semiconductor
Application Note 997

Bus switch products have become a powerful tool in the modern desk top and portable personal computer. They have a number of positive attributes relative to standard bus transceivers. The bus switch parts are faster, consume a negligible amount of power, and introduce none of the noise issues associated with the typical high drive transceiver. In most applications, use of the bus switch will alleviate all the problems of the bus transceiver without creating new ones.

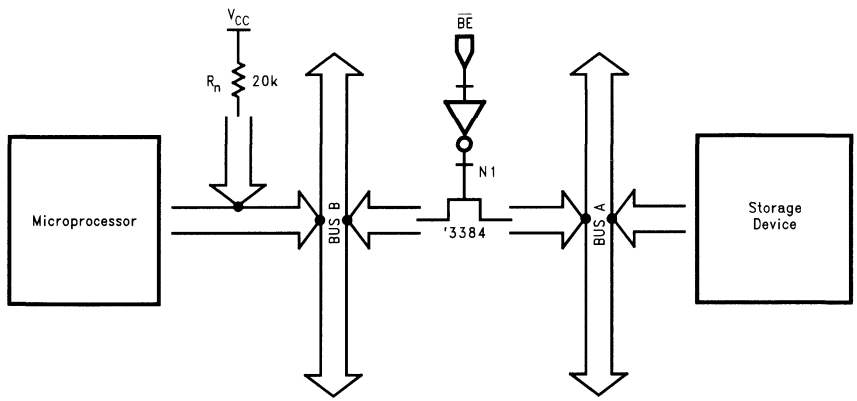
However, in the presence of large amounts of undershoot, typically associated with unterminated transmission lines, bus switches can misbehave. Most people's concern with undershoot pertains to latchup. The bus switch has been characterized for latchup and exceeds 500 mA, the limit of our tester. The issue at hand is data corruption for a small percentage of applications.

This application note will outline the specifics of the applications that can cause problems, list ways of avoiding the problem with system initiatives, and display the "Undershoot Hardened" design that is now available.

In the application of *Figure 1* the bus switch is used as a pathway for data from the A-Bus to move to the B-Bus, or vice versa. When the pin $\overline{BE}$ is a logic one, the two busses are expected to be isolated with any combination of activity that occurs on the two busses.

Assume, for the moment, that $\overline{BE}$ is a logic one and Bus-A is switching as data is written from one storage device to another. Also assume that Bus-A is either unterminated, or poorly terminated. If Bus-A transitions from a 0V to V_{CC}, the end of the bus will try to double to 2 * V_{CC}. This positive excursion, while probably not healthy for the system, will not bother the bus switch. A low going transition is a different story. In the low-going case, V_{CC} to 0V, the voltage swing will attempt to double to $-V_{CC}$. Their exists a clamp diode on the input of the bus switch that will limit the undershoot voltage to approximately -0.65V, but by then the fault has occurred.

For most functions found in family logic data books, a path from input to output exists where the signal must propagate through any number on inverters or complex logic gates. The bus switch is special in that its path is exceedingly simple. The data passes through a simple, but big, N-channel transistor. When $\overline{BE}$ is a "1", the gate of this transistor is at 0V. If the switching bus undershoots ground, the source of the transistor will be lower than the gate by $\approx$ 0.65V. The NMOS V_T for National Semiconductor's process is approximately 0.65V, thus enabling the bus switch to activate weakly and pass a logic "0" to a bus from which it is supposed to be isolated. If the B-Bus during the isolation, is passively pulled to a logic high as shown in *Figure 1.* The undershoot on the A-Bus may result in B-Bus's signals being pulled low. Were the B-Bus being actively driven, data corruption would be unlikely. The bias conditions during the undershoot makes the N-channel (N1), when it does turn on, weak in comparison to an output buffer.



TL/F/12462–1

FIGURE 1. '3384 Application

Sometimes, the standard solutions listed below are not feasible:

- Parallel or Thevinen terminate the bus—Can handle the increase in system power associated with these termination schemes.
- Series terminate the bus—Not enough room for the chip resistors on the printed circuit board.
- Integrate the series terminator within the peripheral storage devices, either as discrete resistors or intergated into the silicon drivers—The storage devices are being supplied by multiple third party vendors to existing industry standards.

When these system-type solutions are not possible, an "Undershoot Hardened" silicon approach should be pursued. One silicon technique, used by some vendors, is to increase the effective NMOS V_T of the bus switch. This is done by pumping the substrate to a voltage below ground. Data sheets with I_{CC} currents that are specified in mA, one well known vendor or has a limit of 3 mA, are likely to use this technique.

A product like the bus switch is likely to be used multiple times in a system, either to link various busses or to handle wide busses. Incurring a 3 mA penalty per usage can be very limiting for battery operated products. To solve the undershoot problem, without incurring an increase in I_{CC}, the 74LVX3L384A extended input voltage bus switch architecture was modified to that shown in *Figure 2.*

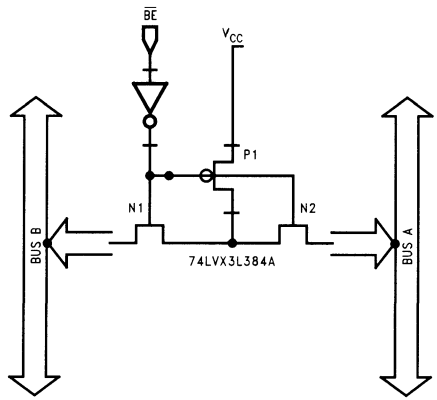
When $\overline{BE}$ is a logic "1", both N1 and N2 transistors are off and the PMOS (P1) on. The intermediate point between the N1 and N2 is actively pulled to V_{CC} by P1. When severe undershoot is present, the NMOS on the side with the undershoot may turn on. However, now P1 will hold the intermediate point high enough to prevent the opposite side NMOS from switching on by keeping $V_{GS} < V_{TN}$. This solution has been verified in the problematic applications to completely isolate the two busses.

Specification Changes for the 74LVX3L384A

- R_{ON} @ 0V — From 7Ω–10.5Ω
- R_{ON} @ 2.4V — From 15Ω–25Ω
- T_{PZL} — From 6.5 ns–6.7 ns

The "Undershoot Hardened" circuitry does force some datasheet specification changes. The changes include an increase in R_{ON} from using two FET's in series, and a marginal increase in T_{PZL} due to the extra capacitive load on the $\overline{BE}$ inverter. The marginal increase in phase delay through the bus switch as a result of RON's change, coupled with the ZL delta, should be attractive relative to a factor of 100 (3 μA–3 mA) increase in I_{CC}.

Many unattractive behaviors can result from neglecting transmission line theory. Use of the 74LVX3L384A should be considered as an aid to get through a marginal termination situation, not as a substitue for sound engineering practice.



TL/F/12462–2

FIGURE 2. 74LVX3L384A "Undershoot Hardened" Bus Switch

Section 7

LVX Family

Section 7 Contents

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National Semiconductor

LVX Family
Low Voltage CMOS Logic
(with 5V tolerant inputs)

Features	Advantages
5V tolerant inputs	Interfaces to 5V and 3V devices
Very low static (40 μA max I_{CCQ} for octals) and dynamic power	Saves power, extends battery life
Extended 2.0V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Balanced $\pm$4 mA output drive	Very low noise generation
SOIC and SSOPI/TSSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

National Semiconductor

74LVX00
Low Voltage Quad 2-Input NAND Gate

General Description

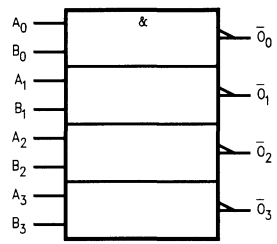
The LVX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

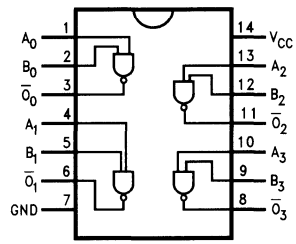
IEEE/IEC



TL/F/11551–3

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11551–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX00M 74LVX00MX	74LVX00SJ 74LVX00SJX	74LVX00MTC 74LVX00MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX00 T_A = +25°C			74LVX00 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX00 T_A = 25°C Typ	74LVX00 T_A = 25°C Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX00 T_A = +25°C Min	Typ	Max	74LVX00 T_A = −40°C to +85°C Min	Max	Units	C_L (pF)
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		5.4	10.1	1.0	12.5	ns	15
				7.9	13.6	1.0	16.0		50
		3.3 ±0.3		4.1	6.2	1.0	7.5		15
				6.6	9.7	1.0	11.0		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX00 T_A = +25°C Min	Typ	Max	74LVX00 T_A = −40°C to +85°C Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		19				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

National Semiconductor

74LVX02
Low Voltage Quad 2-Input NOR Gate

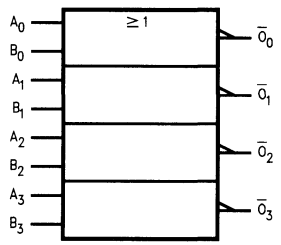
General Description

The LVX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol



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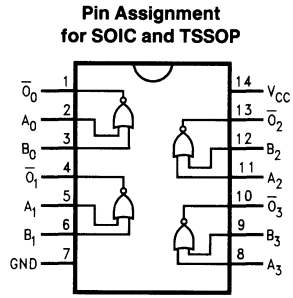
Connection Diagram



TL/F/11600–1

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX02M 74LVX02MX	74LVX02SJ 74LVX02SJX	74LVX02MTC 74LVX02MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta v$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX02 T_A = +25°C			74LVX02 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX02 T_A = 25°C		Units	Conditions C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX02 T_A = +25°C			74LVX02 T_A = −40°C to +85°C		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		5.9	10.7	1.0	13.5	ns	15
				8.4	14.2	1.0	17.0		50
		3.3 ±0.3		4.5	6.6	1.0	8.0		15
				7.0	10.1	1.0	11.5		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHm}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLm}|$

Capacitance

Symbol	Parameter	74LVX02 T_A = +25°C			74LVX02 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		15				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

National Semiconductor

74LVX04
Low Voltage Hex Inverter

General Description

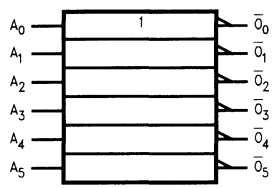
The LVX04 contains six inverters. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

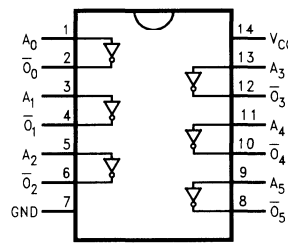
IEEE/IEC



TL/F/11601–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11601–1

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX04M 74LVX04MX	74LVX04SJ 74LVX04SJX	74LVX04MTC 74LVX04MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX04 T_A = +25°C			74LVX04 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX04 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX04 T_A = +25°C			74LVX04 T_A = −40°C to +85°C		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		5.4	10.1	1.0	12.5	ns	15
				7.9	13.6	1.0	16.0		50
		3.3 ±0.3		4.1	6.2	1.0	7.5		15
				6.6	9.7	1.0	11.0		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

Capacitance

Symbol	Parameter	74LVX04 T_A = +25°C			74LVX04 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6 \text{ (per Gate)}}$

National Semiconductor

74LVX08
Low Voltage Quad 2-Input AND Gate

General Description

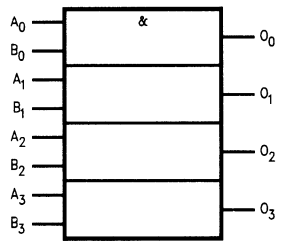
The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

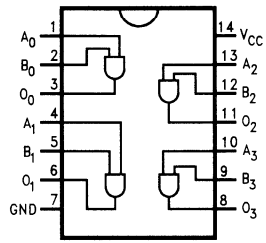
IEEE/IEC



TL/F/11602–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11602–1

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX08M 74LVX08MX	74LVX08SJ 74LVX08SJX	74LVX08MTC 74LVX08MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	240°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX08 T_A = +25°C			74LVX08 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX08 $T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX08 $T_A = +25°C$			74LVX08 $T_A = -40°C$ to $+85°C$		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		6.3	11.4	1.0	13.5	ns	15
				8.8	14.9	1.0	17.0		50
		3.3 ±0.3		4.8	7.1	1.0	8.5		15
				7.3	10.6	1.0	12.0		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX08 $T_A = +25°C$			74LVX08 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

National Semiconductor

74LVX14
Low Voltage Hex Inverter with Schmitt Trigger Input

General Description

The LVX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

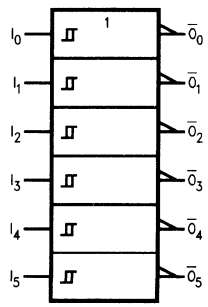
The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

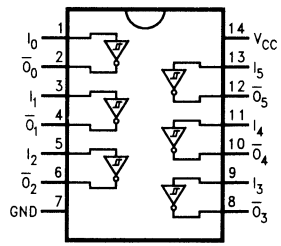
IEEE/IEC



TL/F/11603–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11603–1

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

Input	Output
A	$\overline{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX14M 74LVX14MX	74LVX14SJ 74LVX14SJX	74LVX14MTC 74LVX14MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX14 T_A = +25°C			74LVX14 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_t+	Positive Threshold	3.0			2.2		2.2	V		
V_t-	Negative Threshold	3.0	0.9			0.9		V		
V_H	Hysteresis	3.0	0.3		1.2	0.3	1.2	V		
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX14 $T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX14 $T_A = +25°C$			74LVX14 $T_A = -40°C$ to $+85°C$		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		8.7	16.3	1.0	19.5	ns	15
				11.2	19.8	1.0	23.0		50
		3.3 ±0.3		6.8	10.6	1.0	12.5		15
				9.3	14.1	1.0	16.0		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX14 $T_A = +25°C$			74LVX14 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		21				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6 \text{ (per Gate)}}$

National Semiconductor

74LVX32
Low Voltage Quad 2-Input OR Gate

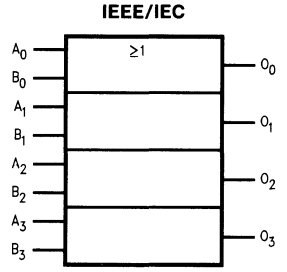
General Description

The LVX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

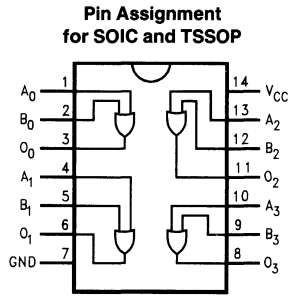
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol



TL/F/11604–2

Connection Diagram



TL/F/11604–1

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX32M 74LVX32MX	74LVX32SJ 74LVX32SJX	74LVX32MTC 74LVX32MTCX
NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX32 T_A = +25°C			74LVX32 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX32 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX32 T_A = +25°C			74LVX32 T_A = −40°C to +85°C		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		5.8	10.7	1.0	12.5	ns	15
				8.3	14.2	1.0	16.0		50
		3.3 ±0.3		4.4	6.6	1.0	7.5		15
				6.9	10.1	1.0	11.5		50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX32 T_A = +25°C			74LVX32 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		14				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

National Semiconductor

74LVX74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

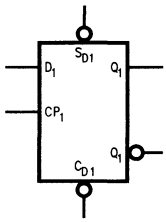
Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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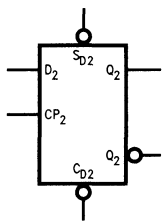
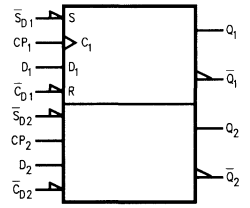


TL/F/11606–2

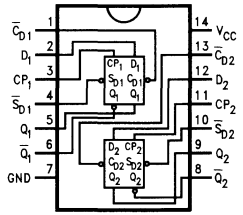
Connection Diagram

IEEE/IEC



TL/F/11606–4

Pin Assignment for SOIC and TSSOP



TL/F/11606–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX74M 74LVX74MX	74LVX74SJ 74LVX74SJX	74LVX74MTC 74LVX74MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX74 T_A = +25°C			74LVX74 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX74 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX74 T_A = +25°C			74LVX74 T_A = −40°C to +85°C		Units	C_L(pF)
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.7		7.3	15	1.0	18.5	ns	15
				9.8	18.5	1.0	22		50
		3.3 ±0.3		5.7	9.7	1.0	11.5		15
				8.2	13.2	1.0	15		50
t_{PLH}, t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.7		8.4	15.6	1.0	18.5	ns	15
				10.9	19.1	1.0	22		50
		3.3 ±0.3		6.6	10.1	1.0	12		15
				9.1	13.6	1.0	15.5		50
t_W	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	2.7	8.5			10		ns	
		3.3 ±0.3	6			7			
t_S	Setup Time D_n to CP_n	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_H	Hold Time D_n to CP_n	2.7	0.5			0.5		ns	
		3.3 ±0.3	0.5			0.5			
t_{rec}	Recovery Time $\overline{CP}_n$ or $\overline{S}_{Dn}$ to CP_n	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
f_{max}	Maximum Clock Frequency	2.7	55	135		50		MHz	15
			45	60		40			50
		3.3 ±0.3	95	145		80			15
			60	85		50			50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSLH} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX74			74LVX74		Units
		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		25				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$

National Semiconductor

74LVX86
Low Voltage Quad 2-Input Exclusive-OR Gate

General Description

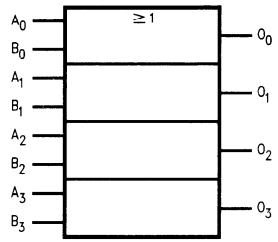
The LVX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

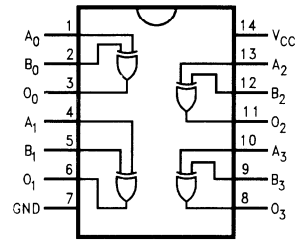
IEEE/IEC



TL/F/11605–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX86M 74LVX86MX	74LVX86SJ 74LVX86SJX	74LVX86MTC 74LVX86MTCX
See NS Package Number	M14A	M14D	MTC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX86 T_A = +25°C			74LVX86 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX86 $T_A = 25°C$ Typ	74LVX86 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX86 $T_A = +25°C$ Min	Typ	Max	74LVX86 $T_A = -40°C$ to $+85°C$ Min	Max	Units	C_L (pF)
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		7.5	14.5	1.0	17.5	ns	15
				10.0	18.0	1.0	21.0		50
		3.3 ±0.3		5.8	9.3	1.0	11.0		15
				8.3	12.8	1.0	14.5		50
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX86 $T_A = +25°C$ Min	Typ	Max	74LVX86 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

National Semiconductor

74LVX125
Low-Voltage Quad Buffer with TRI-STATE® Outputs

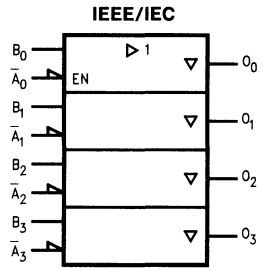
General Description

The LVX125 contains four independent non-inverting buffers with TRI-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol



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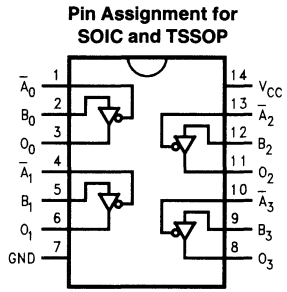
Connection Diagram



TL/F/12007–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX125M 74LVX125MX	74LVX125SJ 74LVX125SJX	74LVX125MTC 74LVX125MTCX
See NS Package Number	M14A	M14D	MTC14

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temp. Range (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta v$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX125 T_A = 25°C			74LVX125 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IH} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX125 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns.

AC Electrical Characteristics: See Section 2 Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX125 T_A = +25°C			74LVX125 T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time Data to Output	2.7		5.8	10.1	1.0	13.5	ns	C_L = 15 pF
				8.3	13.6	1.0	17.0		C_L = 50 pF
		3.3 ±0.3		4.4	6.2	1.0	8.5		C_L = 15 pF
				6.9	9.7	1.0	12.0		C_L = 50 pF
t_{PZH}, t_{PZL}	Output Enable Time	2.7		5.3	9.3	1.0	12.5	ns	C_L = 15 pF, R_L = 1 kΩ
				7.8	12.8	1.0	16.0		C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		4.0	5.6	1.0	7.5		C_L = 15 pF, R_L = 1 kΩ
				6.5	9.1	1.0	11.0		C_L = 50 pF, R_L = 1 kΩ
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7		10.0	15.7	1.0	19.0	ns	C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		8.3	11.2	1.0	13.0		C_L = 50 pF, R_L = 1 kΩ
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C_L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX125 T_A = 25°C			74LVX125 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4.0	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		14				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per bit)}}$

7

National Semiconductor

74LVX138
Low Voltage 1-of-8 Decoder/Demultiplexer

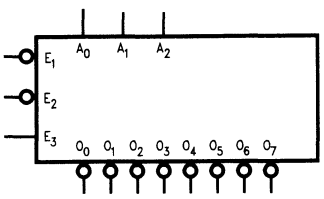
General Description

The LVX138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVX138 devices or a 1-of-32 decoder using four LVX138 devices and one inverter.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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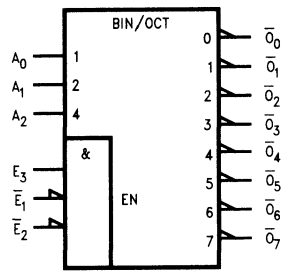
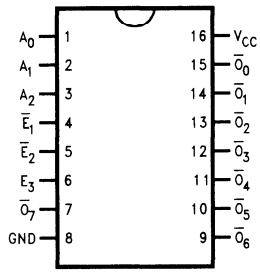
IEEE/IEC



TL/F/11615–3

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11615–2

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX138M 74LVX138MX	74LVX138SJ 74LVX138SJX	74LVX138MTC 74LVX138MTCX
See NS Package Number	M16A	M16D	MTC16

Functional Description

The LVX138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The LVX138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

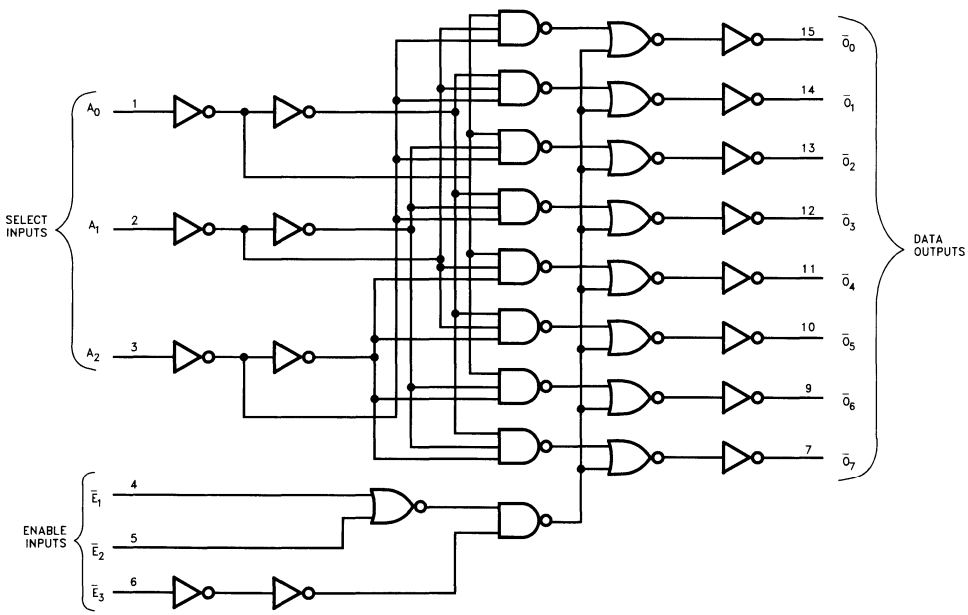
The LVX138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta v$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX138 T_A = +25°C			74LVX138 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX138 $T_A = 25°C$ Typ	74LVX138 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX138 $T_A = +25°C$ Min	Typ	Max	74LVX138 $T_A = -40°C$ to $+85°C$ Min	Max	Units	C_L (pF)
t_{PLH} t_{PHL}	Propagation Delay Time A_n to $\overline{O}_n$	2.7		7.1	13.8	1.0	16.5	ns	15
				9.6	17.3	1.0	20.0		50
		3.3 ±0.3		5.5	8.8	1.0	10.5		15
				8.0	12.3	1.0	14.0		50
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.7		8.8	16.0	1.0	18.5	ns	15
				11.3	19.5	1.0	22.0		50
		3.3 ±0.3		6.9	10.4	1.0	11.5		15
				9.4	13.9	1.0	15.0		50
t_{PLH} t_{PHL}	Propagation Delay Time E_3 to $\overline{O}_n$	2.7		8.7	16.3	1.0	19.5	ns	15
				11.2	19.8	1.0	23.0		50
		3.3 ±0.3		6.8	10.6	1.0	12.5		15
				9.3	14.1	1.0	16.0		50
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX138 $T_A = +25°C$ Min	Typ	Max	74LVX138 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		34				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

National Semiconductor

74LVX157
Low Voltage Quad 2-Input Multiplexer

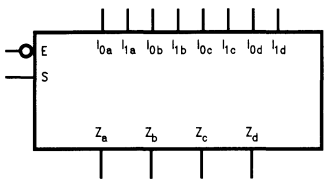
General Description

The LVX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVX157 can also be used as a function generator.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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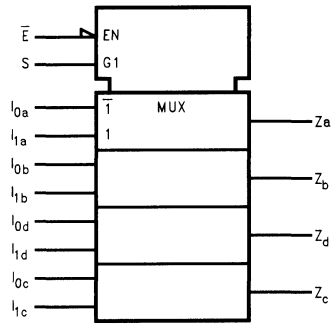
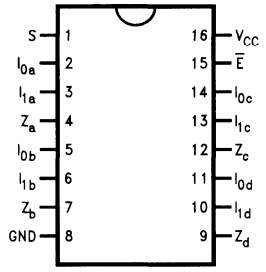


TL/F/11608–4

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11608–2

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX157M 74LVX157MX	74LVX157SJ 74LVX157SJX	74LVX157MTC 74LVX157MTCX
See NS Package Number	M16A	M16D	MTC16

Functional Description

The LVX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

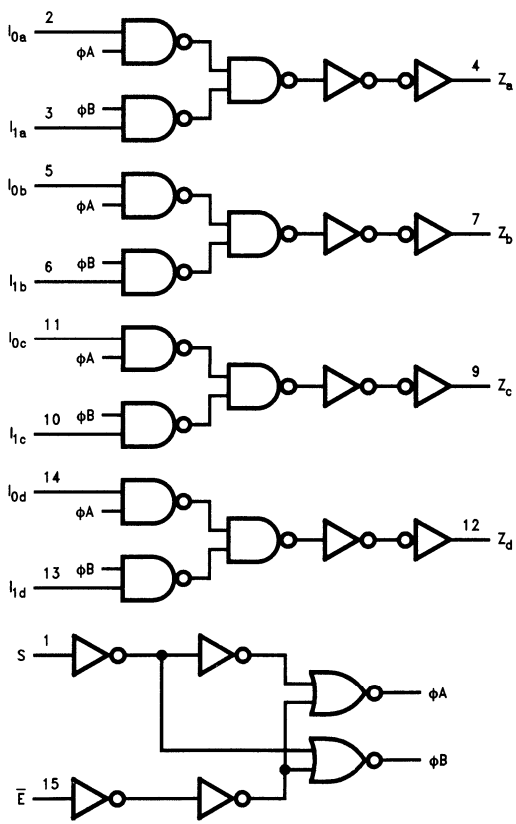
$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the LVX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



TL/F/11608–3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX157 T_A = +25°C			74LVX157 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX157 $T_A = 25°C$ Typ	74LVX157 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX157 $T_A = +25°C$ Min	Typ	Max	74LVX157 $T_A = -40°C$ to $+85°C$ Min	Max	Units	C_L (pF)
t_{PLH}, t_{PHL}	Propagation Delay Time I_n to Z_n	2.7		6.6	12.5	1.0	15.5	ns	15
				9.1	16.0	1.0	19.0		50
		3.3 ±0.3		5.1	7.9	1.0	9.5		15
				7.6	11.4	1.0	13.0		50
t_{PLH}, t_{PHL}	Propagation Delay Time S to Z_n	2.7		8.9	16.9	1.0	20.5	ns	15
				11.4	20.4	1.0	24.0		50
		3.3 ±0.3		7.0	11.0	1.0	13.0		15
				9.5	14.5	1.0	16.5		50
t_{PLH}, t_{PHL}	Propagation Delay Time $\overline{E}$ to Z_n	2.7		9.1	17.6	1.0	20.5	ns	15
				11.6	21.1	1.0	24.0		50
		3.3 ±0.3		7.2	11.5	1.0	13.5		15
				9.7	15.0	1.0	17.0		50
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

Capacitance

Symbol	Parameter	74LVX157 $T_A = +25°C$ Min	Typ	Max	74LVX157 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		20				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

National Semiconductor

74LVX174
Low Voltage Hex D Flip-Flop with Master Reset

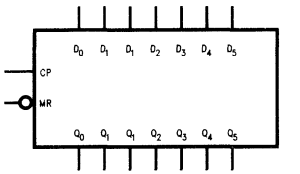
General Description

The LVX174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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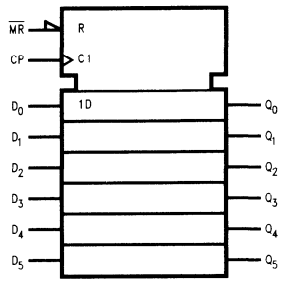
IEEE/IEC



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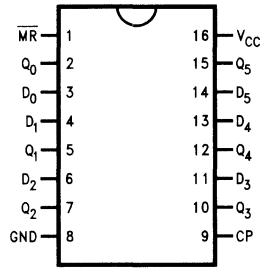
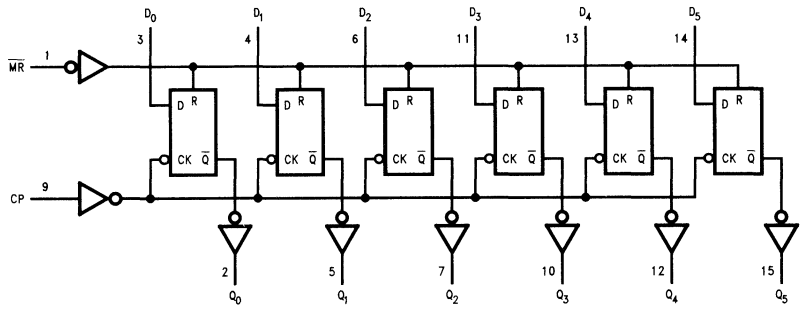
Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11607–2

Logic Diagram



TL/F/11607–3

Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX174M 74LVX174MX	74LVX174SJ 74LVX174SJX	74LVX174MTC 74LVX174MTCX
See NS Package Number	M16A	M16D	MTC16

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX174 T_A = +25°C			74LVX174 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX174 $T_A = 25°C$ Typ	74LVX174 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX174 $T_A = +25°C$ Min	Typ	Max	74LVX174 $T_A = -40°C$ to $+85°C$ Min	Max	Units	C_L (pF)
t_{PLH} t_{PHL}	Propagation Delay Time CP to Q_n	2.7		7.6	14.5	1.0	17.5	ns	15
				10.1	18.0	1.0	21.0		50
		3.3 ±0.3		5.9	9.3	1.0	11.0		15
				8.4	12.8	1.0	14.5		50
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7		7.9	15.0	1.0	18.5	ns	15
				10.4	18.5	1.0	22.0		50
		3.3 ±0.3		6.2	9.7	1.0	11.5		15
				8.7	13.2	1.0	15.0		50
t_S	Setup Time D_n to CP	2.7	7.5			8.5		ns	
		3.3 ±0.3	5.0			6.0			
t_H	Hold Time D_n to CP	2.7	0			0			
		3.3 ±0.3	0			0			
t_{REM}	Removal Time $\overline{MR}$ to CP	2.7	4.5			4.5		ns	
		3.3 ±0.3	3.0			3.0			
t_W	Clock Pulse Width	2.7	6.5			7.5			
		3.3 ±0.3	5.0			5.0			
t_W	$\overline{MR}$ Pulse Width	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
f_{MAX}	Maximum Clock Frequency	2.7	65	130		55		MHz	15
			45	60		40			50
		3.3 ±0.3	115	180		95			15
			65	95		55			50
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX174 $T_A = +25°C$ Min	Typ	Max	74LVX174 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		29				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per F/F)}}$

National Semiconductor

74LVX240
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

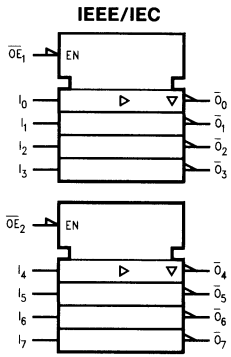
General Description

The LVX240 is an octal inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

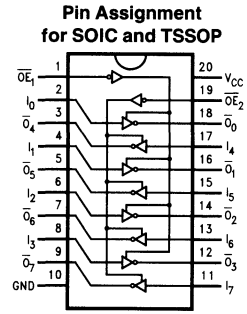
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol



TL/F/11609–2

Connection Diagram



TL/F/11609–1

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX240M 74LVX240MX	74LVX240SJ 74LVX240SJX	74LVX240MTC 74LVX240MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	180 mW

Note: *Absolute Maximum Ratings are those values beyond which the safety to the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX240 T_A = +25°C			74LVX240 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX240 $T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX240 $T_A = +25°C$			74LVX240 $T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		5.7	10.1	1.0	12.5	ns	$C_L = 15$ pF
				8.2	13.6	1.0	16.0		$C_L = 50$ pF
		3.3 ±0.3		4.3	6.2	1.0	7.5		$C_L = 15$ pF
				6.8	9.7	1.0	11.0		$C_L = 50$ pF
t_{PZL}, t_{PZH}	TRI-STATE Output Enable Time	2.7		7.1	13.8	1.0	16.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
				9.6	17.3	1.0	20.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		5.5	8.8	1.0	10.5		$C_L = 15$ pF, $R_L = 1$ kΩ
				8.0	12.3	1.0	14.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ}, t_{PHZ}	TRI-STATE Output Disable Time	2.7		11.6	16.0	1.0	19.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		9.7	11.4	1.0	13.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	$C_L = 50$ pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX240 $T_A = +25°C$			74LVX240 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		17	10			pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$

National Semiconductor

74LVX244
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

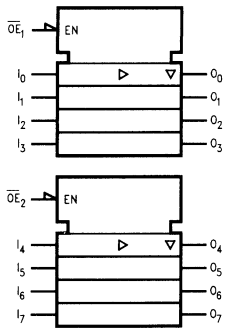
The LVX244 is an octal non-inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbol

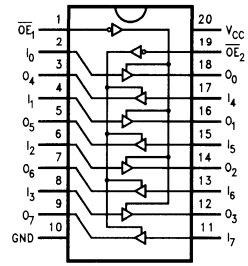
IEEE/IEC



TL/F/11552–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11552–1

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX244M 74LVX244MX	74LVX244SJ 74LVX244SJX	74LVX244MTC 74LVX244MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_o)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX244 T_A = +25°C			74LVX244 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX244 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methdology

Symbol	Parameter	V_{CC} (V)	74LVX244 T_A = +25°C			74LVX244 T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7		6.1	11.4	1.0	13.5	ns	C_L = 15 pF
				8.6	14.9	1.0	17.0		C_L = 50 pF
		3.3 ±0.3		4.7	7.1	1.0	8.5		C_L = 15 pF
				7.2	10.6	1.0	12.0		C_L = 50 pF
t_{PZL}, t_{PZH}	TRI-STATE Output Enable Time	2.7		7.1	13.8	1.0	16.5	ns	C_L = 15 pF, R_L = 1 kΩ
				9.6	17.3	1.0	20.0		C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		5.5	8.8	1.0	10.5		C_L = 15 pF, R_L = 1 kΩ
				8.0	12.3	1.0	14.0		C_L = 50 pF, R_L = 1 kΩ
t_{PLZ}, t_{PHZ}	TRI-STATE Output Disable Time	2.7		11.6	16.0	1.0	19.0	ns	C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		9.7	11.4	1.0	13.0		
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C_L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX244 T_A = +25°C			74LVX244 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		19				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$

National Semiconductor

74LVX245
Low Voltage Octal Bidirectional Transceiver

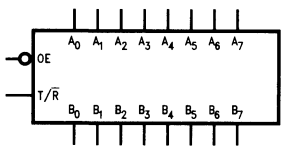
General Description

The LVX245 contains eight non-inverting bidirectional buffers is intended for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH-Z condition.

Features

- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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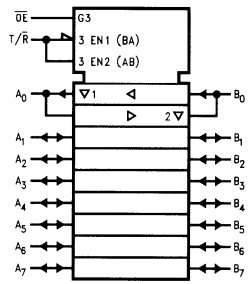
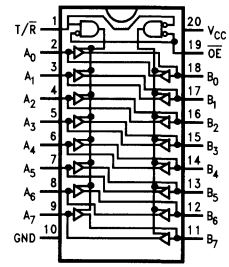


TL/F/11597–5

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11597–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE® Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX245M 74LVX245MX	74LVX245SJ 74LVX245SJX	74LVX245MTC 74LVX245MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_I = −0.5V	−20 mA
DC Input Voltage T/$\overline{R}$, $\overline{OE}$ (V_I)	−0.5V to 7V
DC Diode Current (I_{OK}) V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Bus I/O Voltage ($V_{I/O}$)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage T/$\overline{R}$, $\overline{OE}$ (V_I)	0V to 5.5V
Bus I/O Voltage ($V_{I/O}$)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX245 T_A = +25°C			74LVX245 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX245 $T_A = 25°C$ Typ	74LVX245 $T_A = 25°C$ Limit	Units	Conditions C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX245 $T_A = +25°C$ Min	Typ	Max	74LVX245 $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay Time	2.7		6.1	10.7	1.0	13.5	ns	$C_L = 15$ pF
				8.6	14.2	1.0	17.0		$C_L = 50$ pF
		3.3 ±0.3		4.7	6.8	1.0	8.0		$C_L = 15$ pF
				7.2	10.1	1.0	11.5		$C_L = 50$ pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	2.7		9.0	16.9	1.0	20.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
				11.5	20.4	1.0	24.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ± 0.3		7.1	11.0	1.0	13.0		$C_L = 15$ pF, $R_L = 1$ kΩ
				9.6	14.5	1.0	16.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	2.7		11.5	18.0	1.0	21.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		9.6	12.8	1.0	14.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	$C_L = 50$ pF (Note 1)

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX245 $T_A = +25°C$ Min	Typ	Max	74LVX245 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance T/$\overline{R}$, $\overline{OE}$		4	10		10	pF
$C_{I/O}$	Output Capacitance A_n, B_n		8				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		21				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$

National Semiconductor

74LVX273
Low Voltage Octal D Flip-Flop

General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

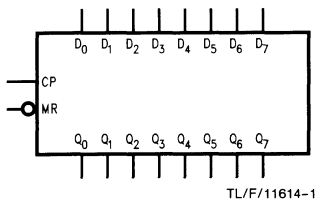
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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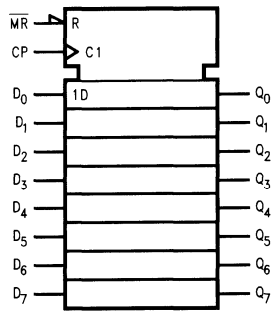
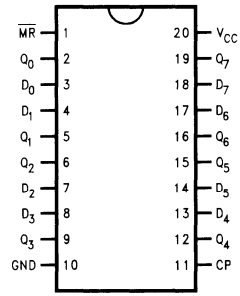
IEEE/IEC



TL/F/11614–4

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11614–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

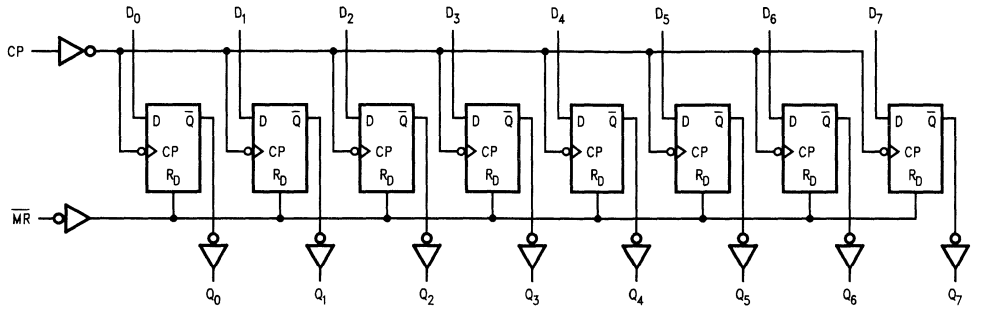
	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX273M 74LVX273MX	74LVX273SJ 74LVX273SJX	74LVX273MTC 74LVX273MTCX
See NS Package Number	M20B	M20D	MTC20

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11614–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX273 T_A = +25°C			74LVX273 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE® Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX273 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input t_r = t_f = 3 ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX273 $T_A = +25°C$			74LVX273 $T_A = -40°C$ to $+85°C$		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time CP to Q_n	2.7		9.0	16.9	1.0	20.5	ns	15
				11.5	20.4	1.0	24.0		50
		3.3 ±0.3		7.1	11.0	1.0	13.0		15
				9.6	14.5	1.0	16.5		50
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7		9.3	17.8	1.0	20.5	ns	15
				11.8	21.1	1.0	24.0		50
		3.3 ±0.3		7.3	11.5	1.0	13.5		15
				9.8	15.0	1.0	17.0		50
t_S	Setup Time D_n to CP	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_H	Hold Time D_n to CP	2.7	1.0			1.0		ns	
		3.3 ±0.3	1.0			1.0			
t_{REM}	Removal Time $\overline{MR}$ to CP	2.7	4.0			4.0		ns	
		3.3 ±0.3	2.5			2.5			
t_W	Clock Pulse Width	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_W	$\overline{MR}$ Pulse Width	2.7	7.5			8.5		ns	
		3.3 ±0.3	5.0			6.0			
f_{MAX}	Maximum Clock Frequency	2.7	55	110		45		MHz	15
			45	60		40			50
		3.3 ±0.3	95	150		80			15
			60	90		50			50
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX273 $T_A = +25°C$			74LVX273 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		31				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$

National Semiconductor

74LVX373
Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

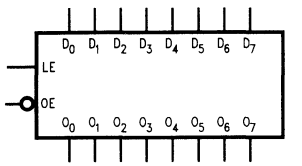
General Description

The LVX373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

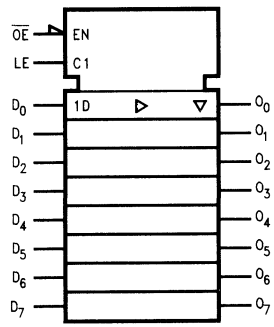
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



TL/F/11613–1

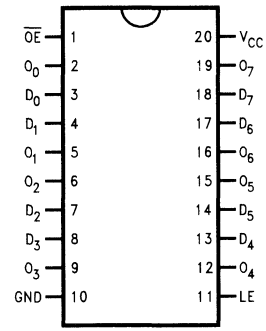
IEEE/IEC



TL/F/11613–4

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11613–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX373M 74LVX373MX	74LVX373SJ 74LVX373SJX	74LVX373MTC 74LVX373MTCX
See NS Package Number	M20B	M20D	MTC20

Functional Description

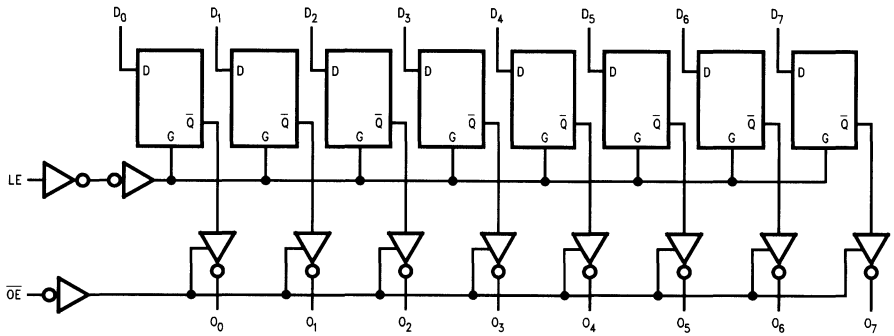
The LVX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/11613–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX373 T_A = +25°C			74LVX373 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX373 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX373 T_A = +25°C			74LVX373 T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time D_n to O_n	2.7		7.7	15.0	1.0	18.5	ns	C_L = 15 pF
				10.2	18.5	1.0	22.0		C_L = 50 pF
		3.3 ±0.3		6.0	9.7	1.0	11.5		C_L = 15 pF
				8.5	13.2	1.0	15.0		C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time LE to O_n	2.7		7.5	14.5	1.0	17.5	ns	C_L = 15 pF
				10.0	18.0	1.0	21.0		C_L = 50 pF
		3.3 ±0.3		5.8	9.3	1.0	11.0		C_L = 15 pF
				8.3	12.8	1.0	14.5		C_L = 50 pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	2.7		7.7	15.0	1.0	18.5	ns	C_L = 15 pF, R_L = 1 kΩ
				10.2	18.5	1.0	22.0		C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		6.0	9.7	1.0	11.5		C_L = 15 pF, R_L = 1 kΩ
				8.5	13.2	1.0	15.0		C_L = 50 pF, R_L = 1 kΩ
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	2.7		9.8	18.0	1.0	21.0	ns	C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		8.2	12.8	1.0	14.5		C_L = 50 pF, R_L = 1 kΩ
t_W	LE Pulse Width, HIGH	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
t_S	Setup Time, D_n to LE	2.7	6.0			6.0		ns	
		3.3 ±0.3	4.0			4.0			
t_H	Hold Time, D_n to LE	2.7	1.0			1.0		ns	
		3.3 ±0.3	1.0			1.0			
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C_L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX373 $T_A = +25°C$			74LVX373 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		27				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per Latch)}}$

National Semiconductor

74LVX374
Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

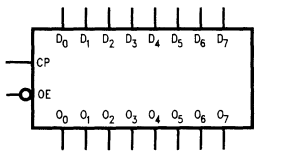
General Description

The LVX374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

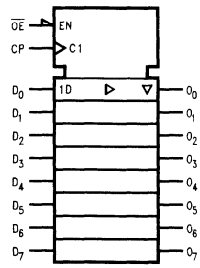
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



TL/F/11612–1

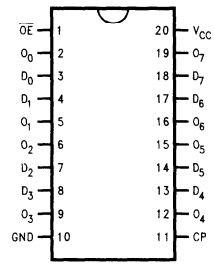
IEEE/IEC



TL/F/11612–4

Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX374M 74LVX374MX	74LVX374SJ 74LVX374SJX	74LVX374MTC 74LVX374MTCX
See NS Package Number	M20B	M20D	MTC20

7

Functional Description

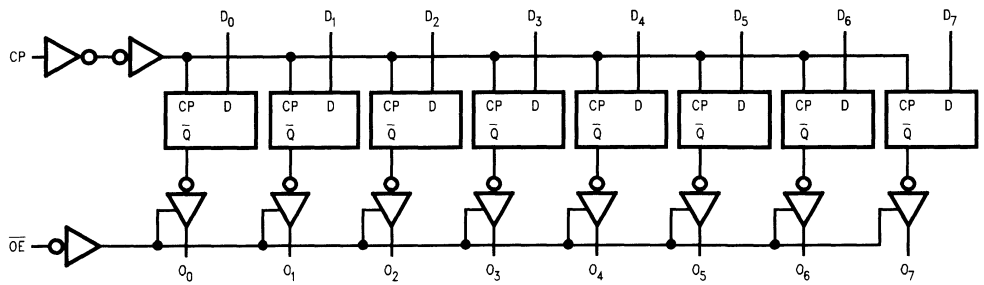
The LVX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11612–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_o)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX374 T_A = +25°C			74LVX374 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX374 $T_A = 25°C$ Typ	74LVX374 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX374 $T_A = +25°C$ Min	Typ	Max	74LVX374 $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay Time CP to O_n	2.7		8.5	16.3	1.0	19.5	ns	$C_L = 15$ pF
				11.0	19.8	1.0	23.0		$C_L = 50$ pF
		3.3 ±0.3		6.7	10.6	1.0	12.5		$C_L = 15$ pF
				9.2	14.1	1.0	16.0		$C_L = 50$ pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	2.7		7.6	14.5	1.0	17.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
				10.1	18.0	1.0	21.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		5.9	9.3	1.0	11.0		$C_L = 15$ pF, $R_L = 1$ kΩ
				8.4	12.8	1.0	14.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	2.7		11.5	18.5	1.0	22.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		9.6	13.2	1.0	15.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_W	CP Pulse Width	2.7	7.5			8.0		ns	
		3.3 ±0.3	5.0			5.5			
t_S	Setup Time D_n to CP	2.7	6.5			6.5		ns	
		3.3 ±0.3	4.5			4.5			
t_H	Hold Time D_n to CP	2.7	2.0			2.0		ns	
		3.3 ±0.3	2.0			2.0			
f_{MAX}	Maximum Clock Frequency	2.7	60	115		50		MHz	$C_L = 15$ pF
			45	60		40			$C_L = 50$ pF
		3.3 ±0.3	100	160		85			$C_L = 15$ pF
			60	95		55			$C_L = 50$ pF
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	$C_L = 50$ pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX374 $T_A = +25°C$ Min	Typ	Max	74LVX374 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		32				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$

National Semiconductor

74LVX573
Low Voltage Octal Latch with TRI-STATE® Outputs

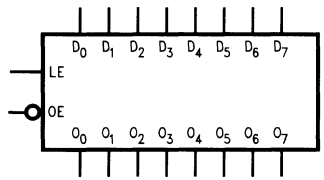
General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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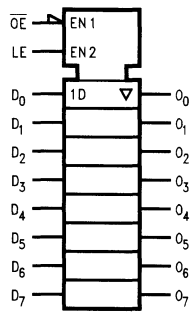
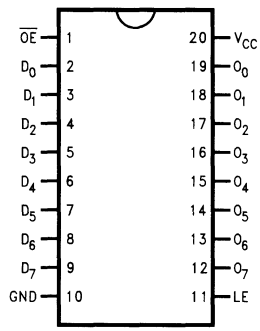
IEEE/IEC



TL/F/11616–4

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11616–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVX573M 74LVX573MX	74LVX573SJ 74LVX573SJX	74LVX573MTC 74LVX573MTCX
See NS Package Number	M20B	M20D	MTC20

Functional Description

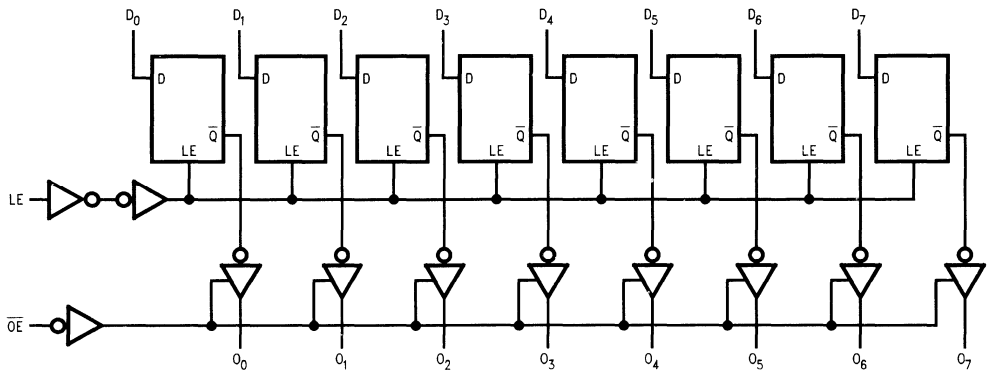
The LVX573 contains eight D-type latches with TRI-STATE® output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE® buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX573 T_A = +25°C			74LVX573 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX573 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX573 T_A = +25°C			74LVX573 T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time D_n to O_n	2.7		7.6	14.5	1.0	17.5	ns	C_L = 15 pF
				10.1	18.0	1.0	21.0		C_L = 50 pF
		3.3 ±0.3		5.9	9.3	1.0	11.0		C_L = 15 pF
				8.4	12.8	1.0	14.5		C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time LE to O_n	2.7		8.2	15.6	1.0	18.5	ns	C_L = 15 pF
				10.7	19.1	1.0	22.0		C_L = 50 pF
		3.3 ±0.3		6.4	10.1	1.0	12.0		C_L = 15 pF
				8.9	13.6	1.0	15.5		C_L = 50 pF
t_{PZL} t_{PZH}	TRI-STATE® Output Enable Time	2.7		7.8	15.0	1.0	18.5	ns	C_L = 15 pF, R_L = 1 kΩ
				10.3	18.5	1.0	22.0		C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		6.1	9.7	1.0	12.0		C_L = 15 pF, R_L = 1 kΩ
				8.6	13.2	1.0	15.5		C_L = 50 pF, R_L = 1 kΩ
t_{PLZ} t_{PHZ}	TRI-STATE® Output Disable Time	2.7		12.1	19.1	1.0	22.0	ns	C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		10.1	13.6	1.0	15.5		C_L = 50 pF, R_L = 1 kΩ
t_W	LE Pulse Width	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
t_S	Setup Time D_n to LE	2.7	5.0			5.0		ns	
		3.3 ±0.3	3.5			3.5			
t_H	Hold Time D_n to LE	2.7	1.5			1.5		ns	
		3.3 ±0.3	1.5			1.5			
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C_L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

Capacitance

Symbol	Parameter	74LVX573			74LVX573		Units
		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		27				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$

Section 8

LVQ Family

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National Semiconductor

LVQ Family
Low Voltage Quiet CMOS Logic

Features	Advantages
Extended 2.0V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Very low static (40 μA max I_{CCQ} for octals) and dynamic power	Saves power, extends battery life
Balanced $\pm$12 mA output drive	Drives transmission lines down to 75Ω
SOIC and QSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

National Semiconductor

74LVQ00
Low Voltage Quad 2-Input NAND Gate

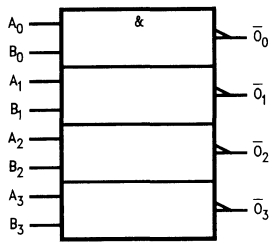
General Description

The LVQ00 contains four 2-input NAND gates.

Features

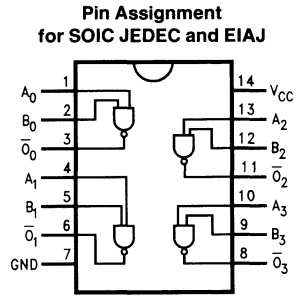
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbol



TL/F/11341–1

Connection Diagram



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Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ00SC 74LVQ00SCX	74LVQ00SJ 74LVQ00SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ00 T_A = +25°C	74LVQ00 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ00 $T_A = +25°C$ Typ	74LVQ00 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6		−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6	2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0	V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−1.0	V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0	V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8	V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ00 $T_A = +25°C$, $C_L = 50$ pF			74LVQ00 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	2.0	8.4	13.4	2.0	14.0	ns
		3.3 ± 0.3	2.0	7.0	9.5	2.0	10.0	
t_{PHL}	Propagation Delay	2.7	1.5	6.6	11.3	1.0	12.0	ns
		3.3 ± 0.3	1.5	5.5	8.0	1.0	8.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ± 0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	22	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ02
Low Voltage Quad 2-Input NOR Gate

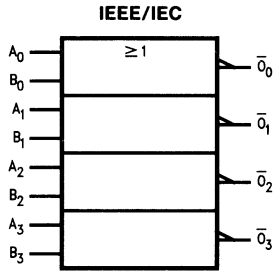
General Description

The LVQ02 contains four, 2-input NOR gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbol



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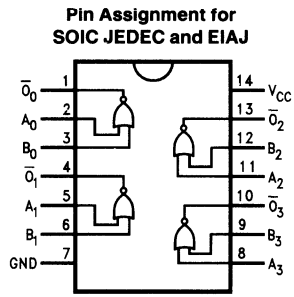
Connection Diagram



TL/F/11342–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ02SC 74LVQ02SCX	74LVQ02SJ 74LVQ02SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ02 T_A = +25°C		74LVQ02 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ02 $T_A = +25°C$		74LVQ02 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.7	−1.0		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Waveforms and Output Load

Symbol	Parameter	V_{CC} (V)	74LVQ02 $T_A = +25°C$, $C_L = 50$ pF			74LVQ02 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	1.5	6.0	10.6	1.0	12.0	ns
		3.3 ±0.3	1.5	5.0	7.5	1.0	8.0	
t_{PHL}	Propagation Delay	2.7	1.5	6.0	10.6	1.0	12.0	ns
		3.3 ±0.3	1.5	5.0	7.5	1.0	8.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	20	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ04
Low Voltage Hex Inverter

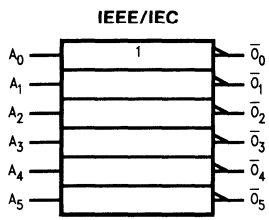
General Description

The LVQ04 contains six inverters.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC Products are available for Military/ Aerospace Applications

Logic Symbol



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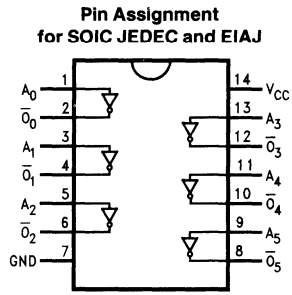
Connection Diagram



TL/F/11343–2

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ04SC 74LVQ04SCX	74LVQ04SJ 74LVQ04SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ04 T_A = +25°C	74LVQ04 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ04 $T_A = +25°C$ Typ	74LVQ04 $T_A = +25°C$ Guaranteed Limits	74LVQ04 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.8	1.1		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.8	−1.1		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}) 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ04 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ04 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay	2.7	1.5	5.4	12.7	1.0	14.0	ns
		3.3 ±0.3	1.5	4.5	9.0	1.0	10.0	
t_{PHL}	Propagation Delay	2.7	1.5	5.4	12.0	1.0	12.0	ns
		3.3 ±0.3	1.5	4.5	8.5	1.0	9.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ08
Low Voltage Quad 2-Input AND Gate

General Description

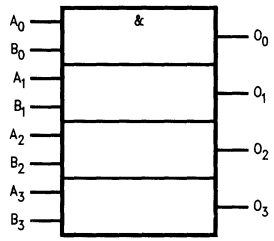
The LVQ08 contains four, 2-input AND gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbol

IEEE/IEC



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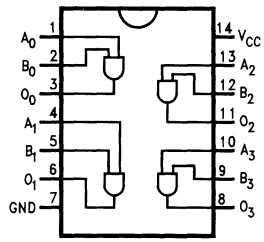
Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



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Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ08SC 74LVQ08SCX	74LVQ08SJ 74LVQ08SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ08 T_A = +25°C		74LVQ08 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ08 $T_A = +25°C$ Typ	74LVQ08 $T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ08 $T_A = +25°C$, $C_L = 50$ pF			74LVQ08 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	9.0 7.5	13.4 9.5	1.0 1.0	14.0 10.0	ns
t_{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	8.4 7.0	12.0 8.5	1.0 1.0	13.0 9.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ14
Low Voltage Hex Inverter with Schmitt Trigger Input

General Description

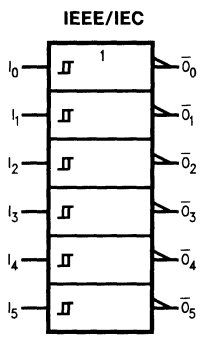
The LVQ14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVQ14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Logic Symbol



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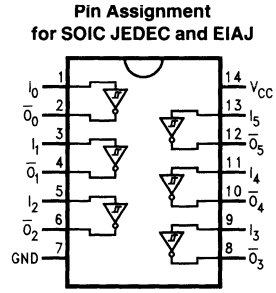
Connection Diagram



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Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

Input	Output
A	$\overline{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ14SC 74LVQ14SCX	74LVQ14SJ 74LVQ14SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ14 T_A = +25°C	74LVQ14 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2	V	T_A = Worst Case
V_{t-}	Minimum Negative Threshold	3.0		0.5	0.5	V	T_A = Worst Case

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ14 $T_A = +25°C$		74LVQ14 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{h(max)}$	Maximum Hysteresis	3.0		1.2	1.2	V	T_A = Worst Case
$V_{h(min)}$	Minimum Hysteresis	3.0		0.3	0.3	V	T_A = Worst Case
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V_{IN} = V_{CC} or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.9	1.1		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.8	−1.1		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.3	2.0		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ14 $T_A = +25°C$, C_L = 50 pF			74LVQ14 $T_A = -40°C$ to $+85°C$, C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	1.5	11.4	19.0	1.5	21.0	ns
		3.3 ±0.3	1.5	9.5	13.5	1.5	15.0	
t_{PHL}	Propagation Delay	2.7	1.5	9.0	16.2	1.5	19.0	ns
		3.3 ±0.3	1.5	7.5	11.5	1.5	13.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	20	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ32
Low Voltage Quad 2-Input OR Gate

General Description

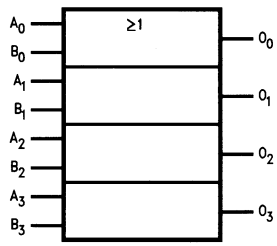
The LVQ32 contains four, 2-input OR gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Logic Symbol

IEEE/IEC



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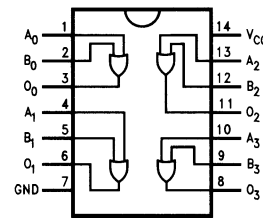
Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



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Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ32SC 74LVQ32SCX	74LVQ32SJ 74LVQ32SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ32 T_A = +25°C	74LVQ32 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ32 $T_A = +25°C$		74LVQ32 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ32 $T_A = +25°C$, $C_L = 50$ pF			74LVQ32 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	1.5	8.4	12.7	1.5	14.0	ns
		3.3 ±0.3	1.5	7.0	9.0	1.5	10.0	
t_{PHL}	Propagation Delay	2.7	1.5	8.4	12.0	1.0	13.0	ns
		3.3 ±0.3	1.5	7.0	8.5	1.5	9.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

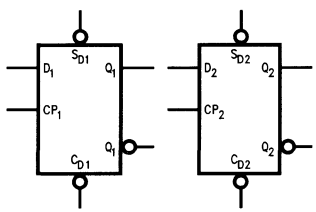
The LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Logic Symbols



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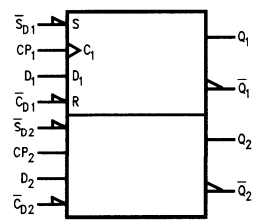
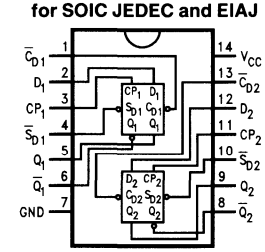
IEEE/IEC



TL/F/11347–3

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



TL/F/11347–4

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

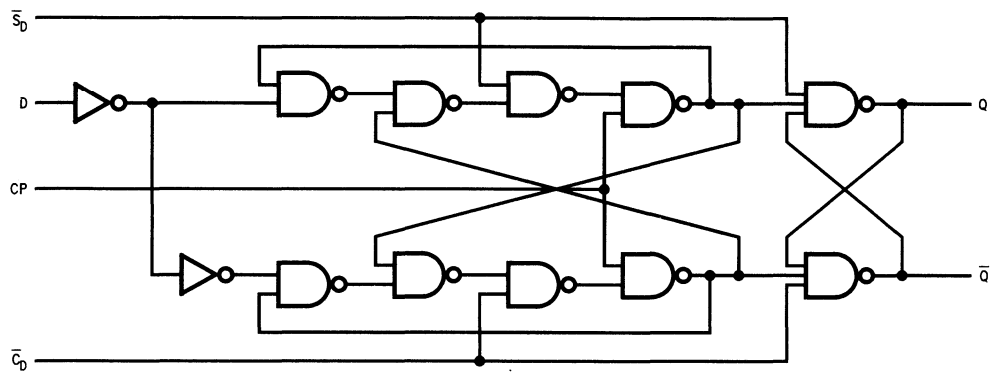
	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ74SC 74LVQ74SCX	74LVQ74SJ 74LVQ74SJX
See NS Package Number	M14A	M14D

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



TL/F/11347–6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteritics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ74 T_A = +25°C		74LVQ74 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ74 $T_A = +25°C$ Typ	74LVQ74 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6		−25	mA	V_{OHD} − 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6	2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.2	0.8	V	(Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.2	−0.8	V	(Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2 and 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}, 0V to threshold (V_{IHD}, f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ74 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ74 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	50 100	100 125		40 95		MHz
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	16.9 12.0	3.5 2.5	19.0 13.0	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n	2.7 3.3 ±0.3	4.0 4.0	12.6 10.5	16.9 12.0	3.5 3.5	19.0 13.5	ns
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.7 3.3 ±0.3	4.5 4.5	9.6 8.0	19.0 13.5	4.0 4.0	23.0 16.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.7 3.3 ±0.3	3.5 3.5	9.6 8.0	19.7 14.0	3.5 3.5	21.0 14.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ74		74LVQ74	Units
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	
			Typ	Guaranteed Minimum		
t_s	Set-up Time, HIGH or LOW	2.7	1.8	5.0	6.5	ns
		3.3 ±0.3	1.5	4.0	4.5	
t_H	Hold Time, HIGH or LOW D_n to CP_n	2.7	−2.4	0.5	0.5	ns
		3.3 ±0.3	−2.0	0.5	0.5	
t_W	Pulse Width	2.7	3.6	7.0	10.0	ns
		3.3 ±0.3	3.0	5.5	7.0	
t_{rec}	Recovery Time	2.7	−3.0	0	0	ns
		3.3 ±0.3	−2.5	0	0	

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	25	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ86
Low Voltage Quad 2-Input Exclusive-OR Gate

General Description

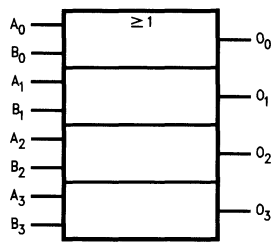
The LVQ86 contains four, 2-input exclusive-OR gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC Products are available for Military/ Aerospace applications

Logic Symbol

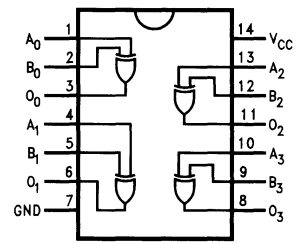
IEEE/IEC



TL/F/11348–1

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



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Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ86SC 74LVQ86SCX	74LVQ86SJ 74LVQ86SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ86 T_A = 25°C		74LVQ86 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44		*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ86 T_A = 25°C		74LVQ86 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V_{IN} = V_{CC} or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2, 4)

†Maximum test duration 20 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC}(V)	74LVQ86 T_A = +25°C C_L = 50 pF			74LVQ86 T_A = −40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	2.0	7.2	16.2	1.5	18.0	ns
		3.3 ±0.3	2.0	6.0	11.5	1.5	12.5	
t_{PHL}	Propagation Delay	2.7	2.0	7.8	16.2	1.5	18.0	ns
		3.3 ±0.3	2.0	6.5	11.5	1.5	12.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skews defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	23	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ125
Low Voltage Quad Buffer with TRI-STATE® Outputs

General Description

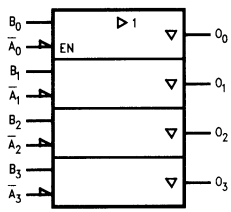
The LVQ125 contains four independent non-inverting buffers with TRI-STATE outputs.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Logic Symbol

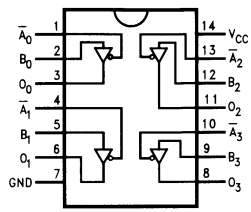
IEEE/IEC



TL/F/11349–1

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



TL/F/11349–2

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ125SC 74LVQ125SCX	74LVQ125SJ 74LVQ125SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteritics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ125 T_A = +25°C	74LVQ125 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ125 $T_A = +25°C$ Typ	74LVQ125 $T_A = +25°C$ Guaranteed Limits	74LVQ125 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Min (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0		V	(Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.6	−1.0		V	(Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8		V	(Notes 2 and 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ125 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ125 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay Data to Output	2.7	1.0	7.8	12.7	1.0	14.0	ns
		3.3 ±0.3	1.0	6.5	9.0	1.0	10.0	
t_{PHL}	Propagation Delay Data to Output	2.7	1.0	7.8	12.7	1.0	14.0	ns
		3.3 ±0.3	1.0	6.5	9.0	1.0	10.0	
t_{PZH}	Output Enable Time	2.7	1.0	7.2	14.8	1.0	16.0	ns
		3.3 ±0.3	1.0	6.0	10.5	1.0	11.0	
t_{PZL}	Output Enable Time	2.7	1.0	9.0	14.0	1.0	16.0	ns
		3.3 ±0.3	1.0	7.5	10.0	1.0	11.0	
t_{PHZ}	Output Disable Time	2.7	1.0	9.0	14.0	1.0	15.0	ns
		3.3 ±0.3	1.0	7.5	10.0	1.0	10.5	
t_{PLZ}	Output Disable Time	2.7	1.0	9.0	14.8	1.0	16.5	ns
		3.3 ±0.3	1.0	7.5	10.5	1.0	11.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	34	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ138
Low Voltage 1-of-8 Decoder/Demultiplexer

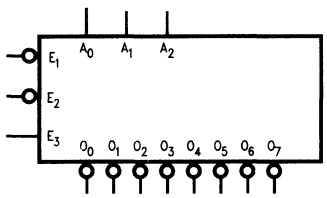
General Description

The LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVQ138 devices or a 1-of-32 decoder using four LVQ138 devices and one inverter.

Features

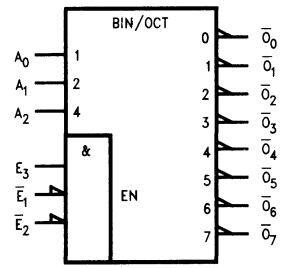
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbols



TL/F/11350–1

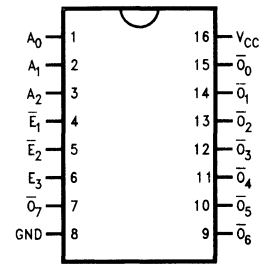
IEEE/IEC



TL/F/11350–4

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



TL/F/11350–2

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ138SC 74LVQ138SCX	74LVQ138SJ 74LVQ138SJX
See NS Package Number	M16A	M16D

Functional Description

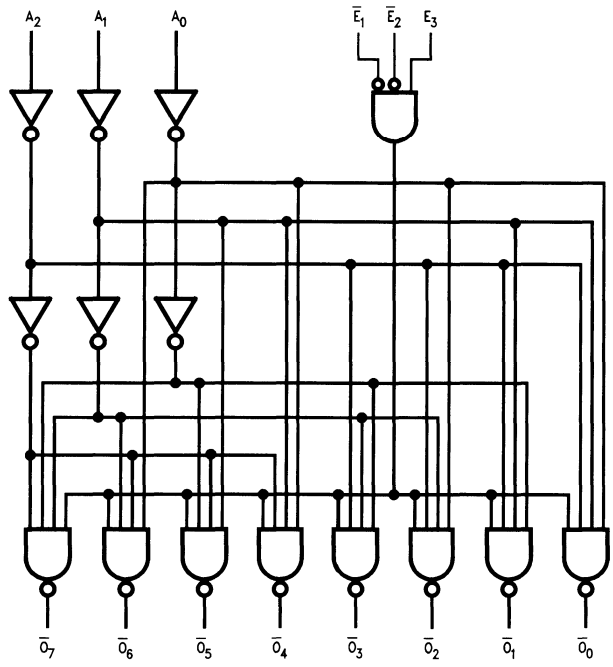
The LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The LVQ138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LVQ138 devices and one inverter (see *Figure 1*). The LVQ138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/11350–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

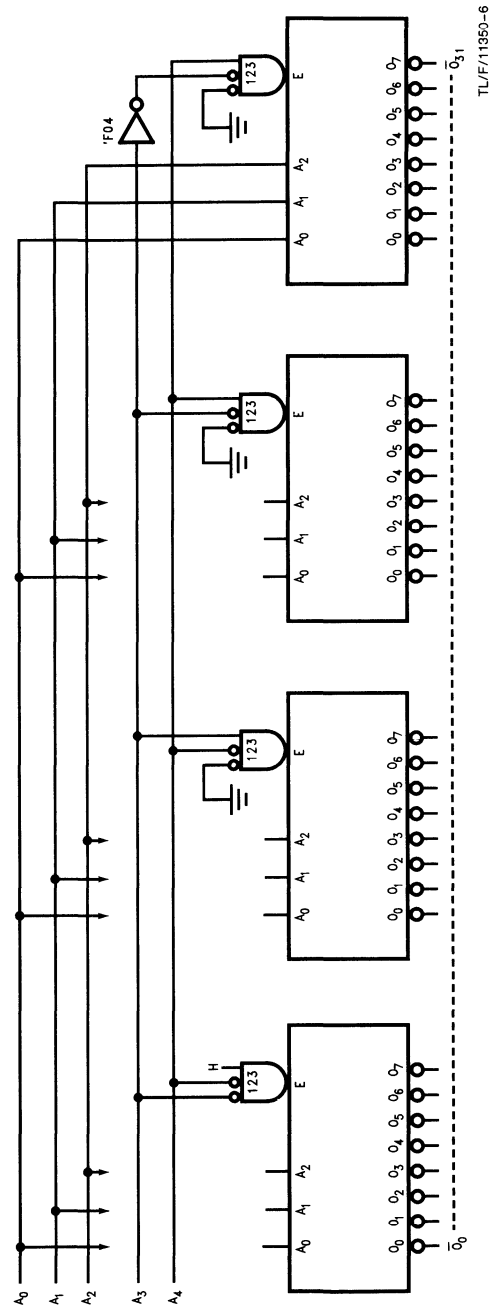


FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ138 T_A = +25°C		74LVQ138 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Outut Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ138 $T_A = +25°C$		74LVQ138 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ138 $T_A = +25°C$, $C_L = 50$ pF			74LVQ138 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	21.0 15.0	ns
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	9.6 8.0	17.6 12.5	1.5 1.5	20.0 14.0	ns
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	13.2 11.0	21.0 15.0	1.5 1.5	23.0 16.0	ns
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	11.4 9.5	19.0 13.5	1.5 1.5	21.0 15.0	ns
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	13.2 11.0	21.8 15.5	1.5 1.5	23.5 16.5	ns
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	2.7 3.3 ±0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	20.0 14.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ151
Low Voltage 8-Input Multiplexer

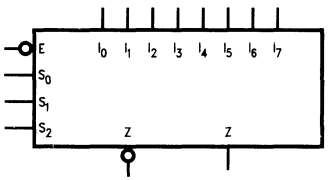
General Description

The LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbols



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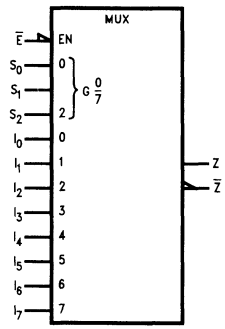
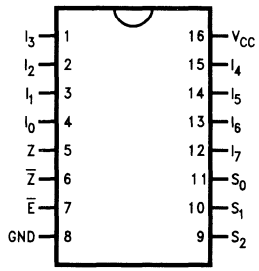
IEEE/IEC



TL/F/11351–4

Connection Diagram

Pin Assignment
SOIC JEDEC and EIAJ



TL/F/11351–2

Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

Truth Table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ151SC 74LVQ151SCX	74LVQ151SJ 74LVQ151SJX
See NS Package Number	M16A	M16D

8

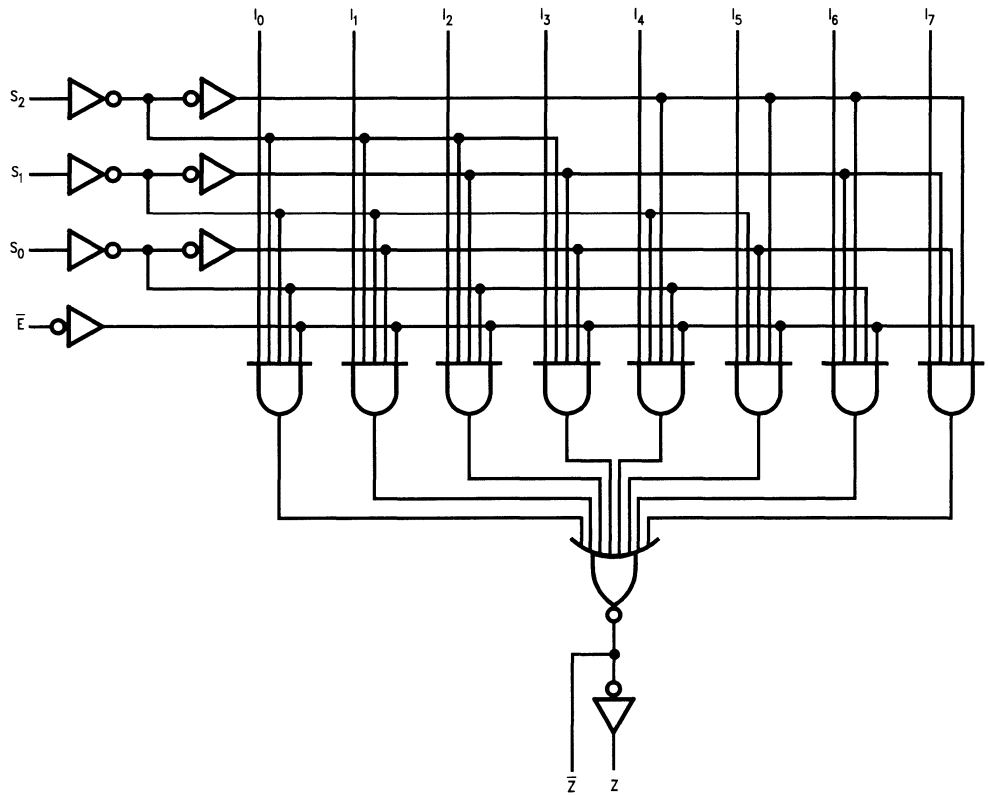
Functional Description

The LVQ151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the LVQ151 can provide any logic function of four variables and its complement.

Logic Diagram



TL/F/11351–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ151 T_A = +25°C		74LVQ151 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ151 $T_A = +25°C$ Typ	74LVQ151 $T_A = +25°C$ Guaranteed Limits	74LVQ151 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ151 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ151 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	2.7	3.0	13.8	25.3	3.0	28.0	ns
		3.3 ±0.3	3.0	11.5	18.0	3.0	20.0	
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	2.7	2.5	14.4	25.3	2.5	28.0	ns
		3.3 ±0.3	2.5	12.0	18.0	2.5	20.0	
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	2.7	2.5	9.6	18.3	2.0	20.0	ns
		3.3 ±0.3	2.5	8.0	13.0	2.0	14.0	
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	2.7	1.5	10.2	18.3	1.5	20.0	ns
		3.3 ±0.3	1.5	8.5	13.0	1.5	14.0	
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	2.7	2.5	11.4	19.7	2.0	22.0	ns
		3.3 ±0.3	2.5	9.5	14.0	2.0	15.5	
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	2.7	2.5	11.4	21.1	2.0	23.0	ns
		3.3 ±0.3	2.5	9.5	15.0	2.0	16.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ157
Low Voltage Quad 2-Input Multiplexer

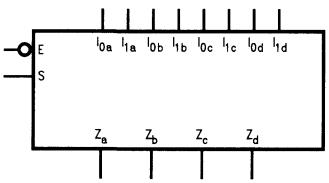
General Description

The LVQ157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVQ157 can also be used as a function generator.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω.
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbols



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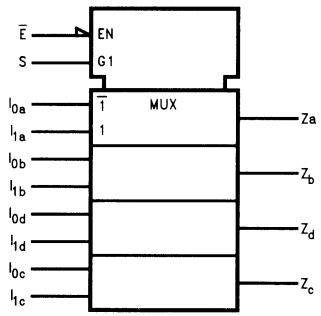
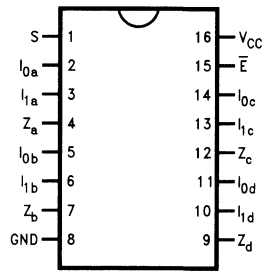
IEEE/IEC



TL/F/11352–3

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



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Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ157SC 74LVQ157SCX	74LVQ157SJ 74LVQ157SJX
See NS Package Number	M16A	M16D

Functional Description

The LVQ157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVQ157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

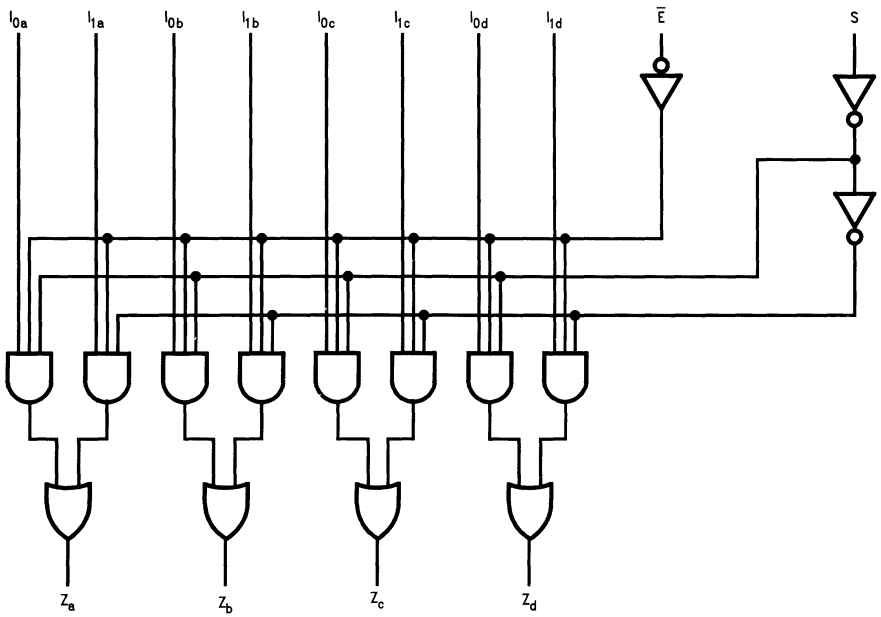
A common use of the LVQ157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVQ157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ157 T_A = +25°C		74LVQ157 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ157 $T_A = +25°C$ Typ	74LVQ157 $T_A = +25°C$ Guaranteed Limits	74LVQ157 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.7	0.8		V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ157 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ157 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay S to Z_n	2.7	1.5	84	16.2	1.5	19.0	ns
		3.3 ±0.3	1.5	7.0	11.5	1.5	13.0	
t_{PHL}	Propagation Delay S to Z_n	2.7	1.5	7.8	15.5	1.5	17.0	ns
		3.3 ±0.3	1.5	6.5	11.0	1.5	12.0	
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	2.7	1.5	8.4	16.2	1.5	19.0	ns
		3.3 ±0.3	1.5	7.0	11.5	1.5	13.0	
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	2.7	1.5	7.8	15.5	1.5	17.0	ns
		3.3 ±0.3	1.5	6.5	11.0	1.5	12.0	
t_{PLH}	Propagation Delay I_n to Z_n	2.7	1.5	6.0	12.0	1.0	13.0	ns
		3.3 ±0.3	1.5	5.0	8.5	1.0	9.0	
t_{PHL}	Propagation Delay I_n to Z_n	2.7	1.5	6.0	11.3	1.0	13.0	ns
		3.3 ±0.3	1.5	5.0	8.0	1.0	9.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	34.0	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ174
Low Voltage Hex D Flip-Flop with Master Reset

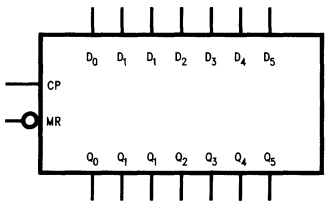
General Description

The LVQ174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Logic Symbols



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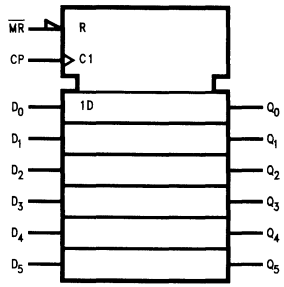
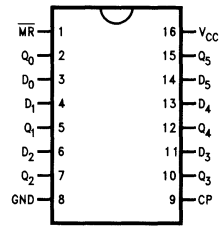
IEEE/IEC



TL/F/11353–2

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



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Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ174SC 74LVQ174SCX	74LVQ174SJ 74LVQ174SJX
See NS Package Number	M16A	M16D

Functional Description

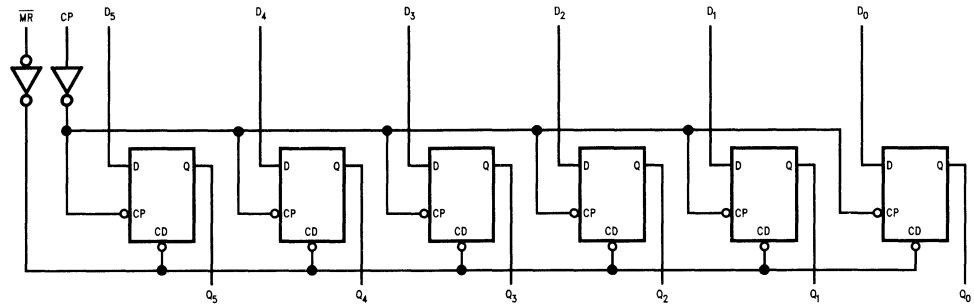
The LVQ174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LVQ174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ174 T_A = +25°C		74LVQ174 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ174 $T_A = +25°C$ Typ	74LVQ174 $T_A = +25°C$ Guaranteed Limits	74LVQ174 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.7	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.6	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ174 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ174 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	60 90	90 100		50 70		MHz
t_{PLH}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	2.0 2.0	10.8 9.0	16.2 11.5	1.5 1.5	18.0 12.5	ns
t_{PHL}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	2.0 2.0	10.2 8.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7 3.3 ±0.3	2.5 2.5	10.8 9.0	16.2 11.5	2.0 2.0	18.0 12.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ174 $T_A = +25°C$, $C_L = 50$ pF		74LVQ174 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	3.0 2.5	8.0 6.5	10.0 7.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	1.2 1.0	4.0 3.0	4.5 3.0	ns
t_w	$\overline{MR}$ Pulse Width, LOW	2.7 3.3 ±0.3	1.2 1.0	7.0 5.5	10.0 7.0	ns
t_w	CP Pulse Width	2.7 3.3 ±0.3	1.2 1.0	7.0 5.5	10.0 7.0	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	2.7 3.3 ±0.3	0 0	3.5 2.5	3.5 2.5	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	23	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ240
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

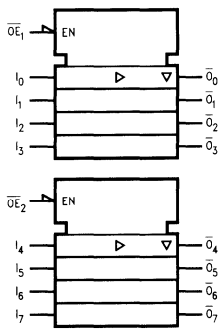
The LVQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbol

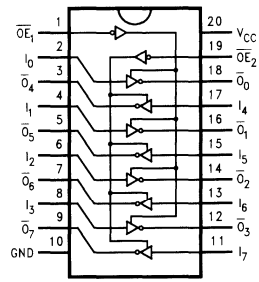
IEEE/IEC



TL/F/11611–1

Connection Diagram

Pin Assignment, SOIC and QSOP



TL/F/11611–2

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ240SC 74LVQ240SCX	74LVQ240SJ 74LVQ240SJX	74LVQ240QSC 74LVQ240QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
V_{IN} 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ240 T_A = +25°C		74LVQ240 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ240 $T_A = +25°C$ Typ	74LVQ240 $T_A = +25°C$ Guaranteed Limits	74LVQ240 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n − 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ240 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ240 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	2.7	2.0	8.4	14.0	2.0	15.0	ns
		3.3 ±0.3	2.0	7.0	10.0	2.0	10.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	2.5	9.6	16.9	2.5	18.0	ns
		3.3±0.3	2.5	8.0	12.0	2.5	12.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.2	19.0	1.0	20.0	ns
		3.3 ±0.3	1.0	8.5	13.5	1.0	14.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew *Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	70	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ241
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

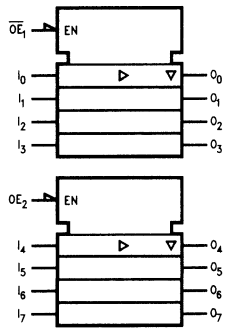
The LVQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbol

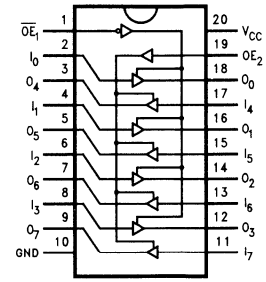
IEEE/IEC



TL/F/11355–1

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11355–2

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I_n	
L	X	Z
H	H	H
H	L	L

H = HIGH Voltage Level L = LOW Voltage Level
X = Immaterial Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, OE_2	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ241SC 74LVQ241SCX	74LVQ241SJ 74LVQ241SJX	74LVQ241QSC 74LVQ241QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Rating (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
V_{IN} 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ241 T_A = +25°C		74LVQ241 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ241 $T_A = +25°C$ Typ	74LVQ241 $T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n − 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ241 $T_A = +25°C$, $C_L = 50$ pF			74LVQ241 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	2.7	2.0	7.8	12.7	2.0	14.0	ns
		3.3 ±0.3	2.0	6.5	9.0	2.0	9.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	2.5	9.6	18.3	2.5	19.0	ns
		3.3 ±0.3	2.5	8.0	13.0	2.5	13.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.2	20.4	1.0	21.0	ns
		3.3 ±0.3	1.0	8.5	14.5	1.0	15.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew *Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	70	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ244
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

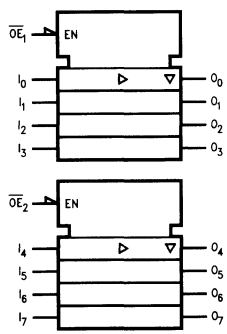
The LVQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbol

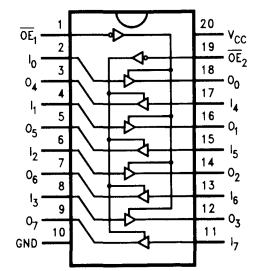
IEEE/IEC



TL/F/11356–1

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11356–2

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ244SC 74LVQ244SCX	74LVQ244SJ 74LVQ244SJX	74LVQ244QSC 74LVQ244QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Rating (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ244 T_A = +25°C		74LVQ244 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ244 $T_A = +25°C$ Typ	74LVQ244 $T_A = +25°C$ Guaranteed Limits	74LVQ244 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ244 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ244 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	2.7	2.0	8.4	12.7	2.0	14.0	ns
		3.3 ±0.3	2.0	7.0	9.0	2.0	9.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	2.5	9.6	16.9	2.5	18.0	ns
		3.3 ±0.3	2.5	8.0	12.0	2.5	12.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.8	19.0	1.0	20.0	ns
		3.3 ±0.3	1.0	9.0	13.5	1.0	14.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ245
Low Voltage Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

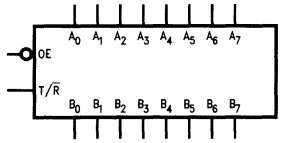
General Description

The LVQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 12 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54 ACQ products are available for Military/Aerospace applications

Logic Symbols



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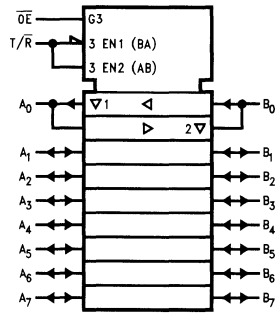

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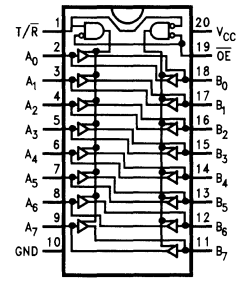
Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11357–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ245SC 74LVQ245SCX	74LVQ245SJ 74LVQ245SJX	74LVQ245QSC 74LVQ245QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum raings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ245 T_A = +25°C	74LVQ245 T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = +12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ245 $T_A = +25°C$ Typ	74LVQ245 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6		−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6	4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	3.6	±0.3	±3.0	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0	V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ245 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay	2.7	2.0	9.0	14.0	2.0	15.0	ns
		3.3 ±0.3	2.0	7.5	10.0	2.0	10.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	3.0	10.2	18.3	3.0	19.0	ns
		3.3 ±0.3	3.0	8.5	13.0	3.0	13.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.2	20.4	1.0	21.0	ns
		3.3 ±0.3	1.0	8.5	14.5	1.0	15.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	67	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ273
Low Voltage Octal D Flip-Flop

General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

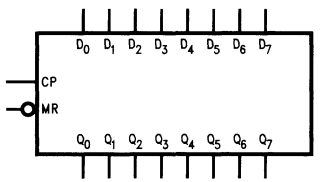
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbols



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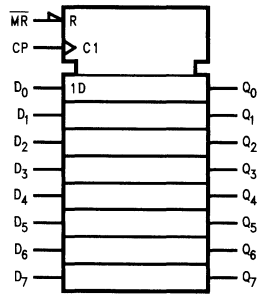

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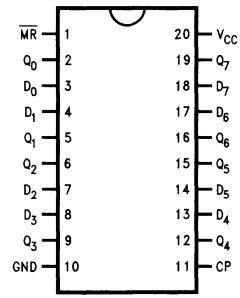
Connection Diagram

Pin Assignment for SOIC and QSOP



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Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ273SC 74LVQ273SCX	74LVQ273SJ 74LVQ273SJX	74LVQ273QSC 74LVQ273QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ273		74LVQ273	Units	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$		74LVQ273 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$, $C_L = 50$ pF			74LVQ273 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	50 90			45 75		MHz
t_{PLH}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t_{PHL}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$, $C_L = 50$ pF		74LVQ273 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3		6.5 5.0	8.5 6.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3		0.0 0.0	0.0 0.0	ns
t_w	Clock Pulse Width HIGH or LOW	2.7 3.3 ±0.3		7.0 5.5	8.5 6.0	ns
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	2.7 3.3 ±0.3		7.0 5.5	8.5 6.0	ns
t_w	Recovery Time $\overline{MR}$ to CP	2.7 3.3 ±0.3		5.0 4.0	6.5 4.5	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	35	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ373
Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

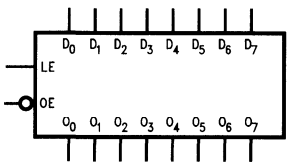
General Description

The LVQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbols



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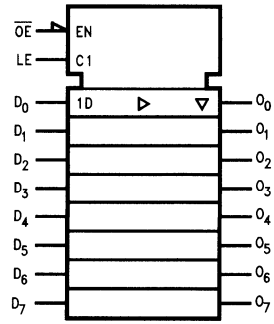

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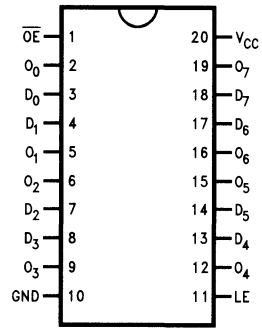
Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11359–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ373SC 74LVQ373SCX	74LVQ373SJ 74LVQ373SJX	74LVQ373QSC 74LVQ373QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

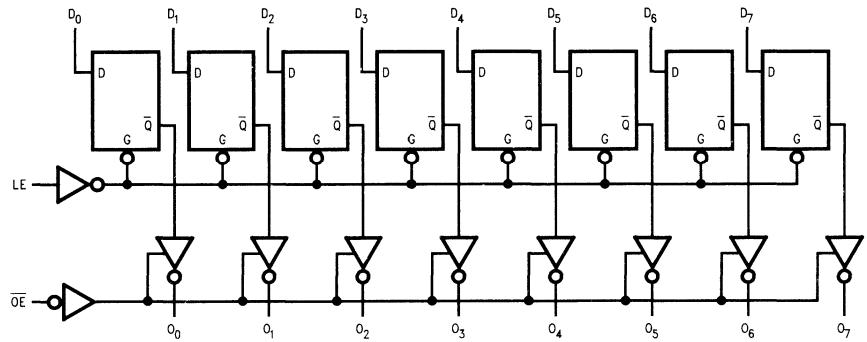
The LVQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/11359–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ373 T_A = +25°C		74LVQ373 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ373 $T_A = +25°C$ Typ	74LVQ373 $T_A = +25°C$ Guaranteed Limits	74LVQ373 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ373 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ373 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	2.7	2.5	9.6	14.8	2.5	16.0	ns
		3.3 ±0.3	2.5	8.0	10.5	2.5	11.0	
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	2.7	2.5	9.6	16.9	2.5	18.0	ns
		3.3 ±0.3	2.5	8.0	12.0	2.5	12.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	ns
		3.3 ±0.3	2.5	8.5	13.0	2.5	13.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
		3.3 ±0.3	1.0	9.0	14.5	1.0	15.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ373 $T_A = +25°C$, $C_L = 50$ pF		74LVQ373 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW	2.7 3.3 ±0.3	0 0	4.0 3.0	4.5 3.0	ns
t_H	Hold Time, HIGH or LOW	2.7 3.3 ±0.3	0 0	1.5 1.5	1.5 1.5	ns
t_W	LE Pulse Width, HIGH	2.7 3.3 ±0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	39	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ374
Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

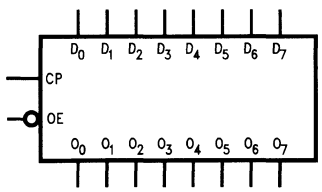
General Description

The LVQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- MIL-STD-883 54ACQ Products are available for Military/Aerospace Applications

Logic Symbols



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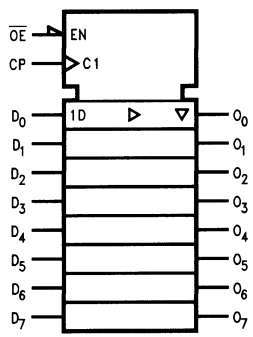
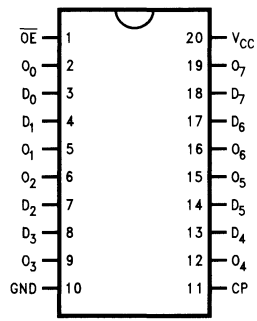
IEEE/IEC



TL/F/11360–2

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11360–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SOIC JEDEC
Order Number	74LVQ374SC 74LVQ374SCX	74LVQ374SJ 74LVQ374SJX	74LVQ374QSC 74LVQ374QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

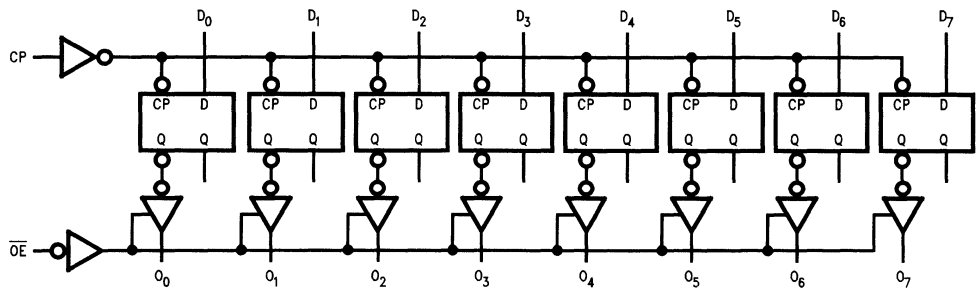
The LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11360–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ374		74LVQ374	Units	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ374 $T_A = +25°C$		74LVQ374 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ374 $T_A = +25°C$, $C_L = 50$ pF			74LVQ374 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	2.7	55			50		MHz
		3.3 ±0.3	75			70		
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	2.7	3.0	11.4	18.3	3.0	19.0	ns
		3.3 ±0.3	3.0	9.5	13.0	3.0	13.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	3.0	11.4	18.3	3.0	19.0	ns
		3.3 ±0.3	3.0	9.5	13.0	3.0	13.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	11.4	20.4	1.0	21.0	ns
		3.3 ±0.3	1.0	9.5	14.5	1.0	15.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* CP to O_n	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ374		74LVQ374	Units
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	0 0	4.0 3.0	4.5 3.0	ns
t_H	Hold Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	0 0	1.5 1.5	1.5 1.5	ns
t_W	CP Pulse Width, HIGH or LOW	2.7 3.3 ±0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	39	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

74LVQ573
Low Voltage Octal Latch with TRI-STATE® Outputs

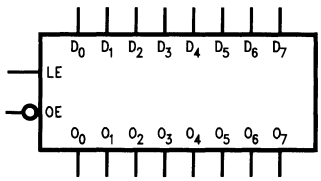
General Description

The LVQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The LVQ573 is functionally identical to the LVQ373 but with inputs and outputs on opposite sides of the package.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbols



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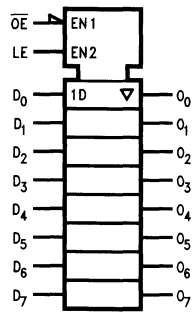
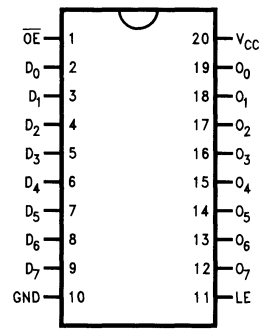
IEEE/IEC



TL/F/11361–2

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11361–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ573SC 74LVQ573SCX	74LVQ573SJ 74LVQ573SJX	74LVQ573QSC 74LVQ573QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

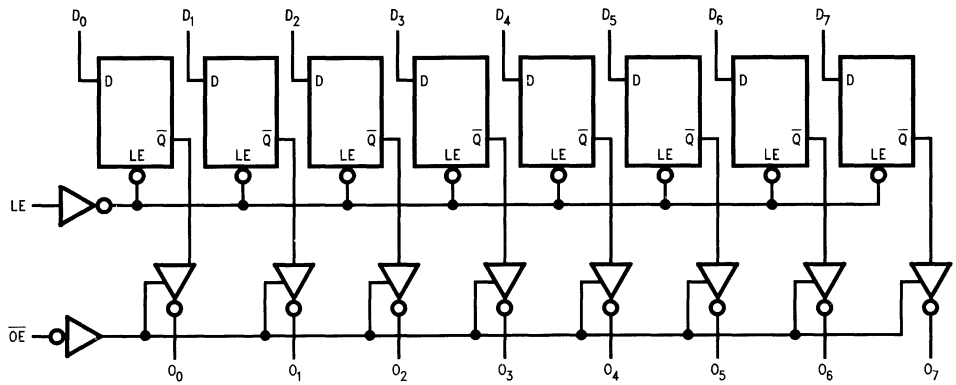
The LVQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/11361–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ573 T_A = +25°C		74LVQ573 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ573 $T_A = +25°C$ Typ	74LVQ573 $T_A = +25°C$ Guaranteed Limits	74LVQ573 $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	$V_{OLD} = 0.8\ V_{Max}$ (Note 1)
I_{OHD}		3.6			−25	mA	$V_{OHD} = 2.0V\ V_{Min}$ (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Curent	3.6		±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ573 $T_A = +25°C$ $C_L = 50$ pF Min	Typ	Max	74LVQ573 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	2.7	2.5	10.2	14.8	2.5	16.0	ns
		3.3 ±0.3	2.5	8.5	10.5	2.5	11.0	
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	2.7	2.5	10.2	16.9	2.5	18.0	ns
		3.3 ±0.3	2.5	8.5	12.0	2.5	12.5	
t_{PZL}, t_{PZH}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	ns
		3.3 ±0.3	2.5	8.5	13.0	2.5	13.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
		3.3 ±0.3	1.0	9.0	14.5	1.0	15.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew* D_n to O_n	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ573 $T_A = +25°C$, $C_L = 50$ pF		74LVQ573 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to LE	2.7	0	4.0	4.5	ns
		3.3 ±0.3	0	3.0	3.0	
t_H	Hold Time, HIGH or LOW D_n to LE	2.7	0	1.5	1.5	ns
		3.3 ±0.3	0	1.5	1.5	
t_W	LE Pulse Width, HIGH	2.7	2.4	5.0	6.0	ns
		3.3 ±0.3	2.0	4.0	4.0	

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	37	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

Section 9

LVT Family

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LVT Family
Low Voltage High Speed BiCMOS Logic

Features	Advantages
High +64/−32 mA output drive	Drives large loads, backplanes, memory arrays, etc.
High speed (4.0 ns max t_{PD})	Talks to the latest high speed processor buses
5V tolerant inputs and outputs	Interfaces seamlessly to 3V and/or 5V devices
Power up/down high impedance inputs and outputs	Facilitates power management and live insertion
2.7V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Bus hold on input, I/O, and control pins	Eliminates the need for pull-up resistors
Latch-up performance exceeds 500 mA	Great for robust applications
SOIC, TSSOP, and SSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensured supply

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ADVANCE INFORMATION

74LVT125
3.3V ABT Quad Buffer with TRI-STATE® Outputs

General Description

The LVT125 contains four independent non-inverting buffers with TRI-STATE outputs.

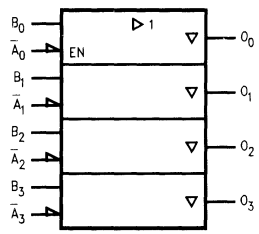
These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, and TSSOP
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500 mA

Logic Symbol

IEEE/IEC



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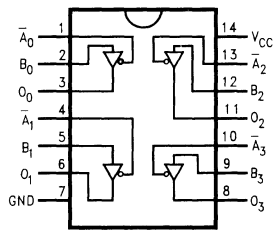
Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	TRI-STATE Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT125M 74LVT125MX	74LVT125SJ 74LVT125SJX	74LVT125MTC 74LVT125MTCX
See NS Package Number	M14A	M14D	MTC14

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PRELIMINARY

74LVT240
3.3V ABT Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

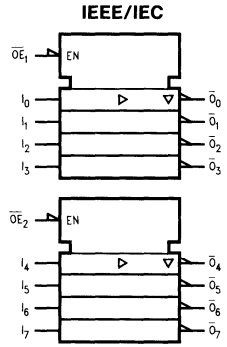
These octal buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOPII
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA

Logic Symbol

IEEE/IEC



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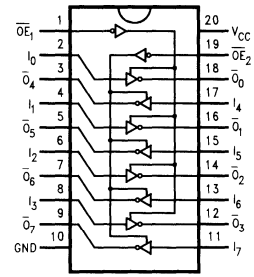
Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOPII



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Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP	SSOPII
Order Number	74LVT240WM 74LVT240WMX	74LVT240SJ 74LVT240SJX	74LVT240MTC 74LVT240MTCX	74LVT240MSA 74LVT240MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at High State	mA
		128	Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	3.6	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \leq$ 0.1V or $V_O \geq V_{CC}$ − 0.1V
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
		2.7	2.2			V	I_{OH} = −8 mA
		3.0	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 μA
		2.7			0.5	V	I_{OL} = 24 mA
		3.0			0.4	V	I_{OL} = 16 mA
		3.0			0.5	V	I_{OL} = 32 mA
		3.0			0.55	V	I_{OL} = 64 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ (Note 3)	Max	Units	Conditions
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	V_I = 0.8V
				−75			μA	V_I = 2.0V
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	V_I = 5.5V
			3.6			±1	μA	V_I = 0V or V_{CC}
		Data Pins	3.6			−5	μA	V_I = 0V
						1	μA	V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	μA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$ (Note 6)	Power up/down TRI-STATE Output Current		0–1.2V			±100	μA	V_O = 0.5V to V_{CC} V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	V_O = 0.5V
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	V_O = 3.0V
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			10	μA	V_{CC} < V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			16.5	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, V_{CC} ≤ V_O ≤ 5.5V, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 3: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	Typ	Max	Units	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.3	1.0	5.2	ns
t_{PHL}		1.0		4.3	1.0	5.0	
t_{PZH}	Output Enable Time	1.0		5.2	1.0	6.3	ns
t_{PZL}		1.0		5.2	1.0	6.7	
t_{PHZ}	Output Disable Time	1.8		5.6	1.8	6.3	ns
t_{PLZ}		1.8		5.1	1.8	5.6	
t_{OSHL}	Output to Output Skew (Note 10)			1.0			ns
t_{OSLH}							

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

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PRELIMINARY

74LVT244
3.3V ABT Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

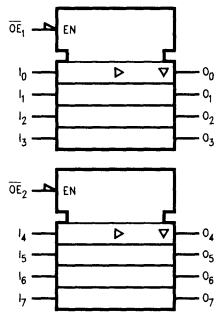
These octal buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOPII
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA

Logic Symbol

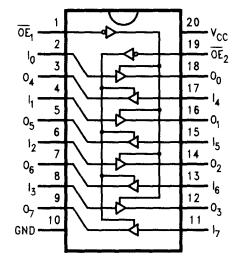
IEEE/IEC



TL/F/12014–1

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOPII



TL/F/12014–2

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	SSOPII
Order Number	74LVT244WM 74LVT244WMX	74LVT244SJ 74LVT244SJX	74LVT244MTC 74LVT244MTCX	74LVT244MSA 74LVT244MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at High State	mA
		128	Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	3.6	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \leq$ 0.1V or $V_O \geq V_{CC}$ − 0.1V
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
		2.7	2.2			V	I_{OH} = −8 mA
		3.0	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 μA
		2.7			0.5	V	I_{OL} = 24 mA
		3.0			0.4	V	I_{OL} = 16 mA
		3.0			0.5	V	I_{OL} = 32 mA
		3.0			0.55	V	I_{OL} = 64 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ (Note 3)	Max	Units	Conditions
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	V_I = 0.8V
				−75			μA	V_I = 2.0V
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	V_I = 5.5V
			3.6			±1	μA	V_I = 0V or V_{CC}
		Data Pins	3.6			−5	μA	V_I = 0V
						1	μA	V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	μA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$ (Note 6)	Power up/down TRI-STATE Output Current		0–1.2V			±100	μA	V_O = 0.5V to V_{CC} V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	V_O = 0.5V
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	V_O = 3.0V
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			10	μA	V_{CC} < V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			16.5	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, V_{CC} ≤ V_O ≤ 5.5V, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 3: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	Typ	Max	Units	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.1	1.0	5.0	ns
t_{PHL}		1.0		4.1	1.0	5.2	
t_{PZH}	Output Enable Time	1.0		5.2	1.0	6.3	ns
t_{PZL}		1.0		5.2	1.0	6.7	
t_{PHZ}	Output Disable Time	1.8		5.6	1.8	6.3	ns
t_{PLZ}		1.8		5.1	1.8	5.6	
t_{OSHL}	Output to Output Skew			1.0			ns
t_{OSLH}	(Note 10)						

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

74LVT245
3.3V ABT Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

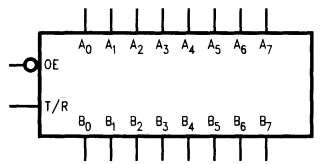
The LVT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOPII
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA

Logic Symbols



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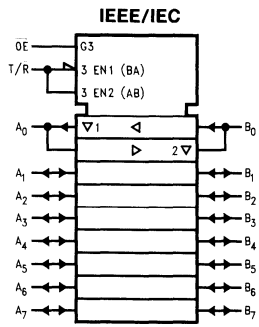
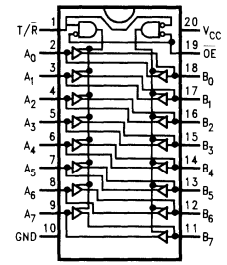


TL/F/12013–2

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOPII



TL/F/12013–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	SSOPII
Order Number	74LVT245WM 74LVT245WMX	74LVT245SJ 74LVT245SJX	74LVT245MTC 74LVT245MTCX	74LVT245MSA 74LVT245MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at High State	mA
		128	Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	3.6	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
		2.7	2.2			V	I_{OH} = −8 mA
		3.0	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 μA
		2.7			0.5	V	I_{OL} = 24 mA
		3.0			0.4	V	I_{OL} = 16 mA
		3.0			0.5	V	I_{OL} = 32 mA
		3.0			0.55	V	I_{OL} = 64 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ (Note 3)	Max	Units	Conditions
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	V_I = 0.8V
				−75			μA	V_I = 2.0V
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	V_I = 5.5V
			3.6			±1	μA	V_I = 0V or V_{CC}
		Data Pins (I/O)	3.6			−5	μA	V_I = 0V
						1	μA	V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	μA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Output Current		0–1.2V			±100	μA	V_O = 0.5V to V_{CC} V_I = GND or V_{CC}
I_{OZH}+	TRI-STATE Output Leakage Current		3.6			20	μA	V_{CC} < V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			16.5	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, Outputs Disabled
I_{CCZH}+	Power Supply Current		3.6			0.19	mA	V_I = GND or V_{CC}, V_{CC} ≤ V_O ≤ 5.5V, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 3: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	Typ	Max	Units	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.0		4.0 4.0	1.0 1.0	5.2 5.5	ns
t_{PZH} t_{PZL}	Output Enable Time	1.1 1.5		5.9 6.5	1.1 1.5	7.1 7.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.2 2.0		5.9 5.5	2.2 2.0	6.5 5.6	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 10)			1.0			ns

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

ADVANCE INFORMATION

74LVT373
3.3V ABT Octal Transparent Latch with TRI-STATE® Outputs

General Description

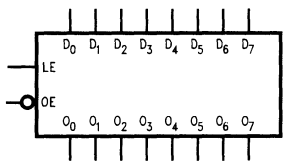
The LVT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOPII
- Functionally compatible with the 74 series 373

Logic Symbols



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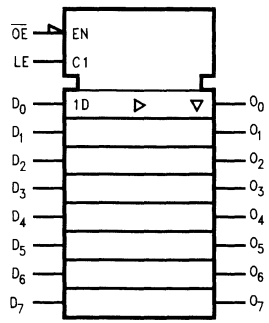
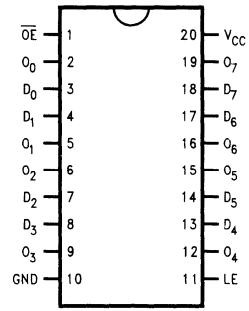
IEEE/IEC



TL/F/12015–2

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOPII



TL/F/12015–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	SSOPII
Order Number	74LVT373WM 74LVT373WMX	74LVT373SJ 74LVT373SJX	74LVT373MTC 74LVT373MTCX	74LVT373MSA 74LVT373MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Functional Description

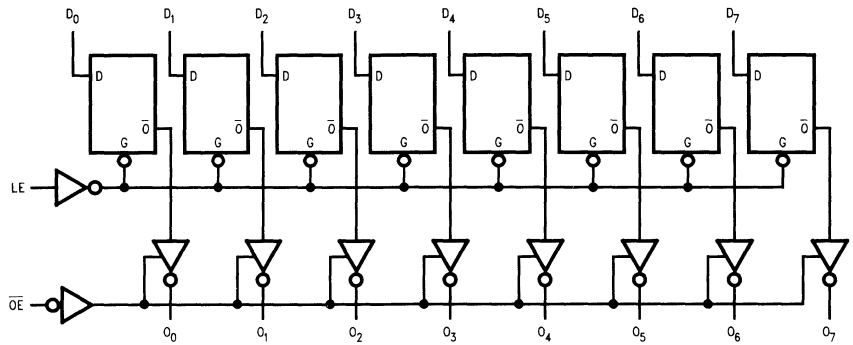
The LVT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



TL/F/12015–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT374
3.3V ABT Octal D Flip-Flop with TRI-STATE® Outputs

General Description

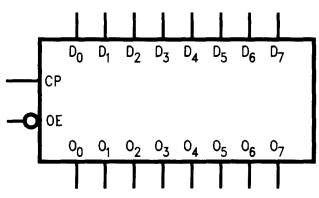
The LVT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

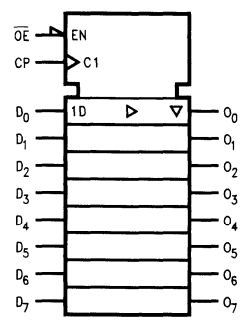
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOPII
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA

Logic Symbols



TL/F/12016–1

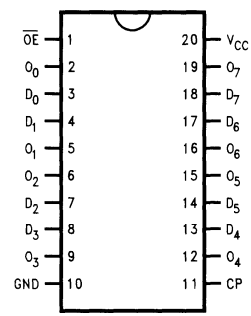
IEEE/IEC



TL/F/12016–2

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOPII



TL/F/12016–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	SSOPII
Order Number	74LVT374WM 74LVT374WMX	74LVT374SJ 74LVT374SJX	74LVT374MTC 74LVT374MTCX	74LVT374MSA 74LVT374MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Functional Description

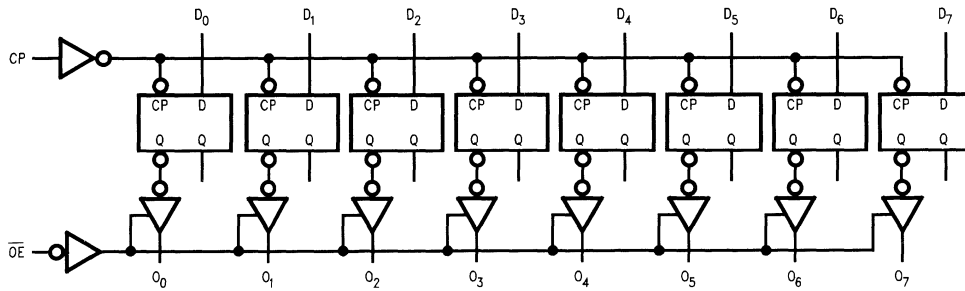
The LVT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



TL/F/12016–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT543
3.3V ABT Octal Registered Transceiver with TRI-STATE® Outputs

General Description

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

These octal registered transceivers is/are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT543 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

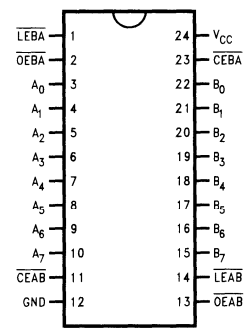
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC and TSSOP
- Functionally compatible with the 74 series 543
- Latch-up performance exceeds 500 mA

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, SSOP II and TSSOP



TL/F/12448–1

	SOIC JEDEC	TSSOP	SSOP II
Order Number	74LVT543WM 74LVT543WMX	74LVT543MTC 74LVT543MTCX	74LTV543MSA 74LTV543MSAX
See NS Package Number	M24B	MTC24	MSA24

Functional Description

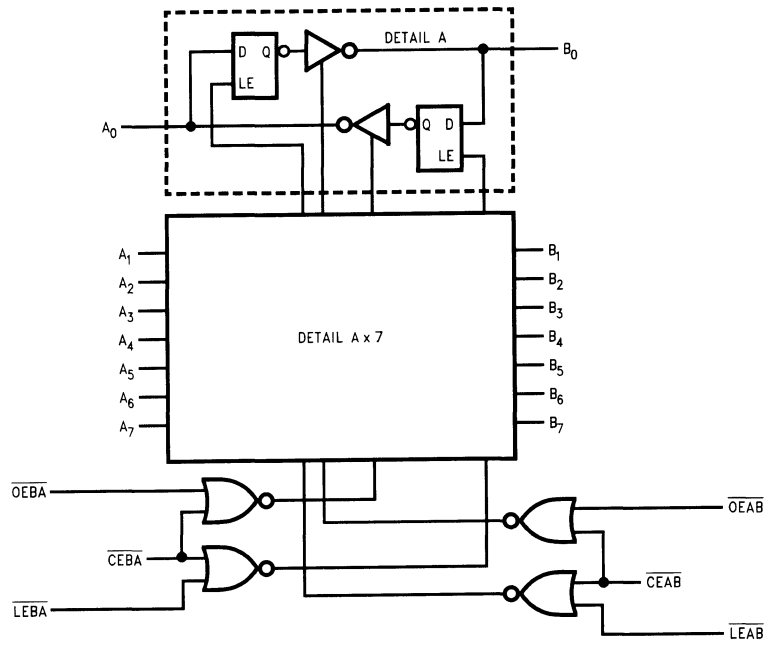
The 'LVT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



TL/F/12448–2

National Semiconductor

ADVANCE INFORMATION

74LVT573
3.3V ABT Octal Transparent Latch with TRI-STATE® Outputs

General Description

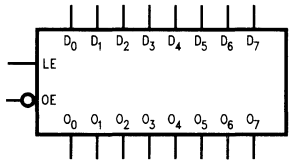
The LVT573 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT573 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

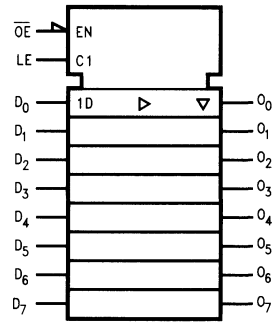
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOP II
- Functionally compatible with the 74 series 573
- Latch-up performance exceeds 500 mA

Logic Symbols



TL/F/12450–1

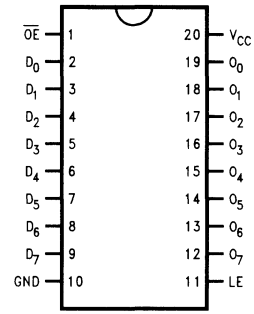
IEEE/IEC



TL/F/12450–2

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOP II



TL/F/12450–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP	SSOP II
Order Number	74LVT573WM 74LVT573WMX	74LVT573SJ 74LVT573SJX	74LVT573MTC 74LVT573MTCX	74LVT573MSA 74LVT573MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Functional Description

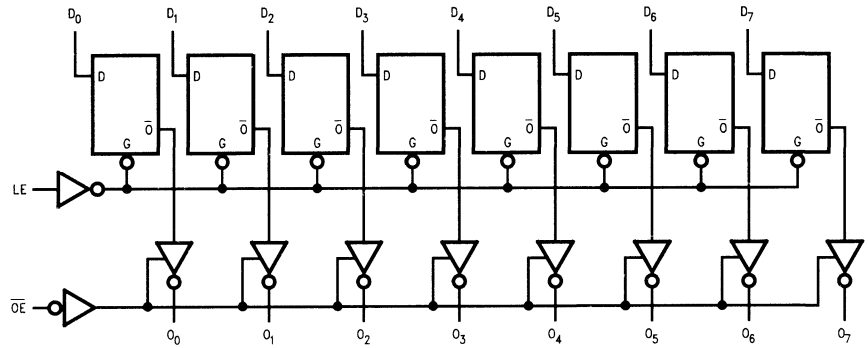
The LVT573 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



TL/F/12450–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT574
3.3V ABT Octal D Flip-Flop with TRI-STATE® Outputs

General Description

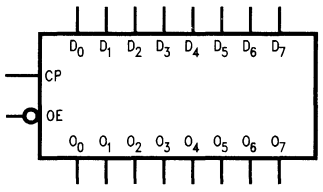
The LVT574 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT574 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

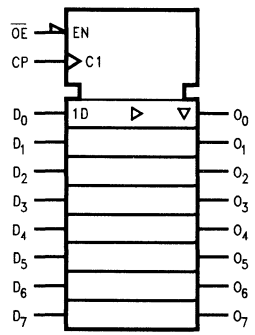
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOP II
- Functionally compatible with the 74 series 574
- Latch-up performance exceeds 500 mA

Logic Symbols



TL/F/12451–1

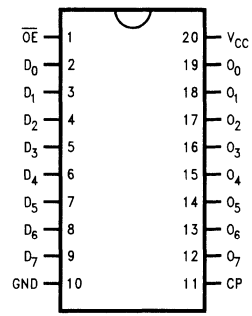
IEEE/IEC



TL/F/12451–2

Connection Diagram

Pin Assignment for SOIC, TSSOP and SSOP II



TL/F/12451–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	SSOP II
Order Number	74LVT574WM 74LVT574WMX	74LVT574SJ 74LVT574SJX	74LVT574MTC 74LVT574MTCX	74LVT574MSA 74LVT574MSAX
See NS Package Number	M20B	M20D	MTC20	MSA20

Functional Description

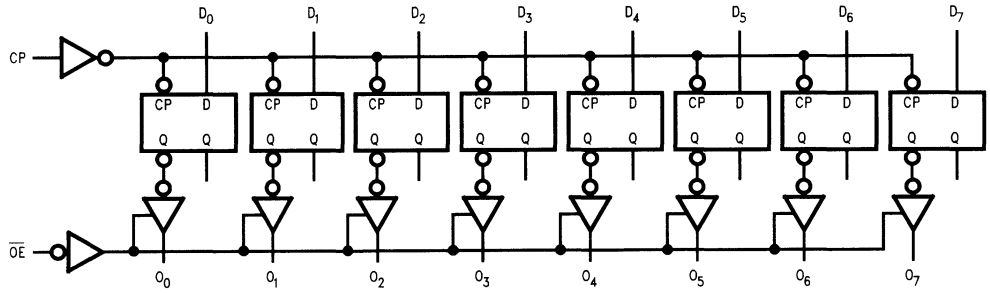
The LVT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



TL/F/12451–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT646
3.3V ABT Octal Transceiver/Register with TRI-STATE® Outputs

General Description

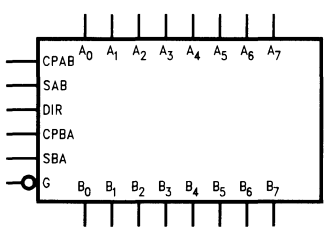
The LVT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1–4*.

The bus transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

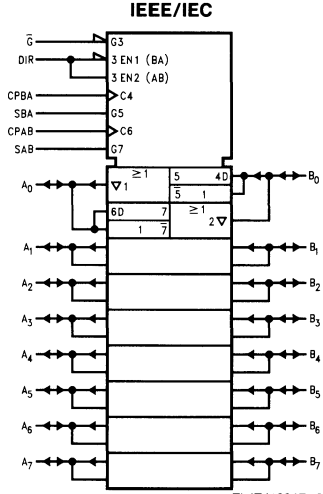
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused input
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, and TSSOP
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA

Logic Symbols



TL/F/12017–1

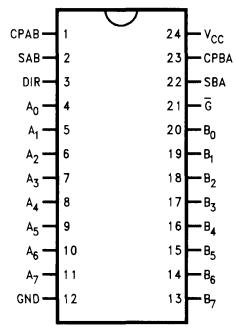
IEEE/IEC



TL/F/12017–2

Connection Diagram

Pin Assignment for SOIC and TSSOP

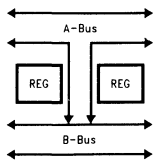


TL/F/12017–3

Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT646WM 74LVT646WMX	74LVT646MTCX
See NS Package Number	M24B	MTC24

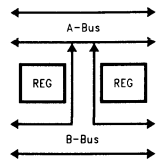
Real Time Transfer A-Bus to B-Bus



TL/F/12017–4

FIGURE 1

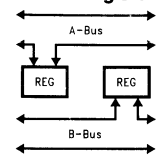
Real Time Transfer B-Bus to A-Bus



TL/F/12017–5

FIGURE 2

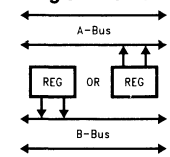
Storage from Bus to Register



TL/F/12017–6

FIGURE 3

Transfer from Register to Bus



TL/F/12017–7

FIGURE 4

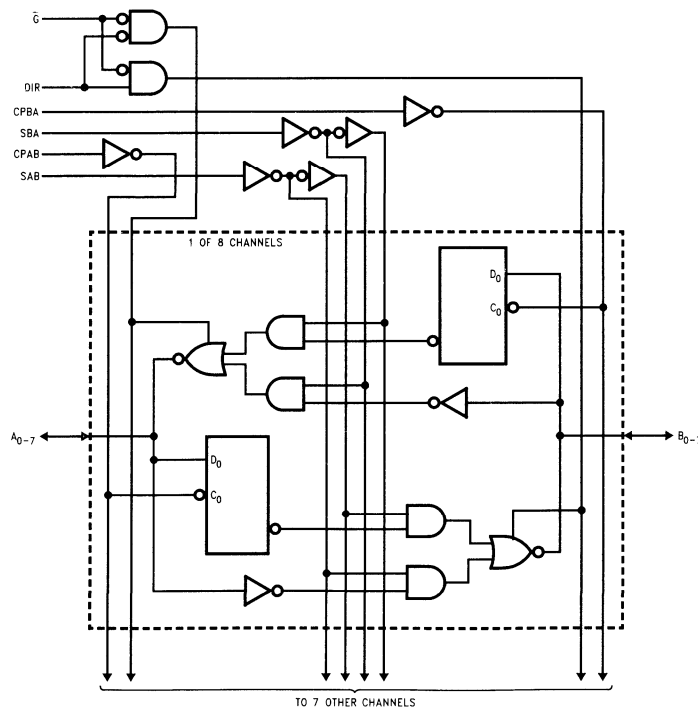
Truth Table (Note)

Inputs						Data I/O		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

Note: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/12017–8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT652
3.3V ABT Octal Transceiver/Register with TRI-STATE® Outputs

General Description

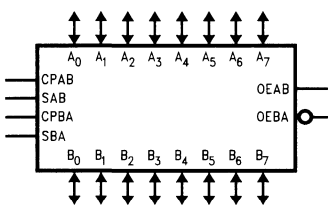
The LVT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

These bus/octal buffers and line drivers is/are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

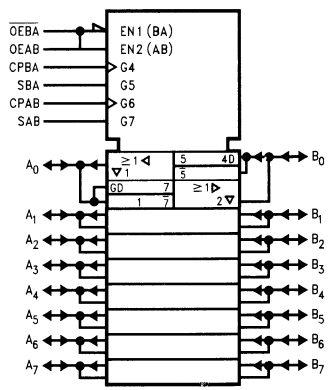
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC and TSSOP
- Functionally compatible with the 74 series 652
- Latch-up performance exceeds 500 mA

Logic Symbols



TL/F/12018–8

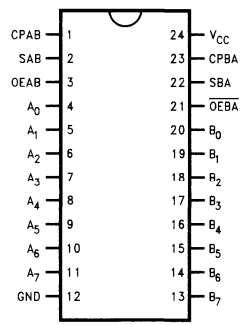
IEEE/IEC



TL/F/12018–7

Connection Diagram

Pin Assignment for SOIC and TSSOP

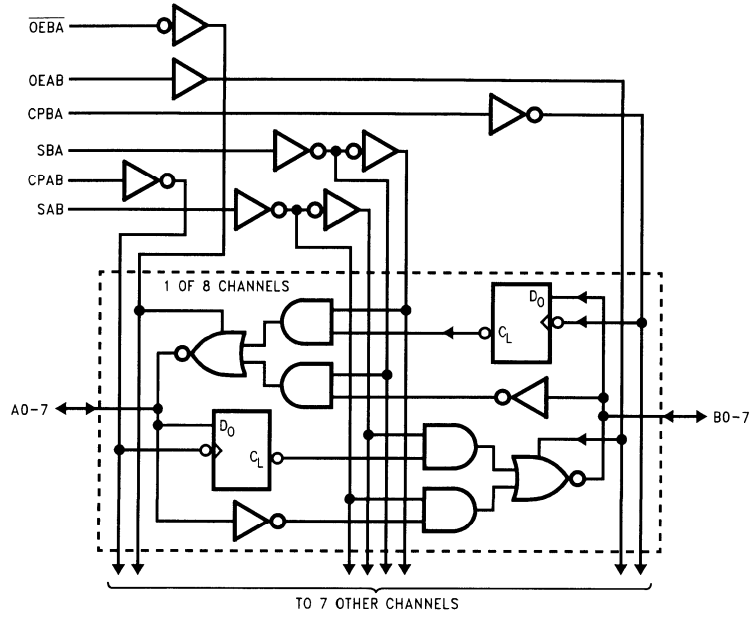


TL/F/12018–1

Pin Names	Description
A_0–A_7	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT652WM 74LVT652WMX	74LVT652MTCX
See NS Package Number	M24B	MTC24

Logic Diagram



TL/F/12018–2

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

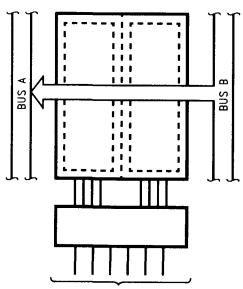
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the LVT652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

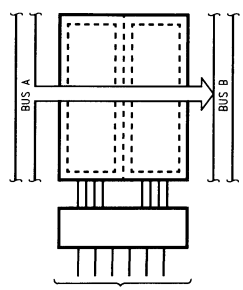
Real-Time Transfer Bus B to Bus A



TL/F/12018–3

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

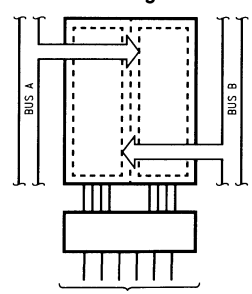
Real-Time Transfer Bus A to Bus B



TL/F/12018–4

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

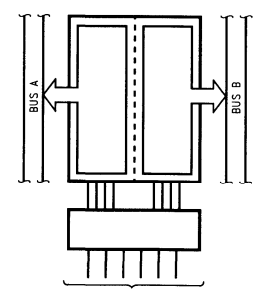
Storage



TL/F/12018–5

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Transfer Storage Data to A or B



TL/F/12018–6

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Truth Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Not Specified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↑ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

National Semiconductor

ADVANCE INFORMATION

74LVT2952
3.3V ABT Octal Registered Transceiver

General Description

The 'LVT2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register.

These octal registered transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT2952 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

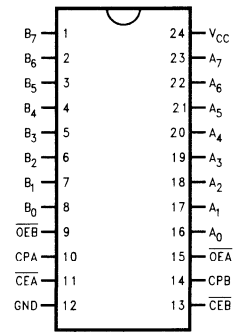
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, TSSOP and SSOP II
- Functionally compatible with the 74 series 2952
- Latch-up performance exceeds 500 mA

Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12452–1

	SOIC JEDEC	TSSOP	SSOP II
Order Number	74LVT2952WM 74LVT2952WMX	74LVT292MTC 74LVT2952MTCX	74LVT2925MSA 74LVT2952MSAX
See NS Package Number	M24B	MTC24	MSA24

Pin Descriptions (Continued)

Output Control

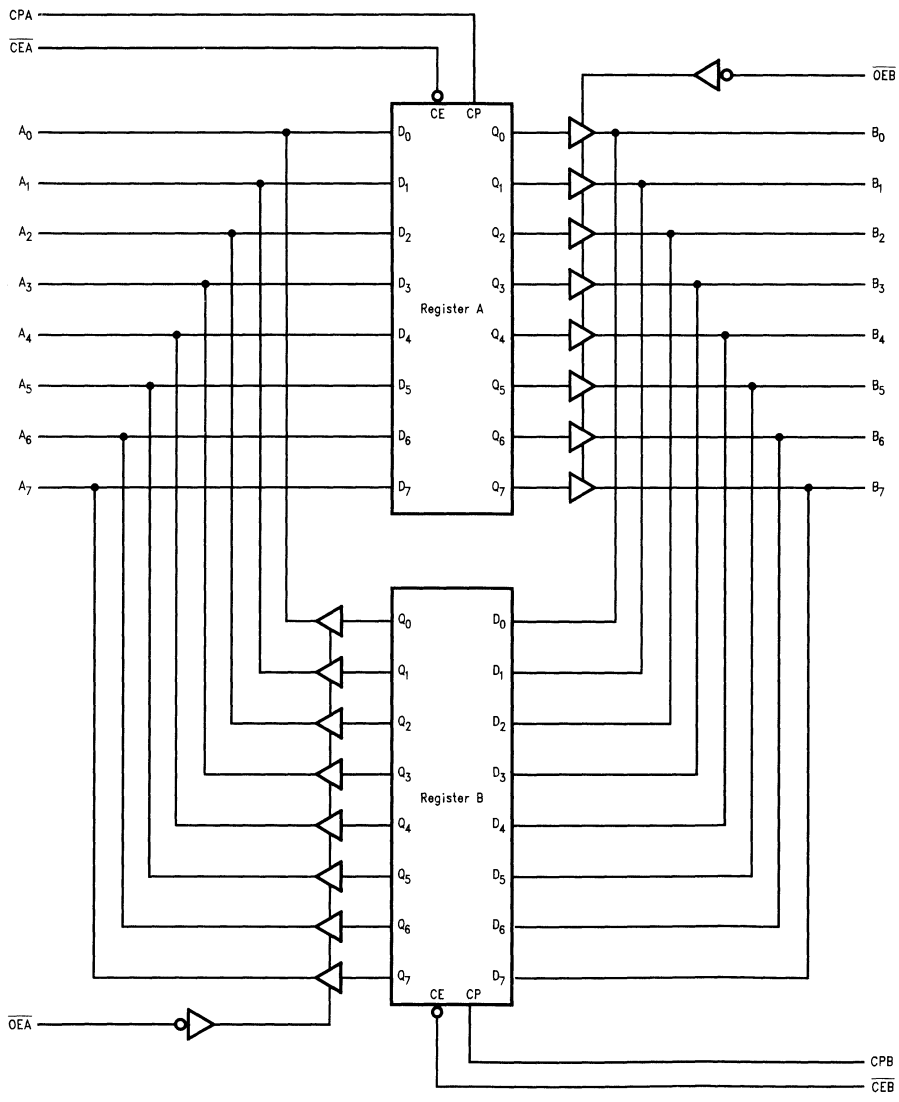
$\overline{OE}$	Internal Q	Output 'LVT2952	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

Block Diagram



TL/F/12452–2

National Semiconductor

PRELIMINARY

74LVT16240
3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/-receiver. The device is nibble controlled.

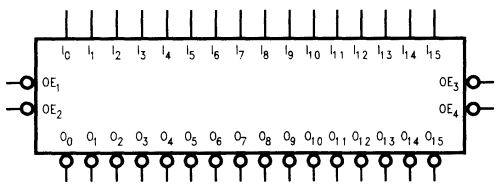
Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12025–1

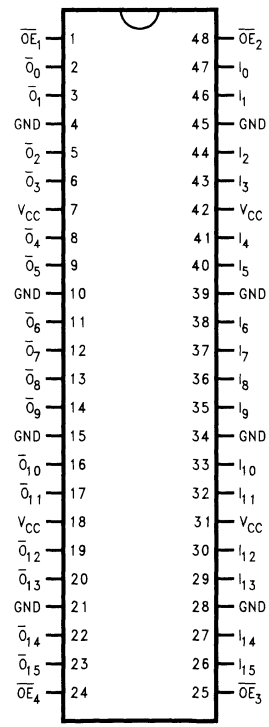
Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LVT16240MEA 74LVT16240MEAX	74LVT16240MTD 74LVT16240MTDX
See NS Package Number	MS48A	MTD48

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Connection Diagram

Pin Assignment for SSOP and TSSOP

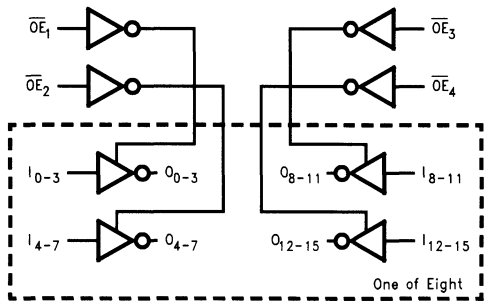


TL/F/12025–2

Functional Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/12025–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level L = Low Voltage Level X = Immaterial Z = High Impedance

9

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at High State	mA
		128	Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
		2.7	2.2			V	I_{OH} = −8 mA
		3.0	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 μA
		2.7			0.5	V	I_{OL} = 24 mA
		3.0			0.4	V	I_{OL} = 16 mA
		3.0			0.5	V	I_{OL} = 32 mA
		3.0			0.55	V	I_{OL} = 64 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ (Note 3)	Max	Units	Conditions
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	V_I = 0.8V
				−75			μA	V_I = 2.0V
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	V_I = 5.5V
			3.6			±1	μA	V_I = 0V or V_{CC}
		Data Pins	3.6			−5	μA	V_I = 0V
						1	μA	V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	μA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Output Current		0–1.2V			±100	μA	V_O = 0.5V to V_{CC} V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	V_O = 0.5V
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	V_O = 3.0V
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			10	μA	V_{CC} < V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			8	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, V_{CC} ≤ V_O ≤ 5.5V, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 3: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	Typ	Max	Units	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.0		4.3 4.3	1.0 1.0	5.2 5.2	ns
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0		5.2 5.2	1.0 1.0	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.8 1.8		5.7 5.1	1.8 1.8	6.3 5.6	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 10)			1.0			ns

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

74LVT16244
3.3V ABT 16-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

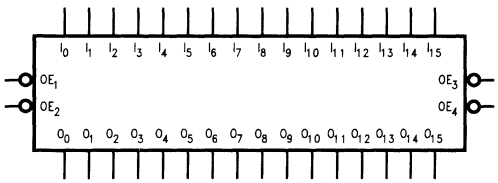
The LVT16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

These bus buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16244
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12019–1

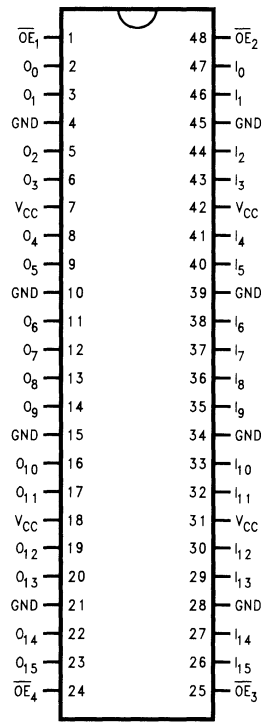
Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LVT16244MEA 74LVT16244MEAX	74LVT16244MTD 74LVT16244MTDX
See NS Package Number	MS48A	MTD48

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12019–2

Functional Description

The LVT16244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

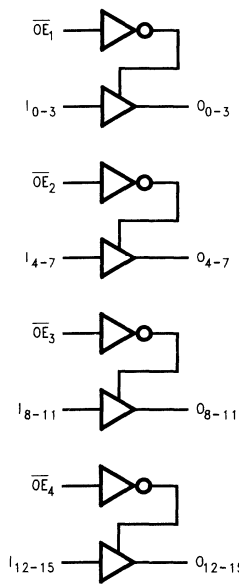
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level L = Low Voltage Level X = Immaterial Z = High Impedance

Logic Diagram



TL/F/12019–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at HIGH State	mA
		128	Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Symbol		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.7	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	mA
T_A	Free Air Operating Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
				Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage		2.7–3.6			0.8	V	
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100\ \mu A$
			2.7	2.2			V	$I_{OH} = -8$ mA
			3.0	2.0			V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7			0.2	V	$I_{OL} = 100\ \mu A$
			2.7			0.5	V	$I_{OL} = 24$ mA
			3.0			0.4	V	$I_{OL} = 16$ mA
			3.0			0.5	V	$I_{OL} = 32$ mA
			3.0			0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	$V_I = 0.8V$
				−75			μA	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	$V_I = 5.5V$
			3.6			±1	μA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6			−5	μA	$V_I = 0V$
						1	μA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0			±100	μA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Current		0–1.2V			±100	μA	$V_O = 0.5V$ to V_{CC}, V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	$V_O = 0.5V$
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	$V_O = 3.0V$
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			10	μA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			8	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, $V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.1	1.0	5.0	ns
t_{PHL}		1.0		4.1	1.0	5.2	
t_{PZH}	Output Enable Time	1.0		5.2	1.0	6.3	ns
t_{PZL}		1.0		5.2	1.0	6.7	
t_{PHZ}	Output Disable Time	1.8		5.7	1.8	6.3	ns
t_{PLZ}		1.8		5.1	1.8	5.6	
t_{OSHL}	Output to Output Skew			1.0			ns
t_{OSLH}	(Note 10)						

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

74LVT16245
3.3V ABT 16-Bit Transceiver with TRI-STATE® Outputs

General Description

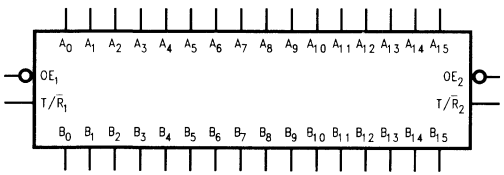
The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

This non-inverting transceiver is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16245
- Latch-up performance exceeds 500 mA

Logic Symbol



TL/F/12020–1

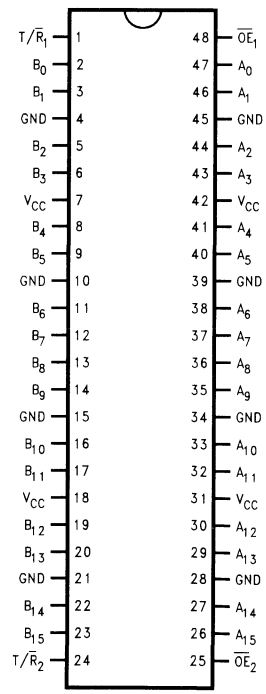
Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/TRI-STATE Outputs
B_0–B_{15}	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LVT16245MEA 74LVT16245MEAX	74LVT16245MTD 74LVT16245MTDX
See NS Package Number	MS48A	MTD48

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12020–2

Functional Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

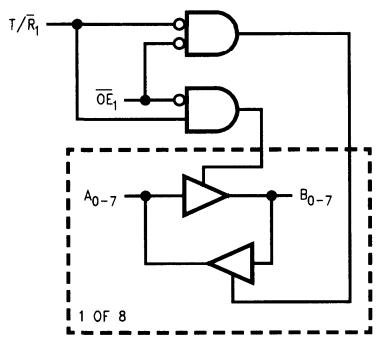
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

H = High Voltage Level L = Low Voltage Level

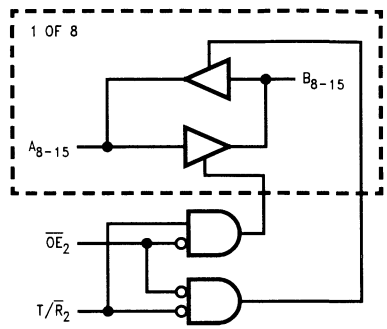
Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

X = Immaterial Z = High Impedance

Logic Diagrams



TL/F/12020–3



TL/F/12020–4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	Output at HIGH State, $V_O > V_{CC}$	mA
		128	Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Ratings must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	mA
T_A	Free-Air Operating Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
				Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage		2.7–3.6			0.8	V	
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100\ \mu A$
			2.7	2.2			V	$I_{OH} = -8$ mA
			3.0	2.0			V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7			0.2	V	$I_{OL} = 100\ \mu A$
			2.7			0.5	V	$I_{OL} = 24$ mA
			3.0			0.4	V	$I_{OL} = 16$ mA
			3.0			0.5	V	$I_{OL} = 32$ mA
			3.0			0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	$V_I = 0.8V$
				−75			μA	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	$V_I = 5.5V$
			3.6			±1	μA	$V_I = 0V$ or V_{CC}
		Data Pins (I/O)	3.6			−5	μA	$V_I = 0V$
						1	μA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0			±100	μA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Output Current		0–1.2			±100	μA	$V_O = 0.5V$ to V_{CC}, V_I = GND or V_{CC}
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			20	μA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			8	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, $V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.1	1.0	5.0	ns
t_{PHL}		1.0		4.1	1.0	5.2	
t_{PZH}	Output Enable Time	1.0		5.3	1.0	6.3	ns
t_{PZL}		1.0		5.2	1.0	6.7	
t_{PHZ}	Output Disable Time	1.8		6.4	1.8	7.2	ns
t_{PLZ}		1.8		5.8	1.8	6.1	
t_{OSHL}	Output to Output Skew			1.0			ns
t_{OSLH}	(Note 10)						

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		8		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

ADVANCE INFORMATION

74LVT16373
3.3V ABT 16-Bit Transparent Latch with TRI-STATE® Outputs

General Description

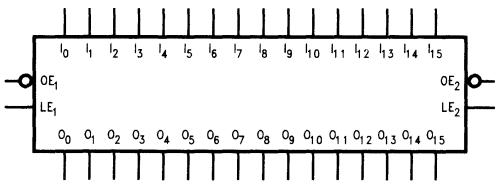
The LVT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA

Logic Symbol



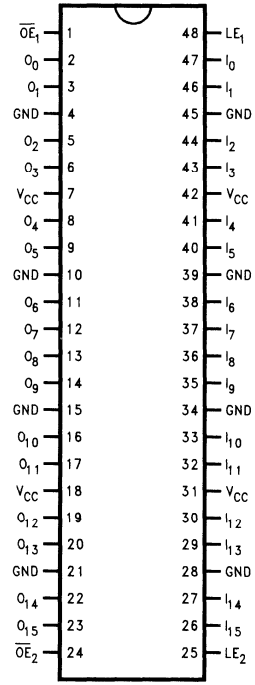
TL/F/12021–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16373MEA 74LVT16373MEAX	74LVT16373MTD 74LVT16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12021–2

Functional Description

The LVT16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

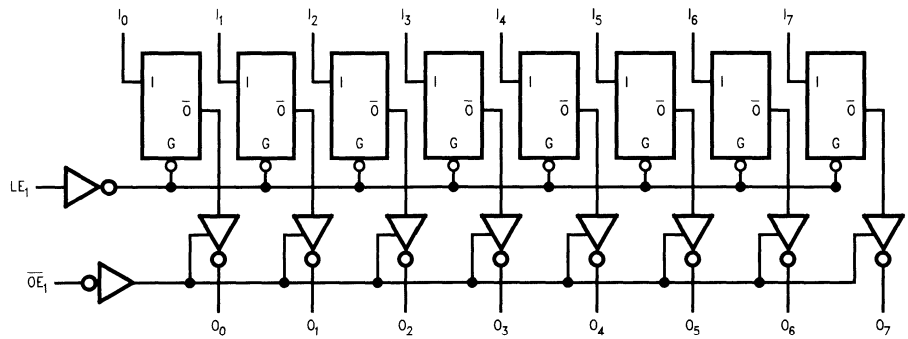
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

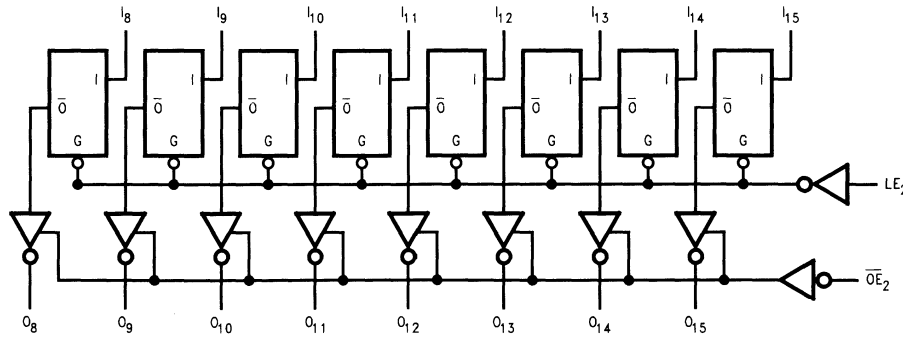
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous output prior to HIGH to LOW transition of LE

Logic Diagrams



TL/F/12021–3



TL/F/12021–4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT16374
3.3V ABT 16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

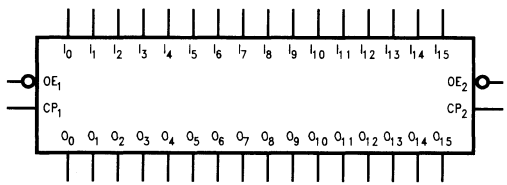
The LVT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

These flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA

Logic Symbol



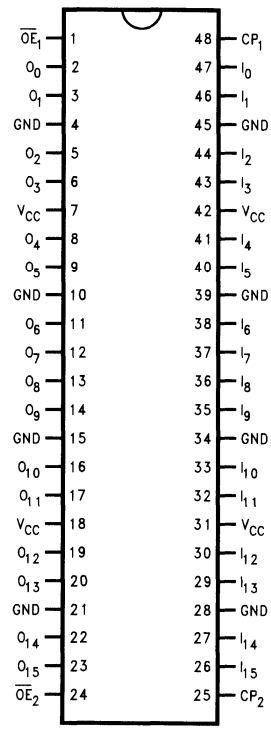
TL/F/12022–1

Pin Names	Description
$\overline{OE}_n$	TRI-STATE Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0–I_{15}	Data Inputs
O_0–O_{15}	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16374MEA 74LVT16374MEAX	74LVT16374MTD 74LVT16374MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12022–2

9

Functional Description

The LVT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

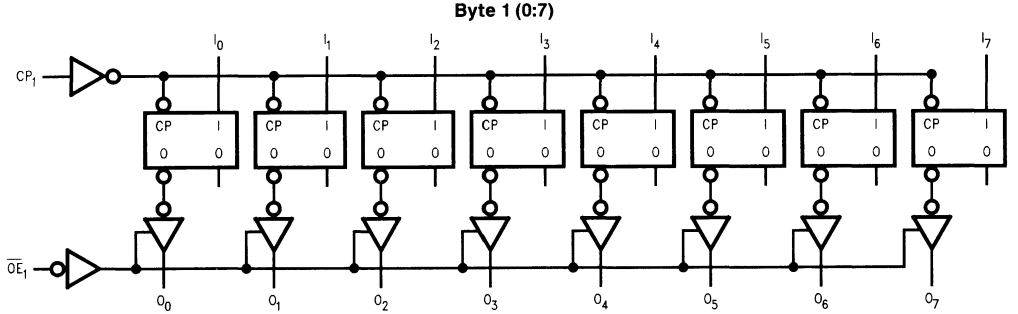
Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW of CP

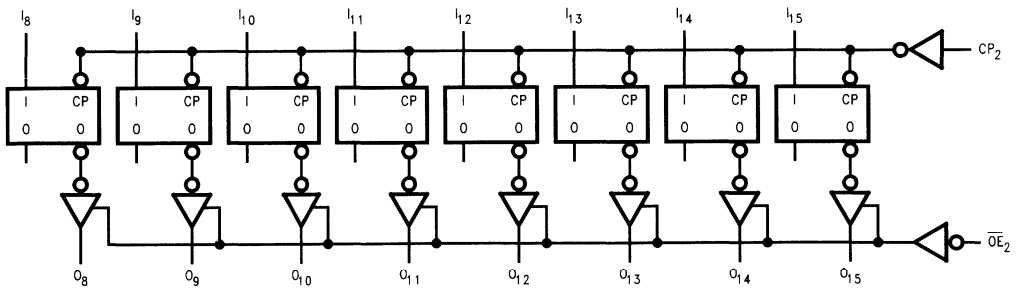
Logic Diagrams

Byte 1 (0:7)



TL/F/12022–3

Byte 2 (8:15)



TL/F/12022–4

Please note that these diagrams are provided for the understanding of logic operaiton and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT16500
3.3V ABT 18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

The LVT16500 consist of eighteen universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16500 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16500
- Latch-up performance exceeds 500 mA

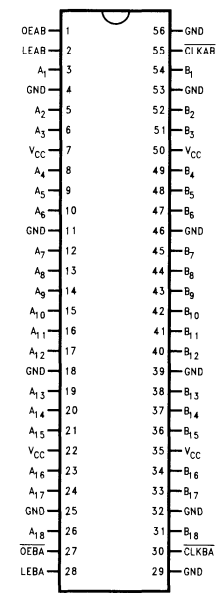
Pin Description

Pin Names	Description
A_0–A_{17}	Data Register A Inputs/TRI-STATE Outputs
B_0–B_{17}	Data Register B Inputs/TRI-STATE Outputs
$\overline{\text{CLKAB}}$, $\overline{\text{CLKBA}}$	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEAB, $\overline{\text{OEBA}}$	Output Enable Inputs

	SSOP EIAJ	TSSOP
Order Number	74LVT16500MEA 74LVT16500MEAX	74LVT16500MTD 74LVT16500MTDX
NS Package Number	MS56A	MTD56

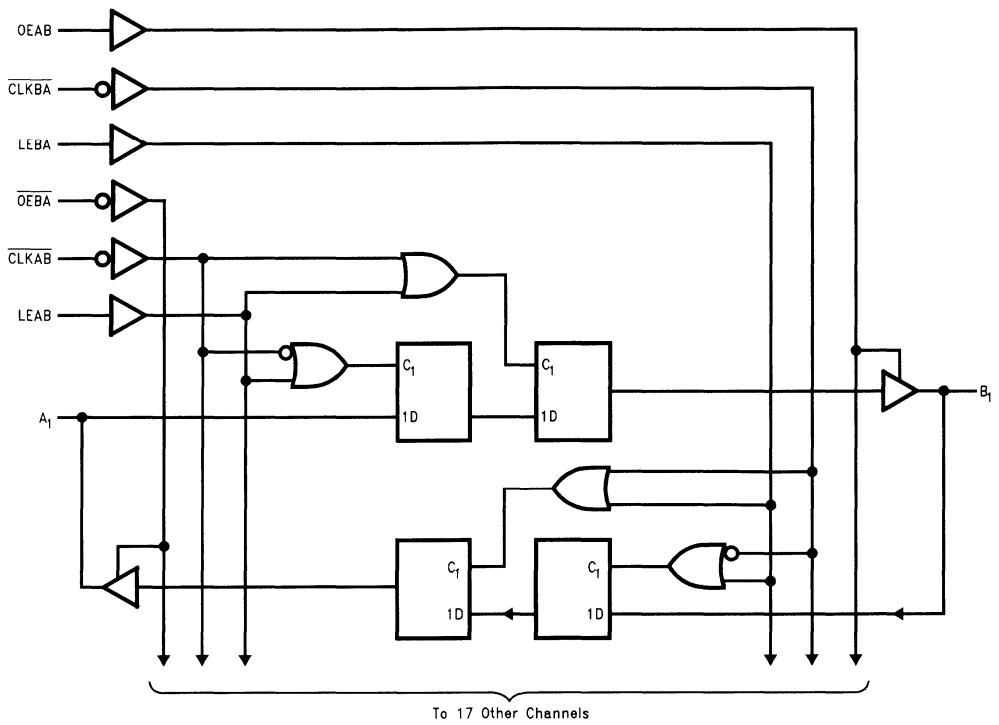
Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12447–1

Logic Diagram



TL/F/12447–2

Function Table†

Inputs				Output
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

National Semiconductor

ADVANCE INFORMATION

74LVT16543
3.3V ABT 16-Bit Registered Transceiver with TRI-STATE® Outputs

General Description

The 'LVT16543 16-bit transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16543 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

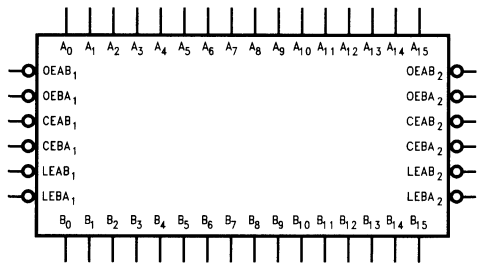
Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16543
- Latch-up performance exceeds 500 mA

Pin Descriptions

Pin Names	Description
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A TRI-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Logic Symbol

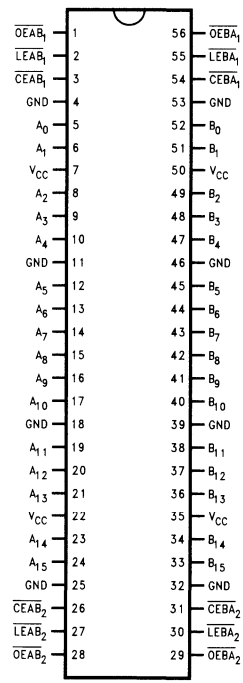


TL/F/12449–1

	SSOP EIAJ	TSSOP
Order Number	74LVT16543MEA 74LVT16543MEAX	74LVT16543MTD 74LVT16543MTDX
NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12449–2

Functional Description

The 'LVT16543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$. Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

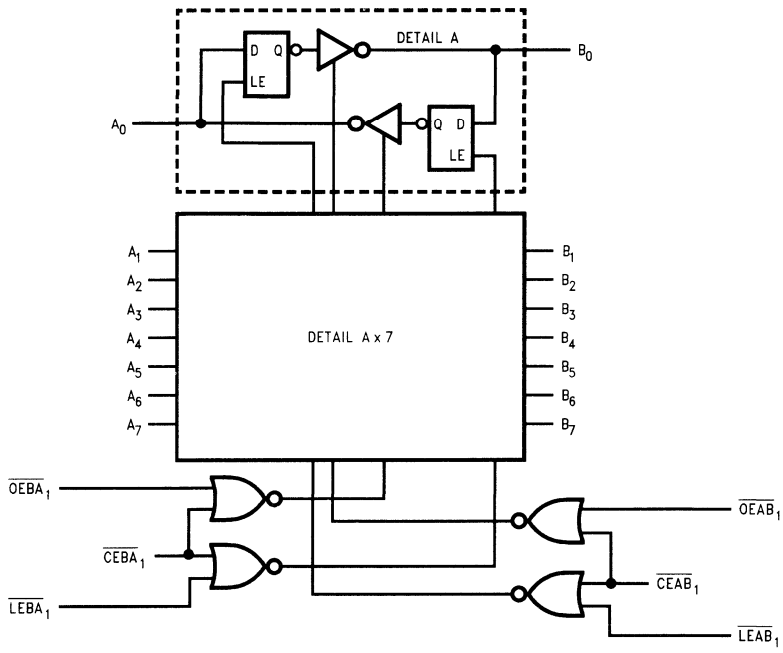
Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

Logic Diagrams

Byte 1 (0:7)

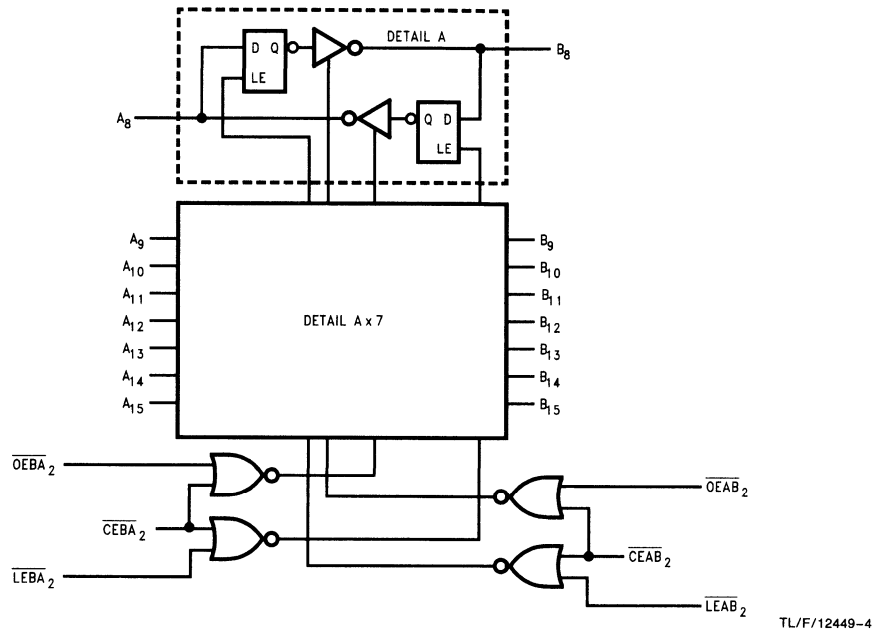


TL/F/12449–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

Byte 2 (8:15)



TL/F/12449–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT16646
3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

General Description

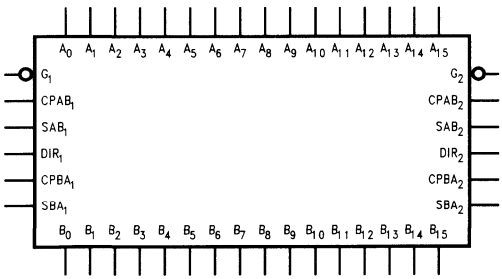
The LVT16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA

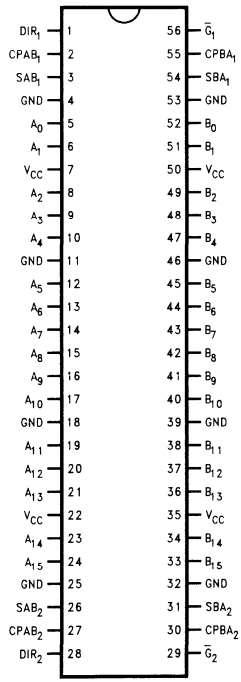
Logic Symbol



TL/F/12023–1

Connection Diagram

Pin Assignment for SSOP and TSSOP

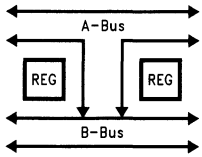


TL/F/12023–2

	SSOP	TSSOP JEDEC
Order Number	74LVT16646MEA 74LVT16646MEAX	74LVT16646MTD 74LVT16646MTDX
See NS Package Number	MS56A	MTD56

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

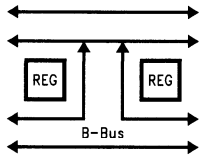
Real Time Transfer A-Bus to B-Bus



TL/F/12023–3

FIGURE 1

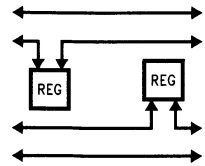
Real Time Transfer B-Bus to A-Bus



TL/F/12023–4

FIGURE 2

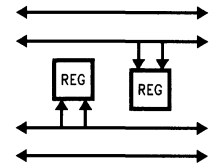
Storage from Bus to Register



TL/F/12023–5

FIGURE 3

Transfer from Register to Bus



TL/F/12023–6

FIGURE 4

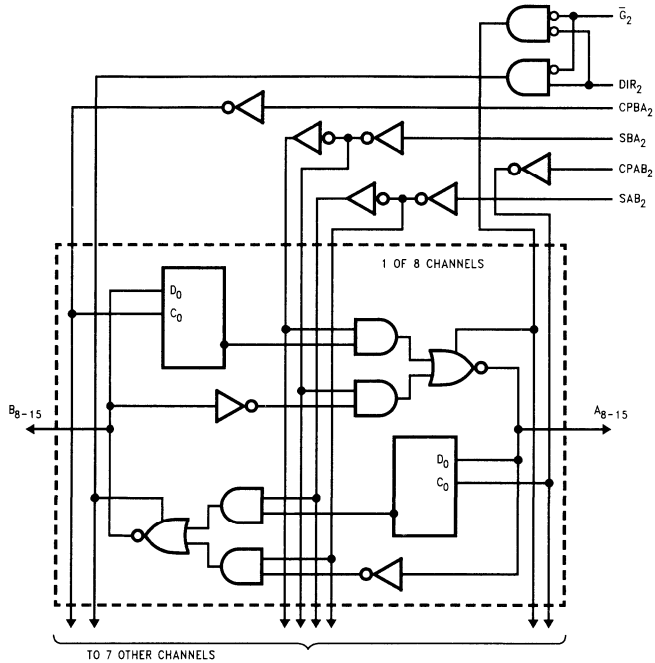
Truth Table (Note)

Inputs						Data I/O		Output Operation Mode
G_1	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock An Data into A Register
H	X	X	↑	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↑	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↑	X	H			Clock Bn into B Register and Output to An

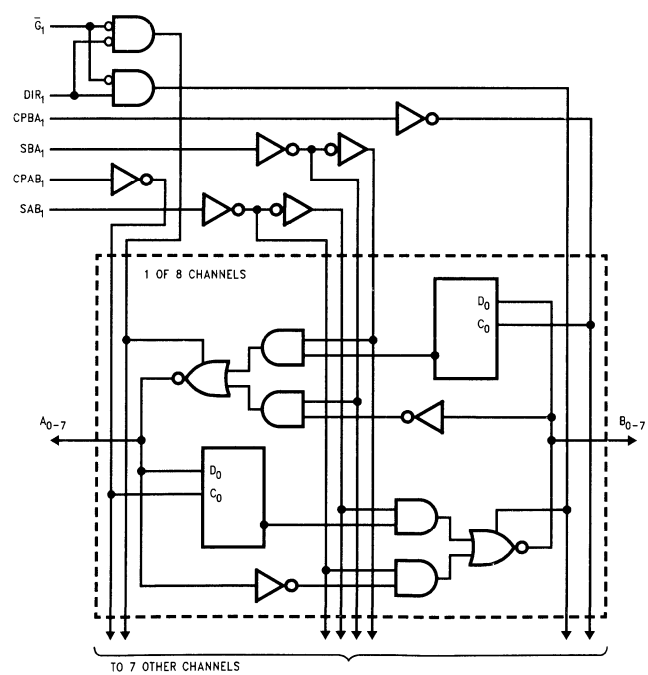
Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level ↑ = LOW-to-HIGH Transition.

Logic Diagram



TL/F/12023–7



TL/F/12023–8

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

National Semiconductor

ADVANCE INFORMATION

74LVT16652
3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

General Description

The LVT16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

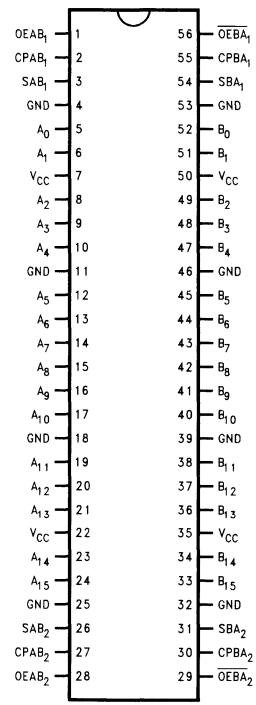
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 500 mA

Pin Names	Description
A_0–A_{16}	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_{16}	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LVT16652MEA 74LVT16652MEAX	74LVT16652MTD 74LVT16652MTDX
NS Package Number	MS56A	MTD56

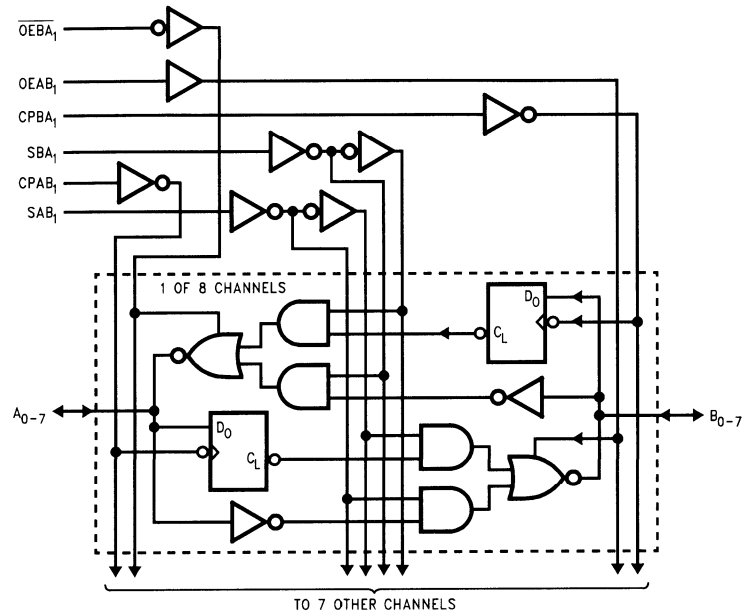
Connection Diagram

Pin Assignment for SSOP and TSSOP

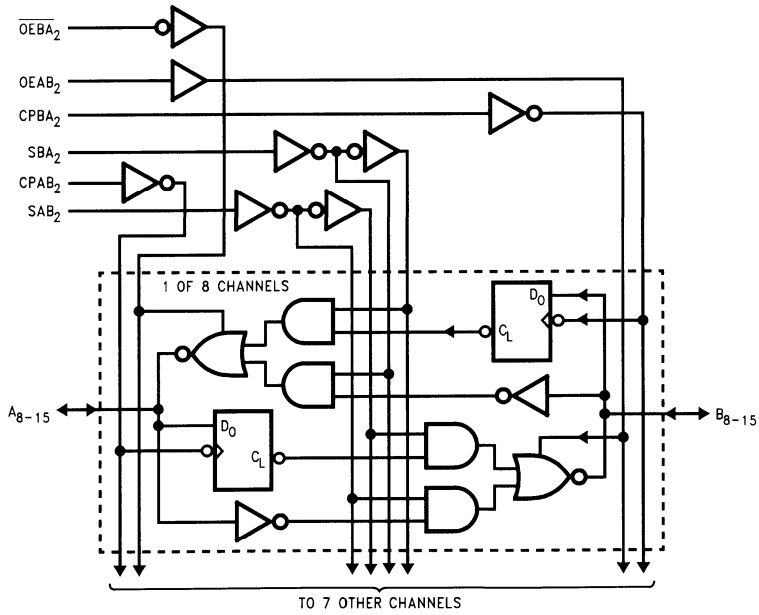


TL/F/12024–1

Logic Diagrams



TL/F/12024–2



TL/F/12024–3

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the LVT16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

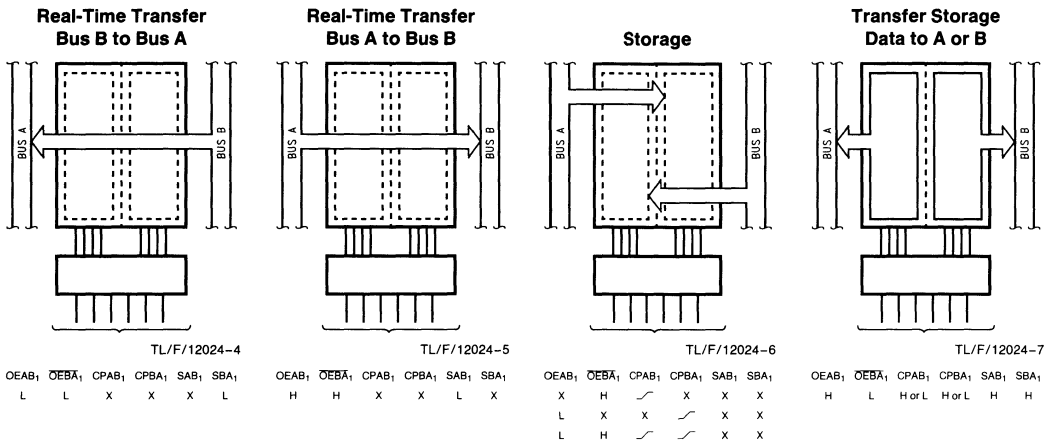


FIGURE 1

Truth Table (Note)

Inputs						Inputs/Outputs		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

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National Semiconductor

ADVANCE INFORMATION

74LVT162240
3.3V ABT 16-Bit Buffer/Line Driver with 25Ω Resistors in TRI-STATE® Outputs

General Description

The LVT162240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

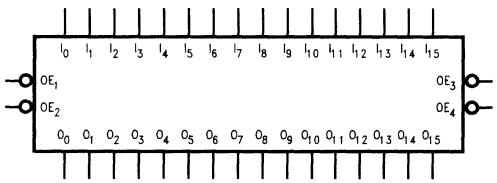
The LVT162240 is designed with 25Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

These bus buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs include series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 162240
- Latch-up performance exceeds 500 mA

Logic Symbol



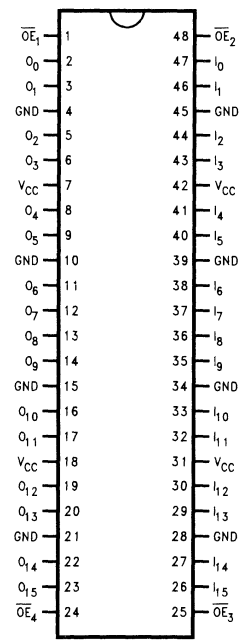
TL/F/12490–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LVT162240MEA 74LVT162240MEAX	74LVT162240MTD 74LVT162240MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

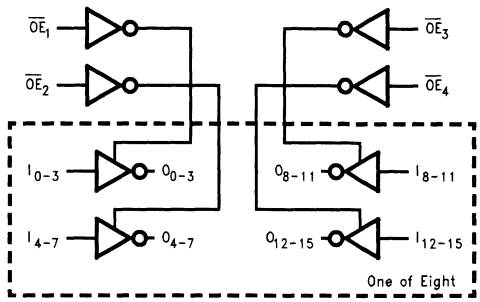


TL/F/12490–2

Functional Description

The LVT162240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/12490–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level L = Low Voltage Level X = Immaterial Z = High Impedance

9

National Semiconductor

ADVANCE INFORMATION

74LVT162244
3.3V ABT 16-Bit Buffer/Line Driver with 25Ω Resistors in TRI-STATE® Outputs

General Description

The LVT162244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

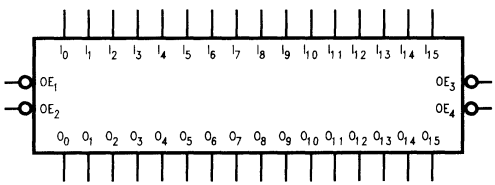
The LVT 162244 is designed with 25Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

These bus buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs include series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 162244
- Latch-up performance exceeds 500 mA

Logic Symbol



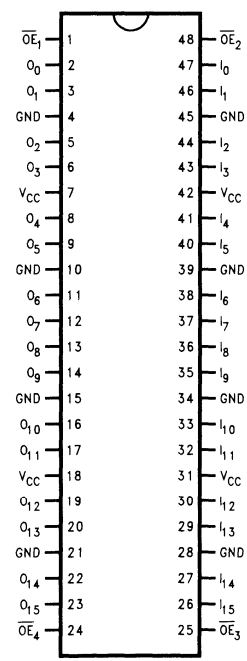
TL/F/12445–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LVT162244MEA 74LVT162244MEAX	74LVT162244MTD 74LVT162244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12445–2

Functional Description

The LVT162244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

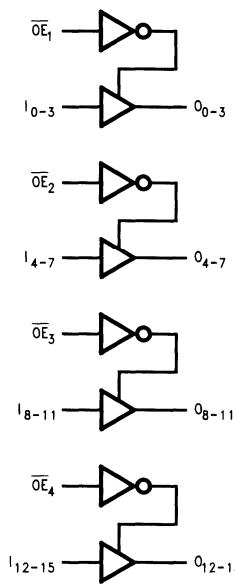
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level L = Low Voltage Level X = Immaterial Z = High Impedance

Logic Diagram



TL/F/12445–3

National Semiconductor

ADVANCE INFORMATION

74LVT162245
3.3V ABT 16-Bit Transceiver with 25Ω Resistors in TRI-STATE® Outputs

General Description

The LVT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

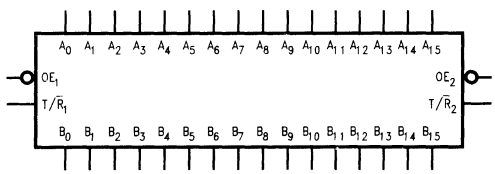
The LVT162245 is designed with 25Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

This non-inverting transceiver is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs include series resistance of 25Ω making external termination resistors unnecessary and reducing overshoot and undershoot
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA

Logic Symbol



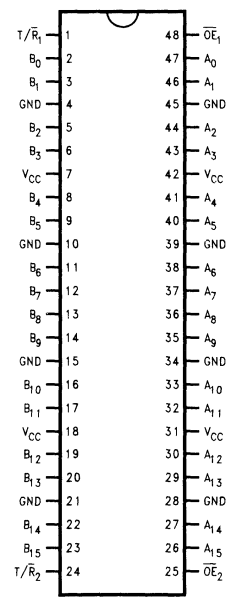
TL/F/12446–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/TRI-STATE Outputs
B_0–B_{15}	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LVT162245MEA 74LVT162245MEAX	74LVT162245MTD 74LVT162245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12446–2

Functional Description

The LVT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

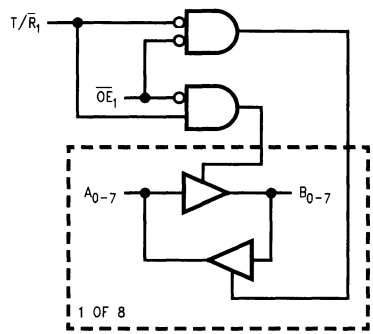
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

H = High Voltage Level L = Low Voltage Level

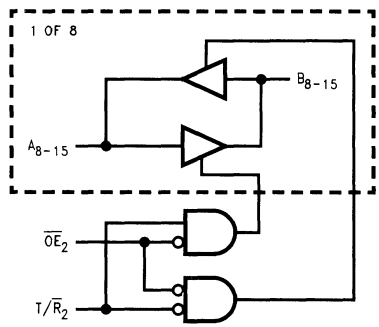
Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

X = Immaterial Z = High Impedance

Logic Diagrams



TL/F/12446–3



TL/F/12446–4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Section 10

ALCX Family

Section 10 Contents

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National Semiconductor

ALCX
Advanced Low Voltage High Speed CMOS Logic with 5V Tolerant Inputs and Outputs

Features	Benefits
5V tolerant inputs and outputs	Interfaces seamlessly to 3V and/or 5V devices
High speed (3.6 ns max t_{PD})	Talks to the latest high speed processor buses
Very low static (20 μA) and dynamic power	Saves power, extends battery life
Power up/down high impedance inputs and outputs	Facilitates power management and live insertion
Extended 2.0V–3.6V V_{CC} supply voltage operation	Fully characterized for unregulated battery operation
Bus hold on input, I/O, and control pins	Eliminates the need for pull-up resistors
Balanced $\pm$24 mA output drive	Drives transmission lines down to 50Ω
Patented Quiet Series™ noise reduction circuitry	Low ground bounce, overshoot, undershoot, and EMI
TSSOP, and SSOP packaging	Saves board space and weight
Alternate sources available	Standardized products, ensure supply

National Semiconductor

ADVANCE INFORMATION

74ALCX16240
Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

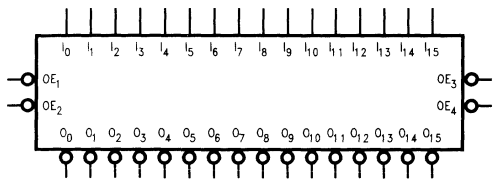
The ALCX16240 contains sixteen inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming less than 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses. ±24 mA output drive means ALCX devices can drive all but the heaviest bus and backplane loads quietly due to National's patented Quiet Series™ circuitry.

Features

- 3.6 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Bus hold
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



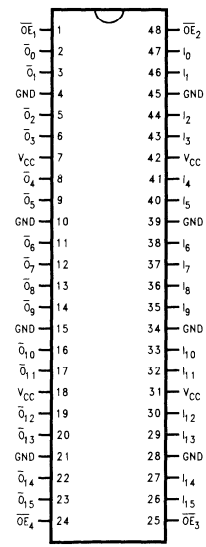
TL/F/12476–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	Outputs

	SSOP	TSSOP
Order Number	74ALCX16240MEA 74ALCX16240MEAX	74ALCX16240MTD 74ALCX16240MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

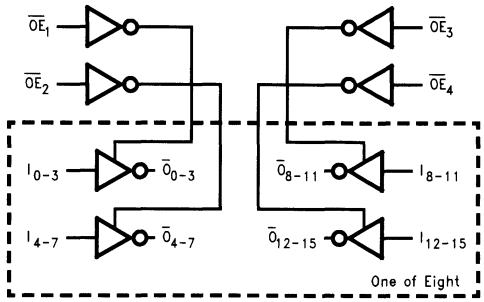


TL/F/12476–2

Functional Description

The ALCX16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/12476–3

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

10

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter		Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
					Min	Max	
V_{IH}	HIGH Level Input Voltage			2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage			2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage		I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
			I_{OH} = −12 mA	2.7	2.2		V
			I_{OH} = −18 mA	3.0	2.4		V
			I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage		I_{OL} = 100 μA	2.7–3.6		0.2	V
			I_{OL} = 12 mA	2.7		0.4	V
			I_{OL} = 16 mA	3.0		0.4	V
			I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	Inputs	V_I = 0V or 5.5V	2.7–3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_I (HOLD)	Bushold Leakage Current	$V_I = 0.8V$ $V_I = 2.0V$	3.0	−75 75		μA
I_I (OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

ADVANCE INFORMATION

74ALCX16244
Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

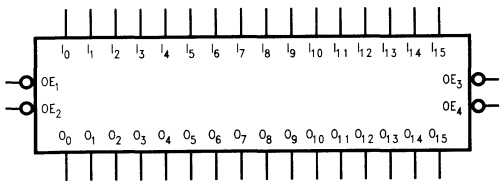
The ALCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming less than 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE® busses. ±24 mA output drive means ALCX devices can drive all but the heaviest bus and backplane loads quietly due to National's patented Quiet Series™ circuitry.

Features

- 3.6 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Bus hold
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



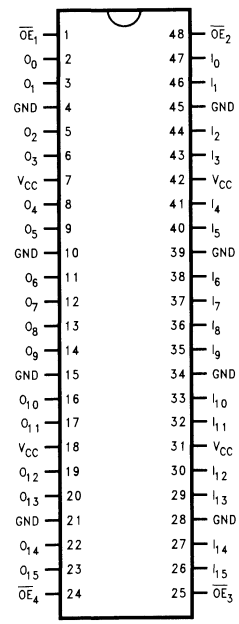
TL/F/12477–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74ALCX16244MEA 74ALCX16244MEAX	74ALCX16244MTD 74ALCX16244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12477–2

Functional Description

The ALCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

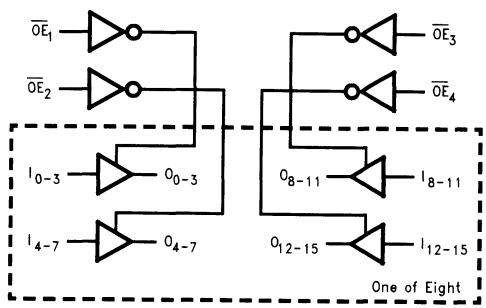
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12477–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Conditions	Value	Units
V_{CC}	Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage	Output in TRI-STATE	−0.5 to +7.0	V
		Output in High or Low State (Note 2)	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
		V_O > V_{CC}	+50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature		−65 to +150	°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	V_I = 0V or 5.5V	2.7–3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_I (HOLD)	Bushold Leakage Current	$V_I = 0.8V$	3.0	−75		μA
		$V_I = 2.0V$	3.0	75		
I_I (OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increases in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 3)	Min	Max (Note 3)	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	3.6 3.6	1.5 1.5	4.5 4.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 4)		0.5 0.5			ns

Note 3: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 4: Skew is defined as the absolute value of the difference between the actual propagaton delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

ADVANCE INFORMATION

74ALCX162244
Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

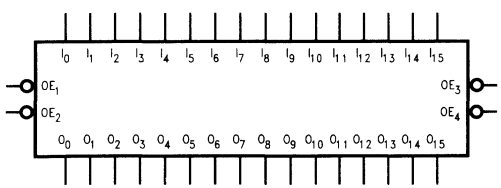
The ALCX162244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation. The 30Ω series resistor helps reducing output overshoot and undershoot.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming less than 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses.

Features

- 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 30Ω series resistor on outputs
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Bus hold
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 162244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

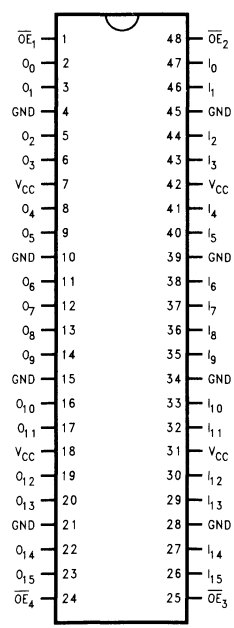


TL/F/12477–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12477–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Conditions	Value	Units
V_{CC}	Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage	Output in TRI-STATE	−0.5 to +7.0	V
		Output in High or Low State (Note 2)	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
		V_O > V_{CC}	+50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature		−65 to +150	°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current			±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −12 mA	3.0	2.0		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 12 mA	3.0		0.8	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		+5.0	μA
I_I(HOLD)	Bushold Leakage Current	V_I = 0.8V	3.0	−75		μA
		V_I = 2.0V		75		
I_I(OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V, V_I = V_{IH} or V_{IL}	2.7–3.6		+5.0	μA
I_{OFF}	Power-Off Leakage Current	0 ≤ V_I, V_O ≤ 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increases in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

National Semiconductor

ADVANCE INFORMATION

74ALCX16245
Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

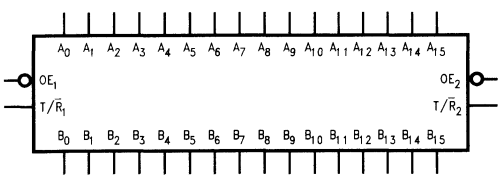
The ALCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming < 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses. ±24 mA output drive means ALCX devices can drive all but the heaviest bus and backplane loads quietly due to National's patented Quiet Series™ circuitry.

Features

- 3.6 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Bus hold
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



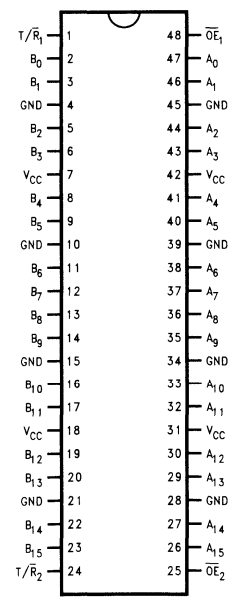
TL/F/12478–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or TRI-STATE Outputs
B_0–B_{15}	Side B Inputs or TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74ALCX16245MEA 74ALCX16245MEAX	74ALCX16245MTD 74ALCX16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12478–2

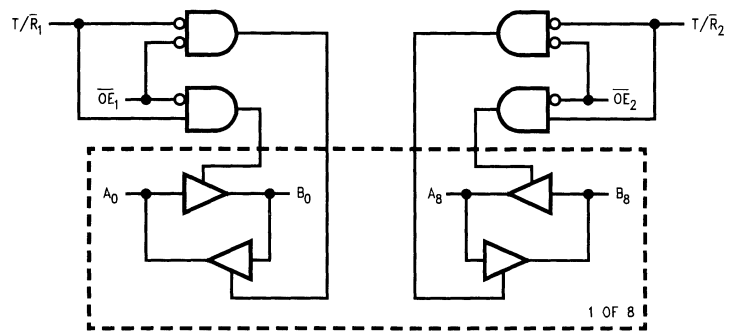
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12478–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter		Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
					Min	Max	
V_{IH}	HIGH Level Input Voltage			2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage			2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage		I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
			I_{OH} = −12 mA	2.7	2.2		V
			I_{OH} = −18 mA	3.0	2.4		V
			I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage		I_{OL} = 100 μA	2.7–3.6		0.2	V
			I_{OL} = 12 mA	2.7		0.4	V
			I_{OL} = 16 mA	3.0		0.4	V
			I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	Inputs I/O	V_I = 0V or 5.5V $V_{I/O}$ = 0V or 5.5V	2.7–3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_I (HOLD)	Bushold Leakage Current	$V_I = 0.8V$ $V_I = 2.0V$	3.0	−75 75		μA
I_I (OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE I/O Leakage	$V_O = 0V$ or 5.5V $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 3)	Min	Max (Note 3)	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	3.6 3.6	1.5 1.5	4.5 4.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 4)		0.5 0.5			ns

Note 3: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 4: Skew is defined as the absolute value of the difference between the actual propagaton delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

ADVANCE INFORMATION

74ALCX162245
Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

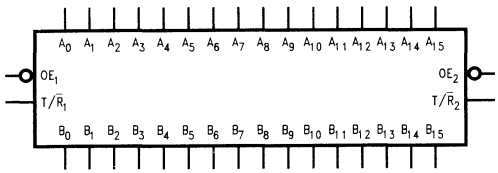
The ALCX162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state. The 30Ω series resistor helps reducing output overshoot and undershoot.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming < 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses.

Features

- 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- 30Ω series resistor on outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Bus hold
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Logic Symbol

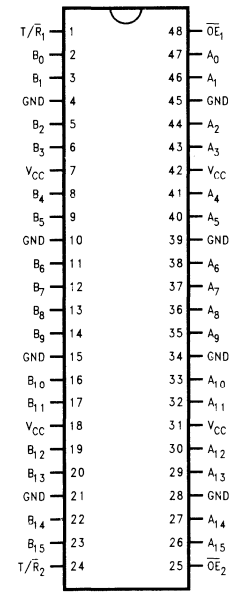


TL/F/12610–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or TRI-STATE Outputs
B_0–B_{15}	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12610–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current			±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OL} = −12 mA	3.0	2.0		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 12 mA	3.0		0.8	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_I(HOLD)	Bushold Leakage Current	V_I = 0.8V V_I = 2.0V	3.0	−75 75		μA
I_I(OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	0 ≤ V_I, V_O ≤ 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increases in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

National Semiconductor

ADVANCE INFORMATION

74ALCX16373
Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

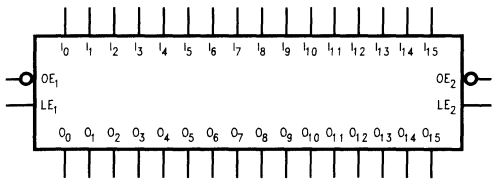
The ALCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming < 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses. ±24 mA output drive means ALCX devices can drive all but the heaviest bus and backplane loads quietly due to National's patented Quiet Series™ circuitry.

Features

- 4.4 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Bus hold
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



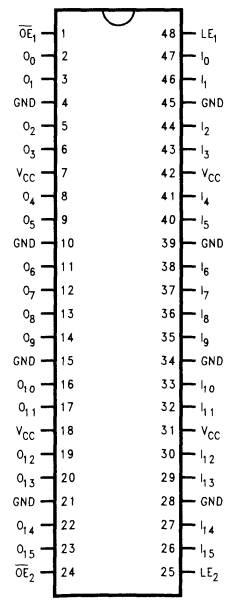
TL/F/12479–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74ALCX16373MEA 74ALCX16373MEAX	74ALCX16373MTD 74ALCX16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12479–2

Functional Description

The ALCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

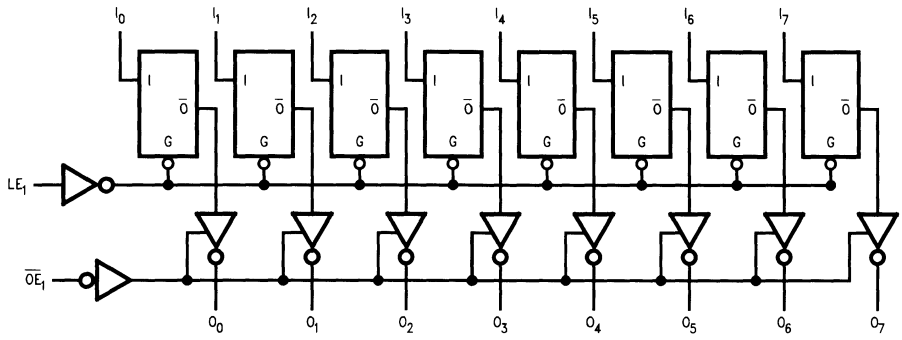
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

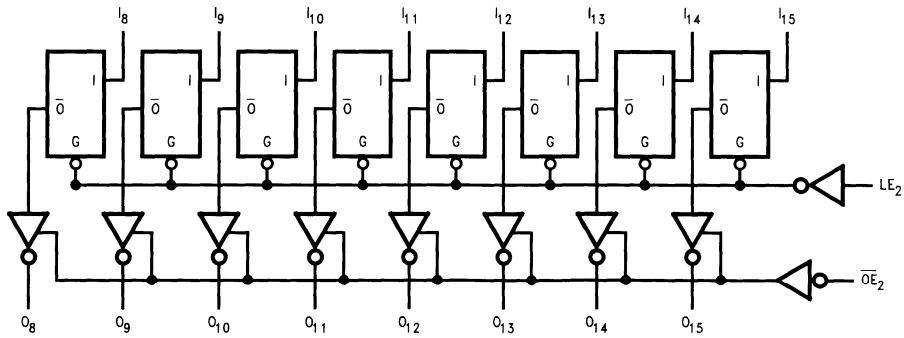
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



TL/F/12479–3



TL/F/12479–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Conditions	Value	Units
V_{CC}	Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage	Output in TRI-STATE	−0.5 to +7.0	V
		Output in High or Low State (Note 2)	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
		V_O > V_{CC}	+50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature		−65 to +150	°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	V_I = 0V or 5.5V	2.7–3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_I (HOLD)	Bushold Leakage Current	$V_I = 0.8V$	3.0	−75		μA
		$V_I = 2.0V$	3.0	75		
I_I (OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

National Semiconductor

ADVANCE INFORMATION

74ALCX16374
Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

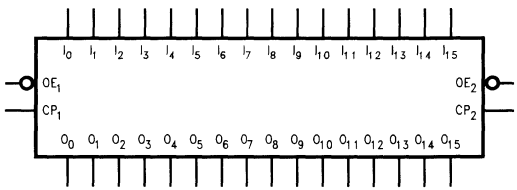
The ALCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (CE) are common to each byte and can be shorted together for full 16-bit operation.

The ALCX family of devices excel in bus interface applications where very high speeds and low power consumption are required. ALCX devices are capable of interfacing to the latest high-speed busses while consuming less than 20 μA of quiescent current. In keeping with National's *CROSSVOLT*™ philosophy, ALCX inputs and outputs are 5V tolerant allowing them to interface to both 3V and 5V components. ALCX inputs and outputs also power up/down in the high impedance state, facilitating power management and live insertion system features. Bus hold on all input, I/O, and control pins removes the need for power-hungry pull-up resistors on TRI-STATE busses. ±24 mA output drive means ALCX devices can drive all but the heaviest bus and backplane loads quietly due to National's patented Quiet Series™ circuitry.

Features

- 4.8 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power up/down high impedance inputs and outputs
- Supports live insertion/withdrawal
- Supports power management
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Bus hold
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Logic Symbol



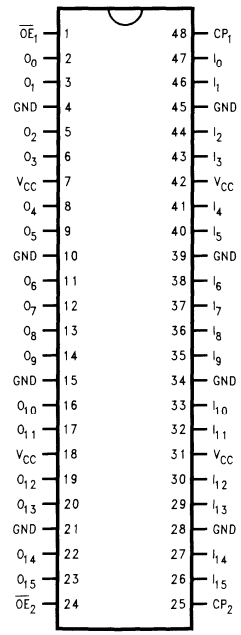
TL/F/12480–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74ALCX16374MEA 74ALCX16374MEAX	74ALCX16374MTD 74ALCX16374MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12480–2

Functional Description

The ALCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

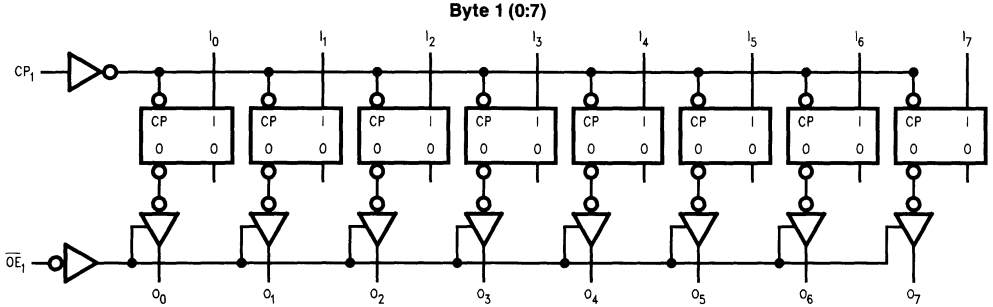
Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW of CP

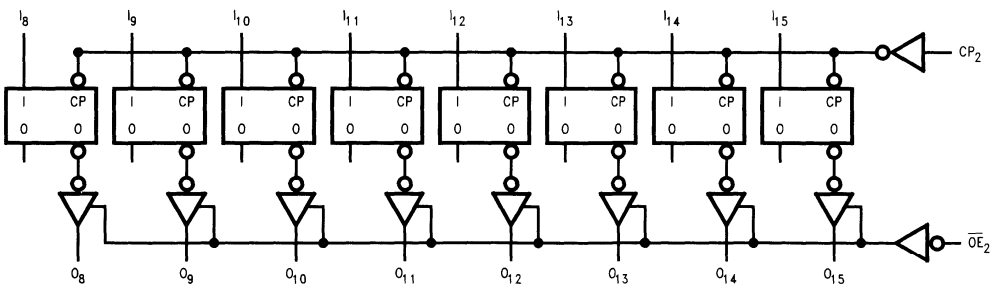
Logic Diagrams

Byte 1 (0:7)



TL/F/12480–3

Byte 2 (8:15)



TL/F/12480–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Conditions	Value	Units
V_{CC}	Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage	Output in TRI-STATE	−0.5 to +7.0	V
		Output in High or Low State (Note 2)	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
		V_O > V_{CC}	+50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature		−65 to +150	°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	V_I = 0V or 5.5V	2.7–3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_I (HOLD)	Bushold Leakage Current	$V_I = 0.8V$	3.0	−75		μA
		$V_I = 2.0V$	3.0	75		
I_I (OD)	Bushold Overdrive Current		3.0	±500		μA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \le V_I, V_O \le 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	μA

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

Section 11

GTL Family

Section 11 Contents

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National Semiconductor

GTL Family
GTL/TTL Universal Bus Transceivers

Features	Advantages
Process, Voltage, and Temperature (PVT) compensated active GTL edge rate control	Clean and consistent system performance
Very precise (±50 mV) GTL receiver input threshold	Extremely wide noise margins, enhanced system reliability
Controlled GTL V_{OL} which hardly varies with changes in output load	Low skew at outputs for improved system speed
Optimized GTLP (GTLplus) versions available	Even lower skew for better system performance
Supply level detection circuitry	maintains TTL/LVTTL compatibility at 3V/5V configurable supply range and allows an easy migration path to 3V
5V tolerant when powered at 3V supply	Interfaces with both 3V and 5V TTL devices
Power Up/Down High Impedance	Suitable for live insertion and power managed applications
Bus-hold circuitry on the TTL I/O	Eliminates external pull-up resistors for unused inputs
64/-32 mA TTL output drive current	Capable of driving large TTL memory arrays or backplanes
Submicron Advanced CMOS technology	Low power dissipation
Universal Bus Transceiver	Both TTL and GTL ports are configurable as transparent, latched or clocked
Flow-through 18-bit architecture	Optimization of board layout
Available in standard 56-pin SSOPII and TSSOP packages	Savings of board space and weight

National Semiconductor

PRELIMINARY

GTL16612
CMOS 18-Bit GTL/TTL Universal Bus Transceiver

General Description

The GTL16612 is one in a series of transceivers designed specifically for GTL logic levels. The device is a CMOS GTL 18-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

National's GTL has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. Its function is similar to BTL or conventional GTL but with different driver output levels and receiver threshold.

The device provides TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

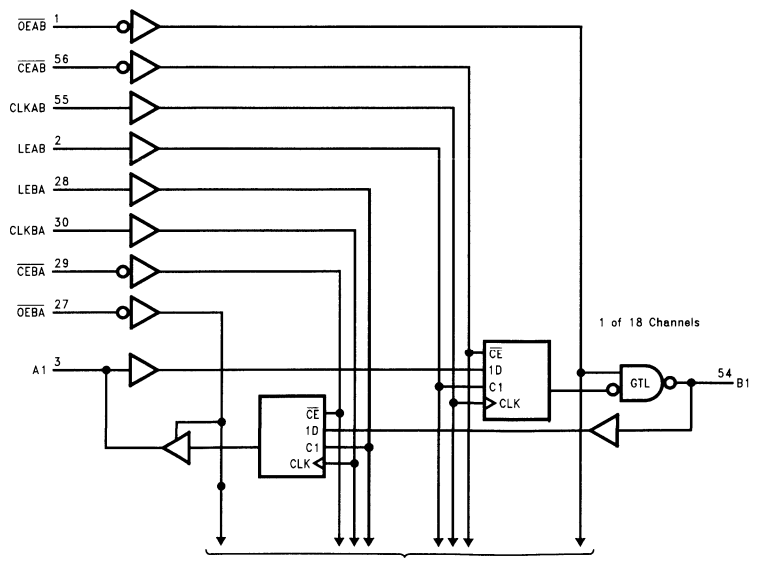
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTL16612 is 100% I/O Spec compatible to conventional GTL.

Features

- Bidirectional interface between GTL and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- V_{REF} pin provides external supply reference voltage for receiver threshold
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



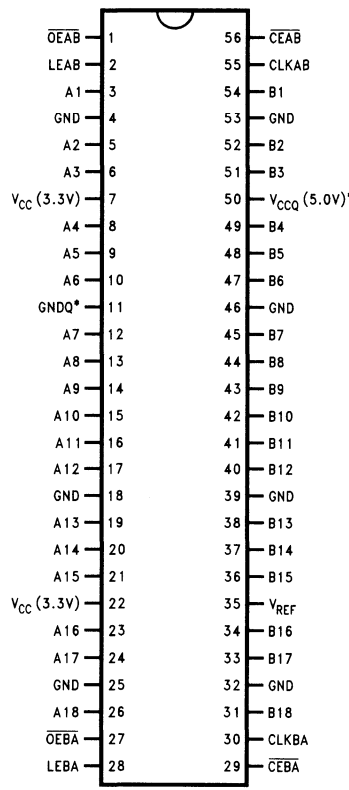
TL/F/12365–2

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{REF}	GTL Input Reference Voltage
A1–A18	A-to-B Data Inputs or B-to-A TRI-STATE Outputs
B1–B18	B-to-A Data Inputs or A-to-B Open Drain Outputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12365–1

Order Number GTL16612MTD or GTL16612MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GNDQ are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 2)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(3)	
L	L	L	L	X	B_0(4)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(4)	Clock inhibit

Note 2: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 3: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 4: Output level before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 6)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into A-port I_{OL}	128 mA
DC Output Source Current from A-port I_{OH}	−64 mA
DC Output Sink Current into B-port in the Low State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: V_{CCQ} and GNDQ are the quiet supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide lower noise performance.

Recommended Operating Conditions

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}(7)	4.75V to 5.25V
V_{REF}	0.8V
Bus Termination Voltage (V_{TT})	1.14V to 1.26V
Input Voltage (V_I)	0.0V to 5.5V
On A-Port and Control Pins	
Input High Voltage (V_{IH})	
B-Port	V_{REF} + 50 mV to V_{TT}
Others	2.0V (min)
Input Low Voltage (V_{IL})	
B-Port	0.0V to V_{REF} − 50 mV
Others	0.8V (max)
High Level Output Current (I_{OH})	
A-Port	−32 mA
Low Level Output Current (I_{OL})	
A-Port	+64 mA
B-Port	+40 mA
Operating Temperature	
T_A	−40°C to +85°C

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OH} = −100 μA	V_{CC} − 0.2			V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OH} = −8 mA	2.4			
			I_{OH} = −32 mA	2.0			
V_{OL}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 24 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B-Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 40 mA			0.4	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 0 or 5.5V			±10	μA
	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = 5.5V			20	μA
			V_I = V_{CCQ}			1	
			V_I = 0			−20	
	B-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	μA
			V_I = 0			−5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	μA
$I_{I(hold)}$	A-Port	V_{CC} = 3.15V, V_{CCA} = 4.75V	V_I = 0.8V	75			μA
			V_I = 2.0V	−75			

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted) (Continued)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
I_{OZH}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.0V			1	μA
	B-Port		V_O = 1.2V			10	
I_{OZL}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−1	μA
	B-Port		V_O = 0.4V			−10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		35	45	mA
			Outputs Low		35	45	
			Outputs Disabled		35	45	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		0.2	1	mA
			Outputs Low		0.2	1	
			Outputs Disabled		0.2	1	
ΔI_{CC} (Note 10)	A Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V			1	mA
C_i	Control Pins		V_I = V_{CCQ} or 0		7		pF
C_{io}	A-Port		V_I = V_{CCQ} or 0		10		
C_{io}	B-Port		Per IEEE1194-1991		8		

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 9: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 10: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Electrical Characteristics

GTL B-port Output Edge Rate over recommended range of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted)

Symbol	Min	Typ (Note 8)	Max	Unit	Conditions
t_{RISE} 0.5V to 1.0V		2.0	2.5	ns	C_L = 5 pF 20% to 80%
t_{FALL} 1.0V to 0.5V		1.3	1.7		

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted)

Symbol			Min	Max	Unit
f_{clock}	Max Clock Frequency		0	100	MHz
t_{width}	Pulse Duration	LEAB or LEBA High	3.3		ns
		CLKAB or CLKBA High or Low	4.8		
t_{SU}	Setup Time	A before CLKAB ↑	0.5		ns
		B before CLKBA ↑	2.5		
		A before LEAB ↓	0.5		
		B before LEBA ↓	2.1		
		$\overline{CEAB}$ before CLKAB ↑	1.0		
		$\overline{CEBA}$ before CLKBA ↑	1.0		
t_{Hold}	Hold Time	A after CLKAB ↑	2.7		ns
		B after CLKBA ↑	0.4		
		A after LEAB ↓	3.4		
		B after LEBA ↓	3.3		
		$\overline{CEAB}$ after CLKAB ↑	1.5		
		$\overline{CEBA}$ after CLKBA ↑	0.4		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted). C_L = 5 pF for B-Port and C_L = 50 pF for A-Port.

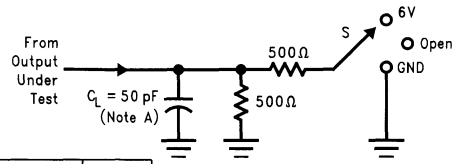
Symbol	From (Input)	To (Output)	Min	Typ (Note 11)	Max	Unit
f_{MAX}			100			MHz
t_{PLH}	A	B	1.0		6.2	ns
t_{PHL}			1.0		5.0	
t_{PLH}	LEAB	B	1.2		7.2	ns
t_{PHL}			1.2		7.0	
t_{PLH}	CLKAB	B	1.0		6.6	ns
t_{PHL}			1.0		5.9	
t_{PLH}	$\overline{OEAB}$	B	1.2		6.0	ns
t_{PHL}			1.2		5.5	
t_{PLH}	B	A	2.3		7.2	ns
t_{PHL}			2.0		6.4	
t_{PLH}	LEBA	A	1.8		7.0	ns
t_{PHL}			1.7		6.7	
t_{PLH}	CLKBA	A	1.8		6.7	ns
t_{PHL}			1.5		5.6	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	2.2		5.5	ns
t_{PHZ}, t_{PLZ}			2.0		6.8	
t_{OSHLA}, t_{OSLHA}	A Port: Output to Output Skew (Note 11)				1.0	ns
t_{OSHLB}, t_{OSLHB}	B Port: Output to Output Skew (Note 11)				1.0	

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5V, and T_A = 25°C.

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameters guaranteed by design.

Test Circuits and Timing Waveforms

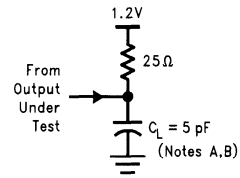
Test Circuit for A Outputs



TL/F/12365-3

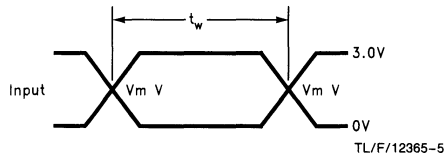
Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Test Circuit for B Outputs



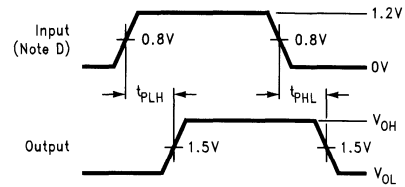
TL/F/12365-4

Voltage Waveforms Pulse Duration (Vm = 1.5V for A Port and 0.8V for B Port)



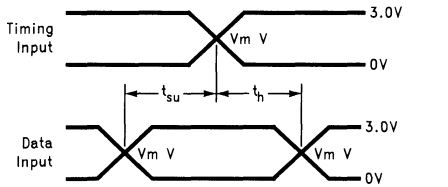
TL/F/12365-5

Voltage Waveforms Propagation Delay Times (B Port to A Port)



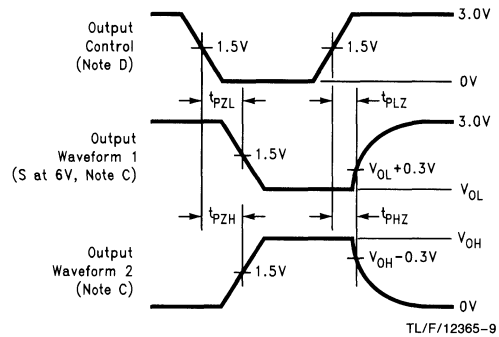
TL/F/12365-8

Voltage Waveforms Setup and Hold Times (Vm = 1.5V for A Port and 0.8V for B Port)



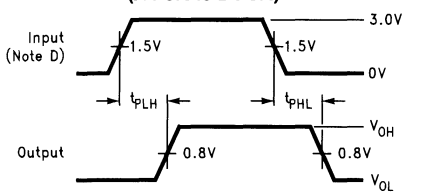
TL/F/12365-6

Voltage Waveforms Enable and Disable Times (A Port)



TL/F/12365-9

Voltage Waveforms Propagation Delay Times (A Port to B Port)



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Note A: C_L includes probes and jig capacitance.

Note B: For B port outputs, C_L = 5 pF is used for worst case edge rate.

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note D: All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

National Semiconductor

PRELIMINARY

GTLP16612
CMOS 18-Bit GTLP/TTL Universal Bus Transceiver

General Description

The GTLP16612 is one in a series of transceivers designed specifically for GTLP logic levels. The device is a CMOS GTLP 18-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

National's GTLP has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. Its function is similar to BTL or conventional GTLP but with different driver output levels and receiver threshold.

The device provides TTL to GTLP translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTLP levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

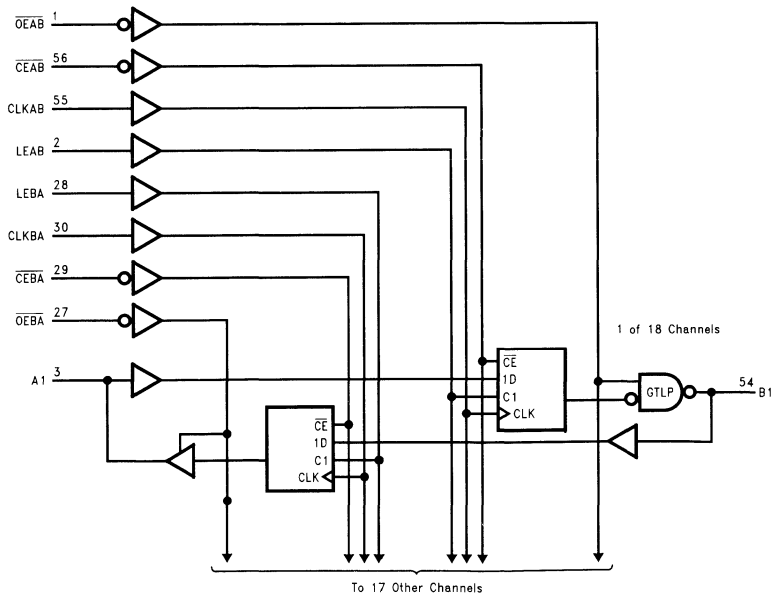
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLP16612 is 100% I/O Spec compatible to enhanced GTLP where the driver output low voltage is typically 0.5V, the output high 1.5V, and the receiver threshold 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- V_{REF} pin provides external supply reference voltage for receiver threshold
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



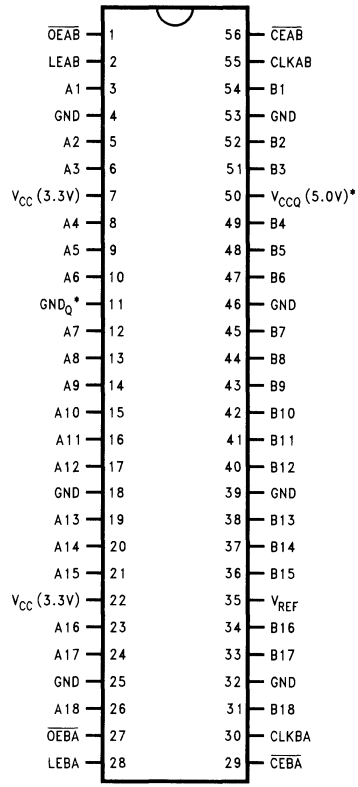
TL/F/12390–1

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{REF}	GTL Input Reference Voltage
A1–A18	A-to-B Data Inputs or B-to-A TRI-STATE Outputs
B1–B18	B-to-A Data Inputs or A-to-B Open Drain Outputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Order Number GTLP16612MTD or GTLP16612MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GND_Q are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GND_Q/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 2)

Inputs					Output B	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(3)	
L	L	L	L	X	B_0(4)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(4)	Clock inhibit

Note 2: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 3: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 4: Output level before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 6)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into A-port I_{OL}	128 mA
DC Output Source Current from A-port I_{OH}	−64 mA
DC Output Sink Current into B-port in the Low State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "*Recommended Operating Conditions*" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: V_{CCQ} and GNDQ are the quiet supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide lower noise performance.

Recommended Operating Conditions

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}(7)	4.75V to 5.25V
V_{REF}	1.0V
Bus Termination Voltage (V_{TT})	1.35V to 1.65V
Input Voltage (V_I)	
on A-Port and Control Pins	0.0V to 5.5V
Input High Voltage (V_{IH})	
B-Port	V_{REF} + 200 mV to V_{TT}
Others	2.0V (min)
Input Low Voltage (V_{IL})	
B-Port	0.0V to V_{REF} − 200 mV
Others	0.8V (max)
High Level Output Current (I_{OH})	
A-Port	−32 mA
Low Level Output Current (I_{OL})	
A-Port	+64 mA
B-Port	+40 mA
Operating Temperature	
T_A	−40°C to +85°C

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OH} = −100 μA	V_{CC} − 0.2			V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OH} = −8 mA	2.4			
			I_{OH} = −32 mA	2.0			
V_{OL}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 24 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B-Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 40 mA			0.55	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 5.5V or 0V			±10	μA
	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = 5.5V			20	μA
			V_I = V_{CC}			1	
			V_I = 0			−20	
	B-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	μA
			V_I = 0			−5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	μA
$I_{I(hold)}$	A-Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	V_I = 0.8V	75			μA
			V_I = 2.0V	−75			

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted) (Continued)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
I_{OZH}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.0V			1	μA
	B-Port		V_O = 1.2V			10	
I_{OZL}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−1	μA
	B-Port		V_O = 0.4V			−10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		35	45	mA
			Outputs Low		35	45	
			Outputs Disabled		35	45	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		0.2	1	mA
			Outputs Low		0.2	1	
			Outputs Disabled		0.2	1	
ΔI_{CC} (Note 10)	A-Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V			1	mA
C_i	Control Pins		V_I = V_{CCQ} or 0		7		pF
C_{io}	A-Port		V_I = V_{CCQ} or 0		10		
C_{io}	B-Port		Per IEEE 1194–1991		8		

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 9: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 10: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Electrical Characteristics

GTLP B-port Output Edge Rate over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted)

Symbol	Min	Typ (Note 1)	Max	Unit	Conditions
t_{RISE}		2.0	2.5	ns	C_L = 5 pF 20% to 80%
t_{FALL}		1.3	1.7		

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted)

Symbol			Min	Max	Unit
f_{clock}	Max Clock Frequency		0	100	MHz
t_{width}	Pulse Duration	LEAB or LEBA High	3.3		ns
		CLKAB or CLKBA High or Low	4.8		
t_{SU}	Setup Time	A before CLKAB ↑	0.5		ns
		B before CLKBA ↑	2.5		
		A before LEAB ↓	0.5		
		B before LEBA ↓	2.1		
		$\overline{CEAB}$ before CLKAB ↑	1.0		
		$\overline{CEBA}$ before CLKBA ↑	1.0		
t_{Hold}	Hold Time	A after CLKAB ↑	2.7		ns
		B after CLKBA ↑	0.4		
		A after LEAB ↓	3.4		
		B after LEBA ↓	3.3		
		$\overline{CEAB}$ after CLKAB ↑	1.5		
		$\overline{CEBA}$ after CLKBA ↑	0.4		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted). C_L = 5 pF for B-Port and C_L = 50 pF for A-Port.

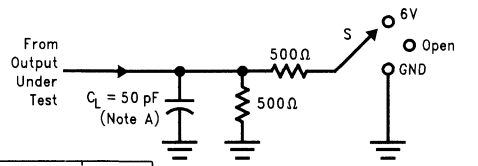
Symbol	From (Input)	To (Output)	Min	Typ (Note 8)	Max	Unit
f_{MAX}			100			MHz
t_{PLH}	A	B	1.0		6.2	ns
t_{PHL}			1.0		5.0	
t_{PLH}	LEAB	B	1.2		7.2	ns
t_{PHL}			1.2		7.0	
t_{PLH}	CLKAB	B	1.0		6.6	ns
t_{PHL}			1.0		5.9	
t_{PLH}	$\overline{OEAB}$	B	1.2		6.0	ns
t_{PHL}			1.2		5.5	
t_{PLH}	B	A	2.3		7.2	ns
t_{PHL}			2.0		6.4	
t_{PLH}	LEBA	A	1.8		7.0	ns
t_{PHL}			1.7		6.7	
t_{PLH}	CLKBA	A	1.8		6.7	ns
t_{PHL}			1.5		5.6	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	2.2		5.5	ns
t_{PHZ}, t_{PLZ}			2.0		6.8	
t_{OSHLA}, t_{OSLHA}	A Port: Output to Output Skew (Note 11)				1.0	ns
t_{OSHLB}, t_{OSLHB}	B Port: Output to Output Skew (Note 11)				1.0	

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameters guaranteed by design.

Test Circuits and Timing Waveforms

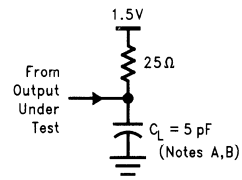
Test Circuit for A Outputs



TL/F/12390-3

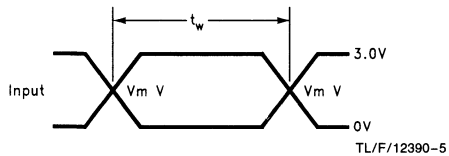
Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Test Circuit for B Outputs



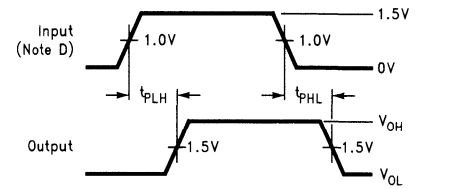
TL/F/12390-4

Voltage Waveforms Pulse Duration (Vm = 1.5V for A Port and 1.0V for B Port)



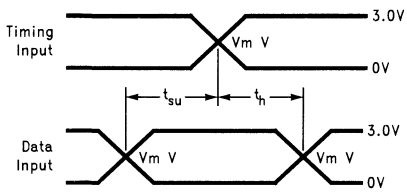
TL/F/12390-5

Voltage Waveforms Propagation Delay Times (B Port to A Port)



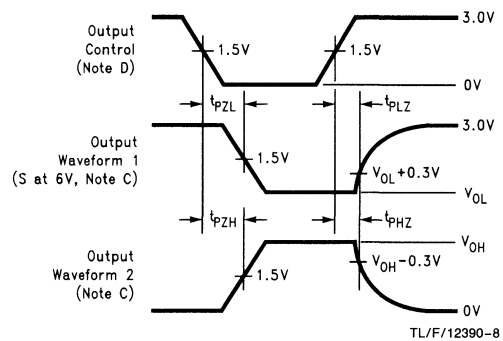
TL/F/12390-6

Voltage Waveforms Setup and Hold Times (Vm = 1.5V for A Port and 1.0V for B Port)



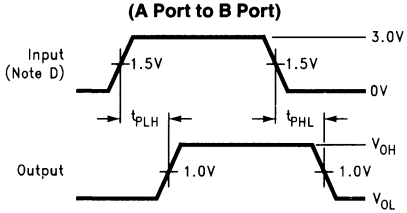
TL/F/12390-7

Voltage Waveforms Enable and Disable Times (A Port)



TL/F/12390-8

Voltage Waveforms Propagation Delay Times (A Port to B Port)



TL/F/12390-9

Note A: C_L includes probes and jig capacitance.

Note B: For B port outputs, C_L = 5 pF is used for worst case edge rate.

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note D: All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

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ADVANCE INFORMATION

GTLE16612 CMOS 18-Bit GTL/TTL Universal Bus Transceiver with Output Edge Rate Control

General Description

The GTLE16612 is one in a series of transceivers designed specifically for GTL logic levels. The device is a CMOS GTL 18-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

The pin programmable GTL "E" edge rate control feature allows the system designer to minimize noise and maximize speed of the system. The V_{ERC} pin (pin 35) is used for this purpose and provides three different edge rates depending on the V_{ERC} pin voltage (high, low, or floating). Voltage changes at the V_{ERC} pin will be reflected at the output within about 100 ns allowing the edge rate to be controlled during system operation.

The device provides TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

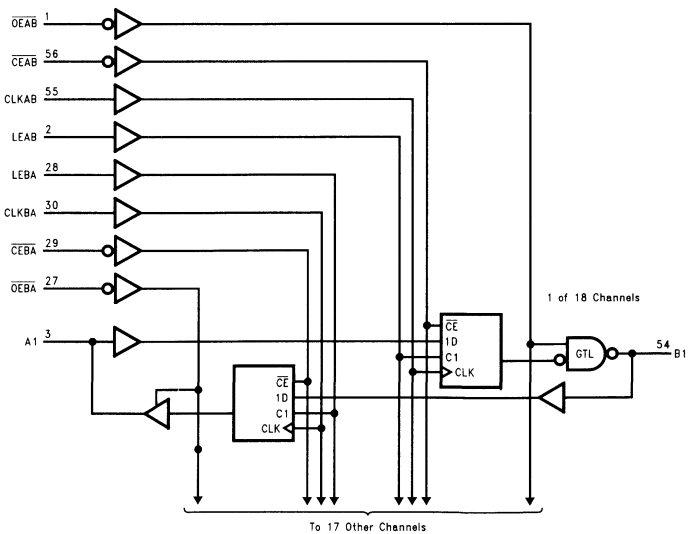
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLE16612 is 100% I/O Spec compatible to conventional GTL.

Features

- Bidirectional interface between GTL and TTL logic levels
- Pin programmable GTL edge rate control (choice of 3 edge rates) selectable even during device operation
- Internal precision receiver threshold voltage reference compensated over process, voltage, and temperature (PVT)
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



TL/F/12468–1

Pin Descriptions

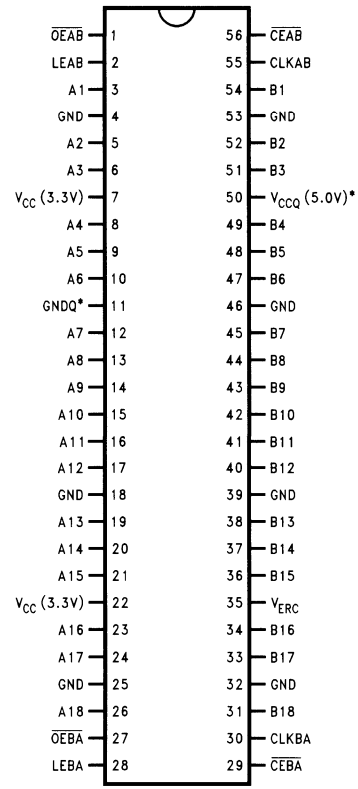
Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{ERC}	GTL Output Edge Rate Control
A1–A18	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B1–B18	B-to-A Data Inputs or A-to-B Open Drain Outputs

GTL Outputs (B Port) Edge Rate Control

V_{ERC} Input	Mode
V_{CC}	Slow
Float	Medium
GND	Fast

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12468–2

Order Number GTLE16612MTD or GTLE16612MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GNDQ are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 2)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(3)	
L	L	L	L	X	B_0(4)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(4)	Clock inhibit

Note 2: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 3: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 4: Output level before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 6)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into A-port I_{OL}	128 mA
DC Output Source Current from A-port I_{OH}	−64 mA
DC Output Sink Current into B-port in the Low State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: V_{CCQ} and GNDQ are the quiet supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide lower noise performance.

Recommended Operating Conditions

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}(7)	4.75V to 5.25V
V_{REF}	0.8V
Bus Termination Voltage (V_{TT})	1.14V to 1.26V
Input Voltage (V_I)	0.0V to 5.5V
On A-Port and Control Pins	
Input High Voltage (V_{IH})	
B-Port	V_{REF} + 50 mV to V_{TT}
Others	2.0V (min)
Input Low Voltage (V_{IL})	
B-Port	0.0V to V_{REF} − 50 mV
Others	0.8V (max)
High Level Output Current (I_{OH})	
A-Port	−32 mA
Low Level Output Current (I_{OL})	
A-Port	+64 mA
B-Port	+40 mA
Operating Temperature	
T_A	−40°C to +85°C

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OH} = −100 μA	V_{CC} − 0.2			V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OH} = −8 mA	2.4			
			I_{OH} = −32 mA	2.0			
V_{OL}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 24 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B-Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 40 mA			0.4	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 0 or 5.5V			±10	μA
	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = 5.5V			20	μA
			V_I = V_{CCQ}			1	
			V_I = 0			−20	
	B-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	μA
			V_I = 0			−5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	μA
$I_{I(hold)}$	A-Port	V_{CC} = 3.15V, V_{CCA} = 4.75V	V_I = 0.8V	75			μA
			V_I = 2.0V	−75			

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted) (Continued)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
I_{OZH}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.0V			1	μA
	B-Port		V_O = 1.2V			10	
I_{OZL}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−1	μA
	B-Port		V_O = 0.4V			−10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		35	45	mA
			Outputs Low		35	45	
			Outputs Disabled		35	45	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		0.2	1	mA
			Outputs Low		0.2	1	
			Outputs Disabled		0.2	1	
ΔI_{CC} (Note 10)	A Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V			1	mA
C_i	Control Pins		V_I = V_{CCQ} or 0		7		pF
C_{io}	A-Port		V_I = V_{CCQ} or 0		10		
C_{io}	B-Port		Per IEEE1194-1991		8		

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 9: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

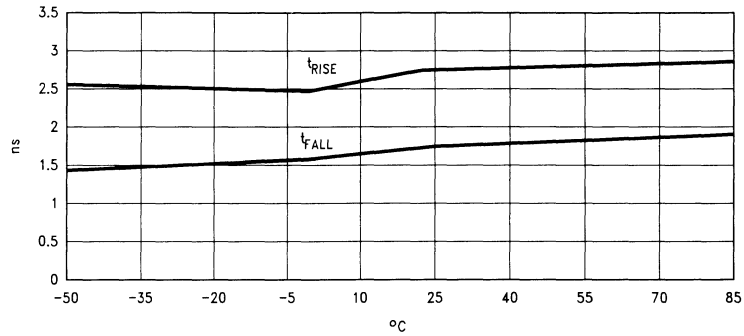
Note 10: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Electrical Characteristics

GTL B-port Output Edge Rate over recommended range of operating free-air temperature, V_{REF} = 0.8V, V_{CCQ} = 4.75V (unless otherwise noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
t_{RISE}	Rise Time	C_L = 5 pF, 0.5V–1.0V	V_{ERC} = 0V		2.5		ns
			V_{ERC} Floating		3.1		
			V_{ERC} = V_{CC}		4.3		
t_{FALL}	Fall Time	C_L = 5 pF, 1.0V–0.5V	V_{ERC} = 0V		1.7		ns
			V_{ERC} Floating		1.9		
			V_{ERC} = V_{CC}		2.8		
Δt_{PLH}	t_{PLH} Adder	C_L = 5 pF	V_{ERC} = 0V			0.0	ns
			V_{ERC} Floating			0.9	
			V_{ERC} = V_{CC}			2.2	
Δt_{PHL}	t_{PHL} Adder	C_L = 5 pF	V_{ERC} = 0			0.0	ns
			V_{ERC} Floating			0.3	
			V_{ERC} = V_{CC}			1.1	

Typical Slew Rate Versus Temperature



TL/F/12468–3

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted)

Symbol			Min	Max	Units
f_{clock}	Max Clock Frequency		0	100	MHz
t_{width}	Pulse Duration	LEAB or LEBA High	3.3		ns
		CLKAB or CLKBA High or Low	4.8		
t_{SU}	Setup Time	A before CLKAB ↑	0.5		ns
		B before CLKBA ↑	2.5		
		A before LEAB ↓	0.5		
		B before LEBA ↓	2.1		
		$\overline{CEAB}$ before CLKAB ↑	1.0		
		$\overline{CEBA}$ before CLKBA ↑	1.0		
t_{Hold}	Hold Time	A after CLKAB ↑	2.7		ns
		B after CLKBA ↑	0.4		
		A after LEAB ↓	3.4		
		B after LEBA ↓	3.3		
		$\overline{CEAB}$ after CLKAB ↑	1.5		
		$\overline{CEBA}$ after CLKBA ↑	0.4		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted). C_L = 5 pF for B-Port and C_L = 50 pF for A-Port.

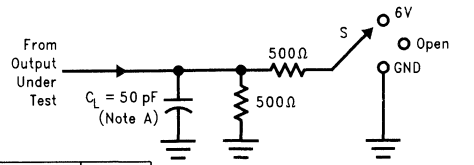
Symbol	From (Input)	To (Output)	Min	Typ (Note 11)	Max	Units
f_{MAX}			100			MHz
t_{PLH}	A	B	1.0		6.2	ns
t_{PHL}			1.0		5.0	
t_{PLH}	LEAB	B	1.2		7.2	ns
t_{PHL}			1.2		7.0	
t_{PLH}	CLKAB	B	1.0		6.6	ns
t_{PHL}			1.0		5.9	
t_{PLH}	$\overline{OEAB}$	B	1.2		6.0	ns
t_{PHL}			1.2		5.5	
t_{PLH}	B	A	2.3		7.2	ns
t_{PHL}			2.0		6.4	
t_{PLH}	LEBA	A	1.8		7.0	ns
t_{PHL}			1.7		6.7	
t_{PLH}	CLKBA	A	1.8		6.7	ns
t_{PHL}			1.5		5.6	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	2.2		5.5	ns
t_{PHZ}, t_{PLZ}			2.0		6.8	
t_{OSHLA}, t_{OSLHA}	A Port: Output to Output Skew (Note 11)				1.0	ns
t_{OSHLB}, t_{OSLHB}	B Port: Output to Output Skew (Note 11)				1.0	

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5V, and T_A = 25°C.

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameters guaranteed by design.

Test Circuits and Timing Waveforms

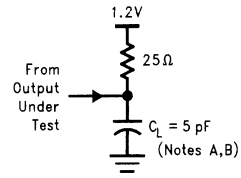
Test Circuit for A Outputs



TL/F/12468-4

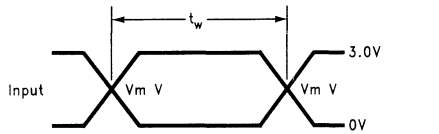
Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Test Circuit for B Outputs



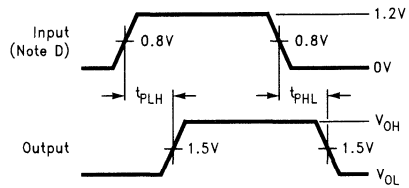
TL/F/12468-5

Voltage Waveforms Pulse Duration
(Vm = 1.5V for A Port and 0.8V for B Port)



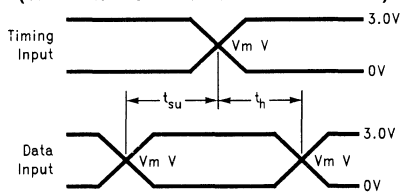
TL/F/12468-6

Voltage Waveforms Propagation Delay Times
(B Port to A Port)



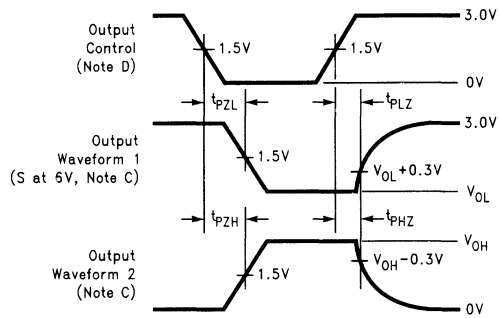
TL/F/12468-7

Voltage Waveforms Setup and Hold Times
(Vm = 1.5V for A Port and 0.8V for B Port)



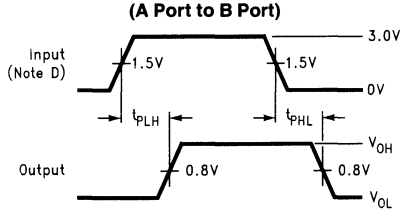
TL/F/12468-8

Voltage Waveforms Enable and Disable Times
(A Port)



TL/F/12468-9

Voltage Waveforms Propagation Delay Times
(A Port to B Port)



TL/F/12468-10

Note A: C_L includes probes and jig capacitance.

Note B: For B port outputs, C_L = 5 pF is used for worst case edge rate.

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note D: All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

National Semiconductor

ADVANCE INFORMATION

GTLPE16612
CMOS 18-Bit GTLP/TTL Universal Bus Transceiver with Output Edge Rate Control

General Description

The GTLPE16612 is one in a series of transceivers designed specifically for GTLP logic levels. The device is a CMOS GTLP 18-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

The pin programmable GTLP "E" edge rate control feature allows the system designer to minimize noise and maximize speed of the system. The V_{ERC} pin (pin 35) is used for this purpose and provides three different edge rates depending on the V_{ERC} pin voltage (high, low, or floating). Voltage changes at the V_{ERC} pin will be reflected at the output within about 100 ns allowing the edge rate to be controlled during system operation.

The device provides TTL to GTLP translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTLP levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

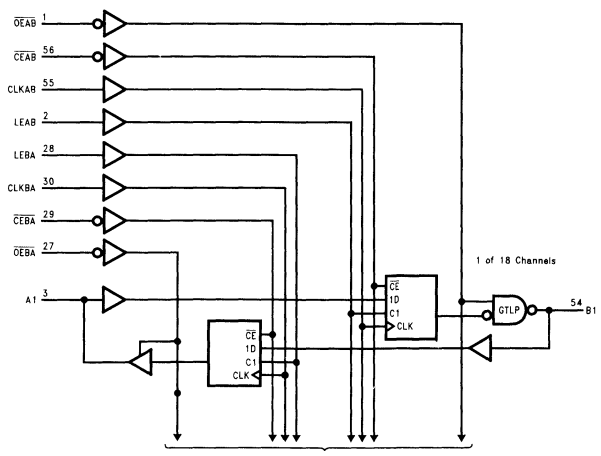
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLPE16612 is 100% I/O Spec compatible to enhanced GTLP where the driver output low voltage is typically 0.5V, the output high 1.5V, and the receiver threshold 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Pin programmable GTLP edge rate control (choice of 3 edge rates) selectable even during device operation
- Internal precision receiver threshold voltage reference compensated over process, voltage, and temperature (PVT)
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



TL/F/12469–1

Pin Descriptions

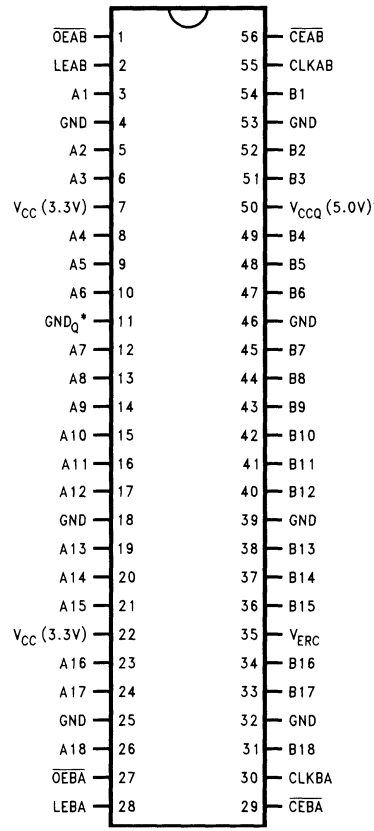
Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{ERC}	GTL Output Edge Rate Control
A1–A18	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B1–B18	B-to-A Data Inputs or A-to-B Open Drain Outputs

GTL Outputs (B Port) Edge Rate Control

V_{ERC} Input	Mode
V_{CC}	Slow
Float	Medium
GND	Fast

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12469–2

Order Number GTLPE16612MTD or GTLPE16612MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GND_Q are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GND_Q/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 2)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(3)	
L	L	L	L	X	B_0(4)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(4)	Clock inhibit

Note 2: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 3: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 4: Output level before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 6)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into A-port I_{OL}	128 mA
DC Output Source Current from A-port I_{OH}	−64 mA
DC Output Sink Current into B-port in the Low State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: V_{CCQ} and GNDQ are the quiet supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide lower noise performance.

Recommended Operating Conditions

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}(7)	4.75V to 5.25V
V_{REF}	1.0V
Bus Termination Voltage (V_{TT})	1.35V to 1.65V
Input Voltage (V_I)	
on A-Port and Control Pins	0.0V to 5.5V
Input High Voltage (V_{IH})	
B-Port	V_{REF} + 200 mV to V_{TT}
Others	2.0V (min)
Input Low Voltage (V_{IL})	
B-Port	0.0V to V_{REF} − 200 mV
Others	0.8V (max)
High Level Output Current (I_{OH})	
A-Port	−32 mA
Low Level Output Current (I_{OL})	
A-Port	+64 mA
B-Port	+40 mA
Operating Temperature	
T_A	−40°C to +85°C

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OH} = −100 μA	V_{CC} − 0.2			V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OH} = −8 mA	2.4			
			I_{OH} = −32 mA	2.0			
V_{OL}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 9)	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_{OL} = 24 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B-Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 40 mA			0.55	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 5.5V or 0V			±10	μA
	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = 5.5V			20	μA
			V_I = V_{CC}			1	
			V_I = 0			−20	
	B-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	μA
			V_I = 0			−5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	μA
$I_{I(hold)}$	A-Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	V_I = 0.8V	75			μA
			V_I = 2.0V	−75			

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted) (Continued)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
I_{OZH}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.0V			1	μA
	B-Port		V_O = 1.2V			10	
I_{OZL}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−1	μA
	B-Port		V_O = 0.4V			−10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		35	45	mA
			Outputs Low		35	45	
			Outputs Disabled		35	45	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		0.2	1	mA
			Outputs Low		0.2	1	
			Outputs Disabled		0.2	1	
ΔI_{CC} (Note 10)	A-Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V			1	mA
C_i	Control Pins		V_I = V_{CCQ} or 0		7		pF
C_{io}	A-Port		V_I = V_{CCQ} or 0		10		
C_{io}	B-Port		Per IEEE 1194–1991		8		

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 9: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

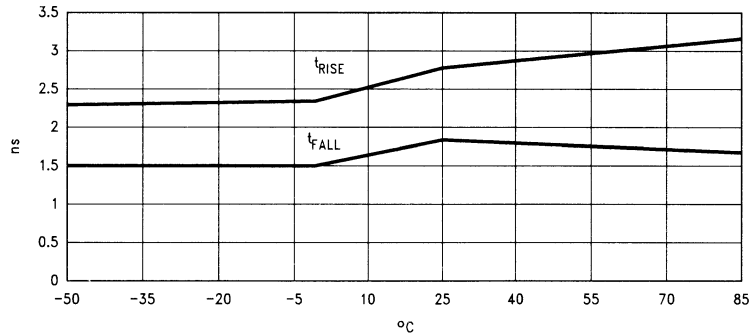
Note 10: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Electrical Characteristics

GTL B-port Output Edge Rate over recommended range of operating free-air temperature, V_{REF} = 1.0V, V_{CCQ} = 4.75V (unless otherwise noted)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
t_{RISE}	Rise Time	C_L = 5 pF, 20%–80%	V_{ERC} = 0V		2.5		ns
			V_{ERC} Floating		3.1		
			V_{ERC} = V_{CC}		4.2		
t_{FALL}	Fall Time	C_L = 5 pF, 80%–20%	V_{ERC} = 0V		1.5		ns
			V_{ERC} Floating		1.6		
			V_{ERC} = V_{CC}		2.4		
Δt_{PLH}	t_{PLH} Adder	C_L = 5 pF	V_{ERC} = 0V			0.0	ns
			V_{ERC} Floating			0.7	
			V_{ERC} = V_{CC}			1.8	
Δt_{PHL}	t_{PHL} Adder	C_L = 5 pF	V_{ERC} = 0V			0.0	ns
			V_{ERC} Floating			0.2	
			V_{ERC} = V_{CC}			1.1	

Typical Slew Rate Versus Temperature



TL/F/12469–3

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted)

Symbol			Min	Max	Units
f_{clock}	Max Clock Frequency		0	100	MHz
t_{width}	Pulse Duration	LEAB or LEBA High	3.3		ns
		CLKAB or CLKBA High or Low	4.8		
t_{SU}	Setup Time	A before CLKAB ↑	0.5		ns
		B before CLKBA ↑	2.5		
		A before LEAB ↓	0.5		
		B before LEBA ↓	2.1		
		$\overline{CEAB}$ before CLKAB ↑	1.0		
		$\overline{CEBA}$ before CLKBA ↑	1.0		
t_{Hold}	Hold Time	A after CLKAB ↑	2.7		ns
		B after CLKBA ↑	0.4		
		A after LEAB ↓	3.4		
		B after LEBA ↓	3.3		
		$\overline{CEAB}$ after CLKAB ↑	1.5		
		$\overline{CEBA}$ after CLKBA ↑	0.4		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted). C_L = 5 pF for B-Port and C_L = 50 pF for A-Port.

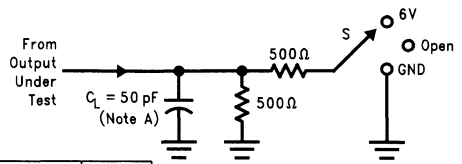
Symbol	From (Input)	To (Output)	Min	Typ (Note 8)	Max	Units
f_{MAX}			100			MHz
t_{PLH}	A	B	1.0		6.2	ns
t_{PHL}			1.0		5.0	
t_{PLH}	LEAB	B	1.2		7.2	ns
t_{PHL}			1.2		7.0	
t_{PLH}	CLKAB	B	1.0		6.6	ns
t_{PHL}			1.0		5.9	
t_{PLH}	$\overline{OEAB}$	B	1.2		6.0	ns
t_{PHL}			1.2		5.5	
t_{PLH}	B	A	2.3		7.2	ns
t_{PHL}			2.0		6.4	
t_{PLH}	LEBA	A	1.8		7.0	ns
t_{PHL}			1.7		6.7	
t_{PLH}	CLKBA	A	1.8		6.7	ns
t_{PHL}			1.5		5.6	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	2.2		5.5	ns
t_{PHZ}, t_{PLZ}			2.0		6.8	
t_{OSHLA}, t_{OSLHA}	A Port: Output to Output Skew (Note 11)				1.0	ns
t_{OSHLB}, t_{OSLHB}	B Port: Output to Output Skew (Note 11)				1.0	

Note 8: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameters guaranteed by design.

Test Circuits and Timing Waveforms

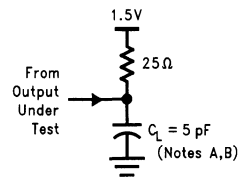
Test Circuit for A Outputs



TL/F/12469-4

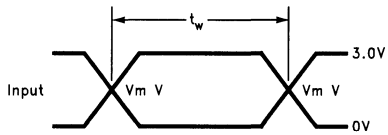
Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Test Circuit for B Outputs



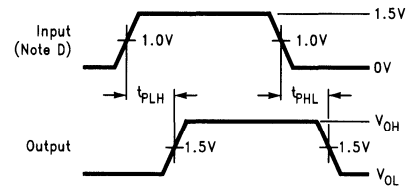
TL/F/12469-5

Voltage Waveforms Pulse Duration
(Vm = 1.5V for A Port and 1.0V for B Port)



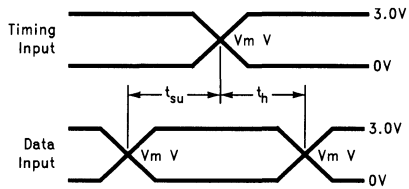
TL/F/12469-6

Voltage Waveforms Propagation Delay Times
(B Port to A Port)



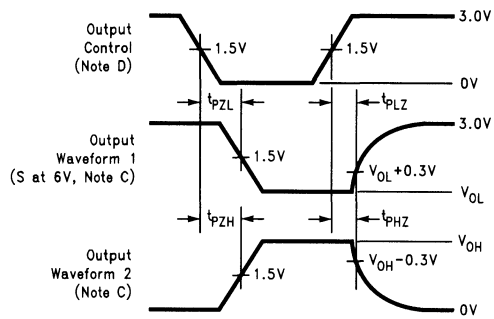
TL/F/12469-7

Voltage Waveforms Setup and Hold Times
(Vm = 1.5V for A Port and 1.0V for B Port)



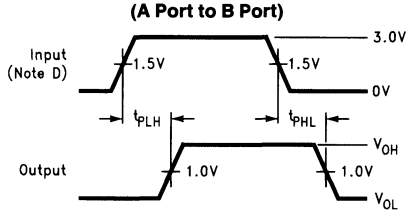
TL/F/12469-8

Voltage Waveforms Enable and Disable Times
(A Port)



TL/F/12469-9

Voltage Waveforms Propagation Delay Times
(A Port to B Port)



TL/F/12469-10

Note A: C_L includes probes and jig capacitance.

Note B: For B port outputs, C_L = 5 pF is used for worst case edge rate.

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note D: All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

National Semiconductor

ADVANCE INFORMATION

GTL16616
CMOS 17-Bit GTL/TTL Universal Bus Transceiver with Clock Buffer

General Description

The GTL16616 is one in a series of transceivers designed specifically for GTL logic levels. The device is a CMOS GTL 17-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode. The 18th bit is used as a unidirectional clock buffer.

National's GTL has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. Its function is similar to BTL or conventional GTL but with different driver output levels and receiver threshold.

The device provides TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

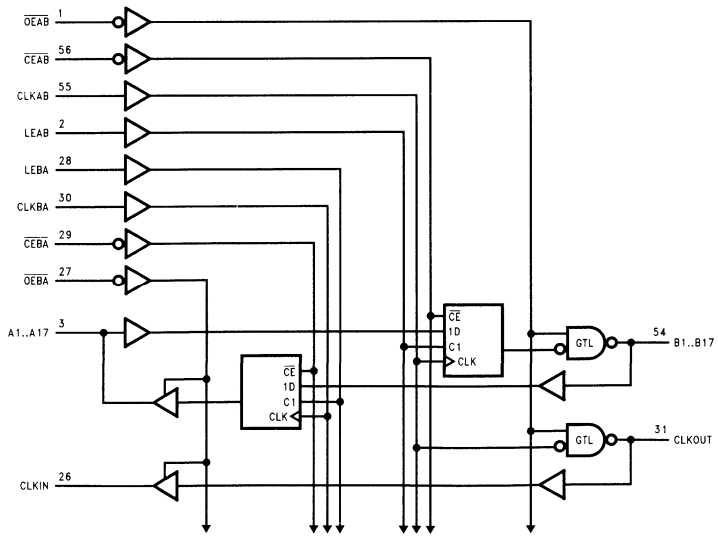
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTL16616 is 100% I/O Spec compatible to conventional GTL.

Features

- Bidirectional interface between GTL and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- V_{REF} pin provides external supply reference voltage for receiver threshold
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

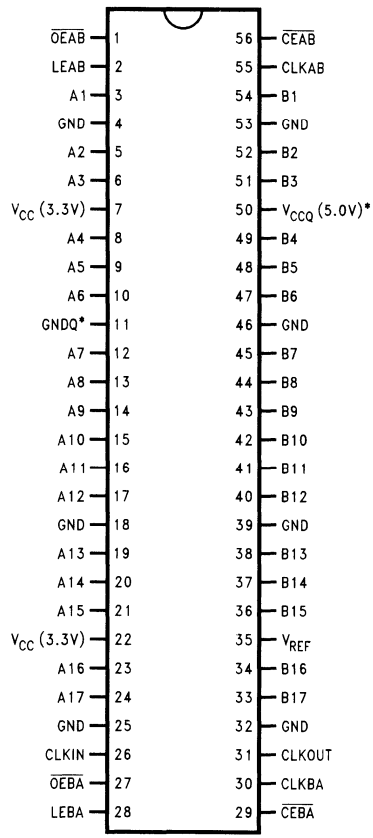
Logic Diagram



TL/F/12536–1

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12536–2

Order Number GTL16616MTD or GTL16616MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GNDQ are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 1)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(2)	
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established.

National Semiconductor

ADVANCE INFORMATION

GTLP16616
CMOS 17-Bit GTLP/TTL Universal Bus Transceiver with Clock Buffer

General Description

The GTLP16616 is one in a series of transceivers designed specifically for GTLP logic levels. The device is a CMOS GTLP 17-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode. The 18th bit is used as a undirectional clock buffer.

National's GTLP has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. Its function is similar to BTL or conventional GTLP but with different driver output levels and receiver threshold.

The device provides TTL to GTLP translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTLP levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

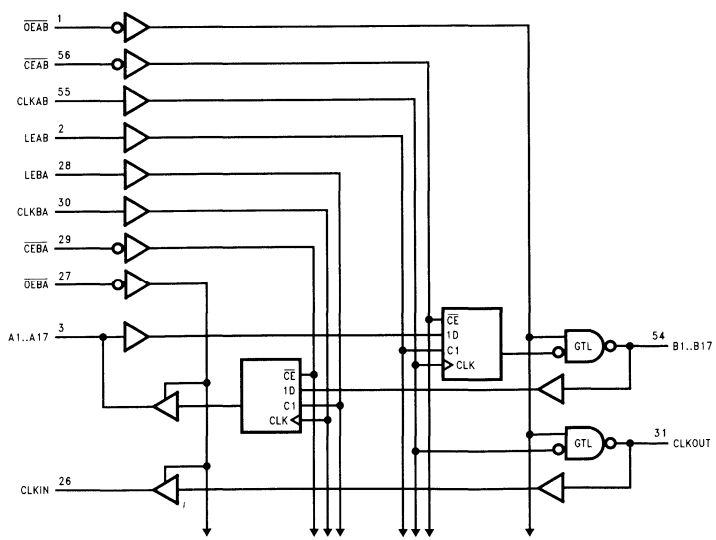
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLP16616 is 100% I/O Spec compatible to enhanced GTLP where the driver output low voltage is typically 0.5V, the output high 1.5V, and the receiver threshold 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- V_{REF} pin provides external supply reference voltage for receiver threshold
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



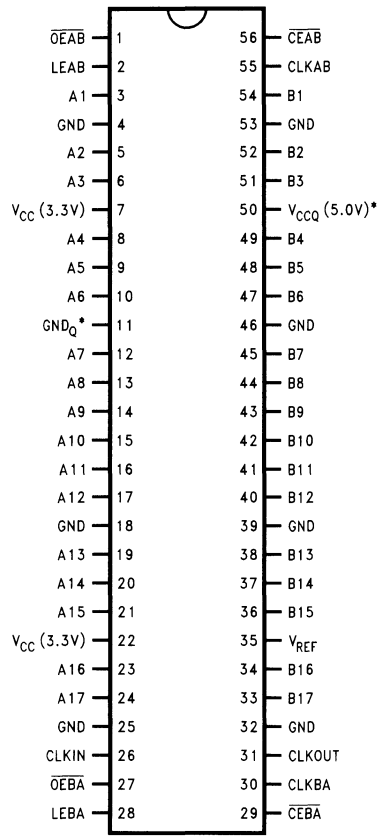
TL/F/12537–1

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{ERC}	GTL Output Edge Rate Control
A1–A17	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B1–B17	B-to-A Data Inputs or A-to-B Open Drain Outputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12537–2

Order Number GTLP16616MTD or GTLP16616MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GND_Q are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GND_Q/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 1)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(2)	
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established.

National Semiconductor

ADVANCE INFORMATION

GTLE16616
CMOS 17-Bit GTLE/TTL Universal Bus Transceiver with Clock Buffer and Output Edge Rate Control

General Description

The GTLE16616 is one in a series of transceivers designed specifically for GTL logic levels. The device is a CMOS GTL 17-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode. The 18th bit is used as a unidirectional clock buffer.

The pin programmable GTL "E" edge rate control feature allows the system designer to minimize noise and maximize speed of the system. The V_{ERC} pin (pin 35) is used for this purpose and provides three different edge rates depending on the V_{ERC} pin voltage (high, low, or floating). Voltage changes at the V_{ERC} pin will be reflected at the output within about 100 ns allowing the edge rate to be controlled during system operation.

The device provides TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

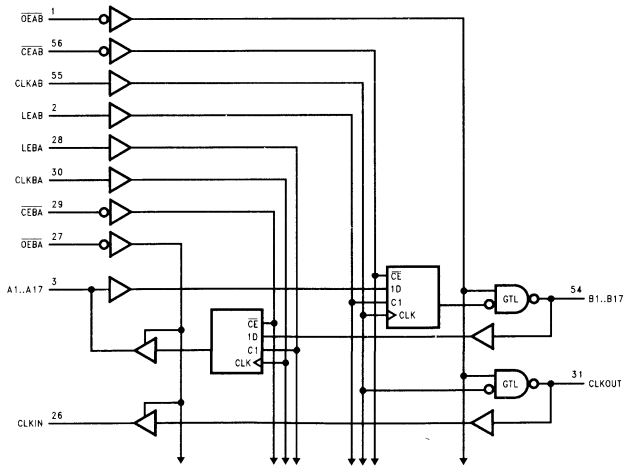
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLE16616 is 100% I/O Spec compatible to conventional GTL.

Features

- Bidirectional interface between GTL and TTL logic levels
- Pin programmable GTL edge rate control (choice of 3 edge rates) selectable even during device operation
- Internal precision receiver threshold voltage reference compensated over process, voltage, and temperature (PVT)
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



TL/F/12538–1

Pin Descriptions

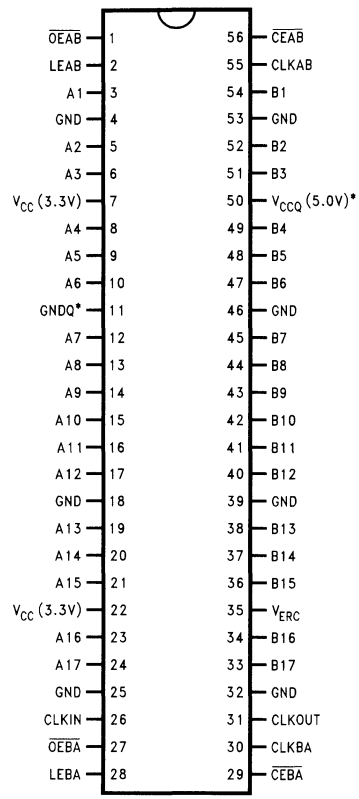
Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{ERC}	GTL Output Edge Rate Control
A1–A17	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B1–B17	B-to-A Data Inputs or A-to-B Open Drain Outputs

GTL Outputs (B Port) Edge Rate Control

V_{ERC} Input	Mode
V_{CC}	Slow
Float	Medium
GND	Fast

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12538–2

Order Number GTLE16616MTD or GTLE16616MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GNDQ are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 1)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(2)	
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established.

National Semiconductor

ADVANCE INFORMATION

GTLPE16616
CMOS 17-Bit GTLP/TTL Universal Bus Transceiver with Clock Buffer and Output Edge Rate Control

General Description

The GTLPE16616 is one in a series of transceivers designed specifically for GTLP logic levels. The device is a CMOS GTLP 17-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode. The 18th bit is used as a unidirectional clock buffer.

The pin programmable GTLP "E" edge rate control feature allows the system designer to minimize noise and maximize speed of the system. The V_{ERC} pin (pin 35) is used for this purpose and provides three different edge rates depending on the V_{ERC} pin voltage (high, low, or floating). Voltage changes at the V_{ERC} pin will be reflected at the output within about 100 ns allowing the edge rate to be controlled during system operation.

The device provides TTL to GTLP translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTLP levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

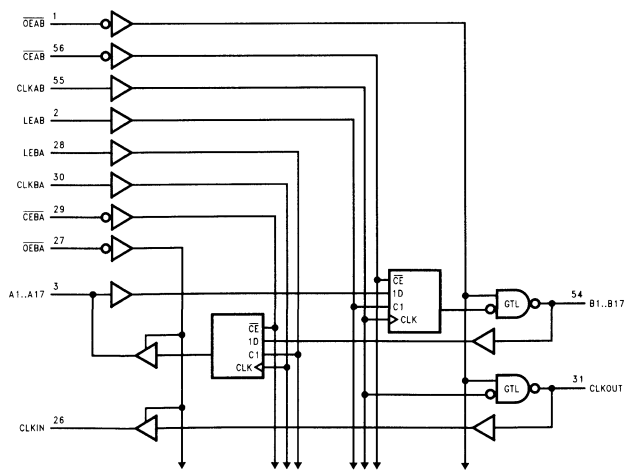
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTLPE16616 is 100% I/O Spec compatible to enhanced GTLP where the driver output low voltage is typically 0.5V, the output high 1.5V, and the receiver threshold 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Pin programmable GTLP edge rate control (choice of 3 edge rates) selectable even during device operation
- Internal precision receiver threshold voltage reference compensated over process, voltage, and temperature (PVT)
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



TL/F/12539–1

Pin Descriptions

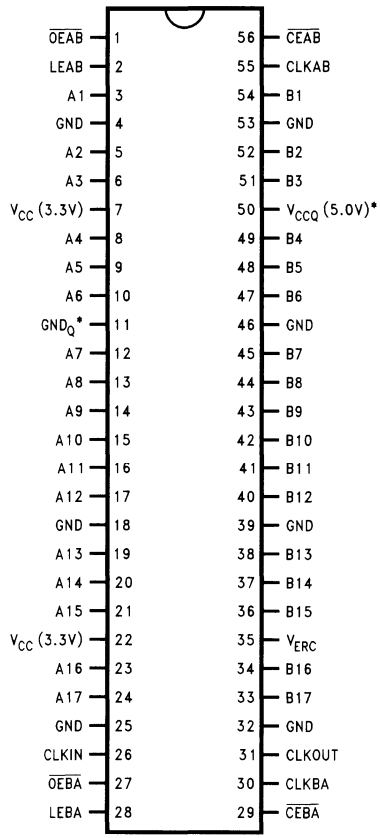
Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Active HIGH)
LEBA	B-to-A Latch Enable (Active HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{ERC}	GTL Output Edge Rate Control
A1–A17	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B1–B17	B-to-A Data Inputs or A-to-B Open Drain Outputs

GTL Outputs (B Port) Edge Rate Control

V_{ERC} Input	Mode
V_{CC}	Slow
Float	Medium
GND	Fast

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12539–2

Order Number GTLPE16616MTD or GTLPE16616MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GND_Q are the analog supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GND_Q/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide better bus performance.

Truth Table (Note 1)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(2)	
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similiar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established.

National Semiconductor

ADVANCE INFORMATION

GTLE412/GTLPE412 CMOS 4-Bit GTL/TTL Universal Backplane Transceivers with Programmable Output Edge Rate Control and Live Insertion Pin

General Description

The GTLE412/GTLPE412 are a series of transceivers designed specifically for GTL and GTLP logic levels. The devices are CMOS GTL 4-Bit registered bus transceivers which combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

The pin programmable output edge rate control feature allows the system designer to minimize noise and maximize speed of the system. The V_{ERC} pin is used for this purpose and provides three different edge rates depending on the V_{ERC} pin voltage (high, low, or floating). Voltage changes at the V_{ERC} pin will be reflected at the output within about 100 ns allowing the edge rate to be controlled during system operation.

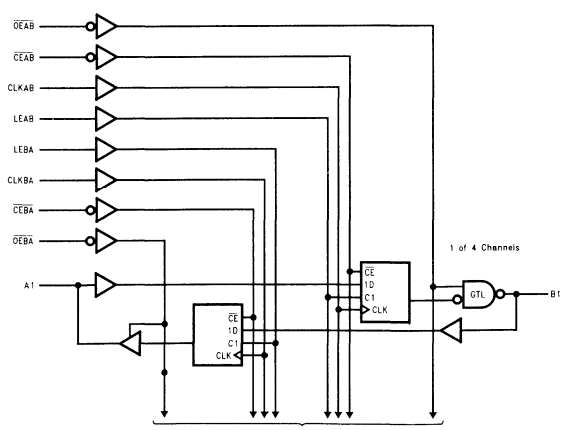
The devices provide TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL or GTLP levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit. In addition, the live insertion pin precharges GTL (B-Port) outputs.

Features

- Increased 60 mA GTL output drive for driving larger backplanes
- Live insertion pin precharges outputs for glitch-free live insertion
- Bidirectional interface between GTL and TTL logic levels
- Pin programmable GTL edge rate control (choice of 3 edge rates) selectable even during device operation
- Internal precision receiver threshold voltage reference compensated over process, voltage, and temperature (PVT)
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SOIC, TSSOP, and SSOPII

Logic Diagram



TL/F/12659–1

National Semiconductor

ADVANCE INFORMATION

GTL245, GTLP245
CMOS 8-Bit GTL/TTL Translating Transceivers

General Description

A series of transceivers designed specifically for GTL and GTLP logic levels. These octal devices provide TTL/GTL(P) translation while providing '245 standard logic functionality.

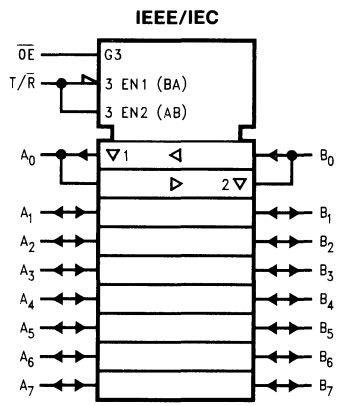
National's GTL has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. This technology assures consistent low noise performance.

Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

Features

- Interface between GTL and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- Standard logic '245 function
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SOIC and TSSOP

Logic Symbol



TL/F/12660–2

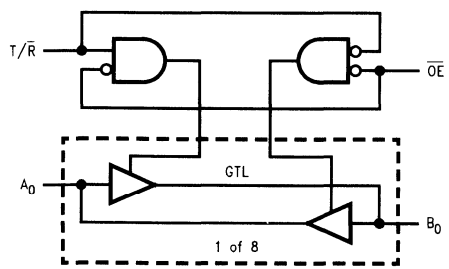
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE® Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12660–3

Section 12

Ordering Information and Physical Dimensions

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Package Offering

Available and Planned Package Offering

For most current packaging information, contact your National Semiconductor representatives.

Type	Lead	LCX	LVX	LVQ	LVT	ALCX	GTL
00	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
02	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
04	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
05	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™					
08	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
10	14	SOIC JEDEC & EIAJ, TSSOP					
11	14	SOIC JEDEC & EIAJ, TSSOP					
14	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
32	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
38	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™					
74	14	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
86	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
109	14	SOIC JEDEC & EIAJ, TSSOP					
112	14	SOIC JEDEC & EIAJ, TSSOP					
125	14*	SOIC JEDEC & EIAJ, TSSOP, TinyPak™	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, TSSOP		
126	14*	TinyPak™					
138	16	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
151	16			SOIC JEDEC & EIAJ			
157	16	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
174	16		SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ			
240	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
241	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP		SOIC JEDEC & EIAJ, QSOP			
244	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
2244	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP					
245	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
2245	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP					
257	16	SOIC JEDEC & EIAJ, TSSOP					
273	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP			
373	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
374	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
540	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP					
541	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP					
543	24	SOIC JEDEC, SSOP II, TSSOP			SOIC JEDEC & EIAJ, SSOP II, TSSOP		
573	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP II, TSSOP		
574	20	SOIC JEDEC & EIAJ, SSOP II, TSSOP			SOIC JEDEC & EIAJ, SSOP II, TSSOP		
646	24	SOIC JEDEC, SSOP II, TSSOP			SOIC JEDEC, TSSOP		
652	24	SOIC JEDEC, SSOP II, TSSOP			SOIC JEDEC, TSSOP		
821	24	SOIC JEDEC, SSOP II, TSSOP					
841	24	SOIC JEDEC, SSOP II, TSSOP					
2952	24				SOIC JEDEC, SSOP II, TSSOP		
3245	24		SOIC JEDEC, QSOP, TSSOP				
4245	24		SOIC JEDEC, QSOP, TSSOP				
C3245	24		SOIC JEDEC, QSOP, TSSOP				
C4245	24		SOIC JEDEC, QSOP, TSSOP				
C164245	48		SSOP, TSSOP				
3L383	24		SOIC JEDEC, QSOP, TSSOP				
3L384	24*		SOIC JEDEC, QSOP, TSSOP, TinyPak™				
3L384A	24		SOIC JEDEC, QSOP, TSSOP				
16212	56		SSOP, TSSOP				

*TinyPak™ = 5-Lead SOT-23.

Available and Planned Package Offering (Continued)

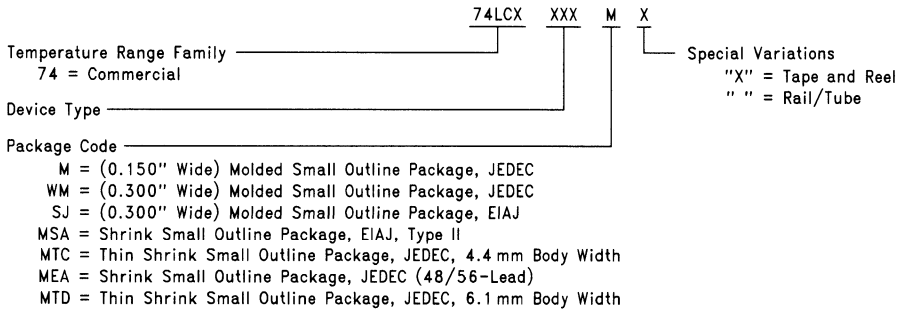
Type	Lead	LCX	LVX	LVQ	LVT	ALCX	GTL
16240	48	SSOP, TSSOP			SSOP, TSSOP	SSOP, TSSOP	
162240	48				SSOP, TSSOP		
16244	48	SSOP, TSSOP			SSOP, TSSOP	SSOP, TSSOP	
162244	48				SSOP, TSSOP	SSOP, TSSOP	
16245	48	SSOP, TSSOP			SSOP, TSSOP	SSOP, TSSOP	
162245	48				SSOP, TSSOP	SSOP, TSSOP	
16373	48	SSOP, TSSOP			SSOP, TSSOP	SSOP, TSSOP	
16374	48	SSOP, TSSOP			SSOP, TSSOP	SSOP, TSSOP	
C164245	48		SSOP, TSSOP				
16500	56	SSOP, TSSOP			SSOP, TSSOP		
16501	56	SSOP, TSSOP					
16543	56	SSOP, TSSOP			SSOP, TSSOP		
16646	56	SSOP, TSSOP			SSOP, TSSOP		
16652	56	SSOP, TSSOP			SSOP, TSSOP		
16841	56	SSOP, TSSOP					
16843	56	SSOP, TSSOP					
16612	56						SSOP, TSSOP
P16612	56						SSOP, TSSOP
E16612	56						SSOP, TSSOP
PE16612	56						SSOP, TSSOP
16616	56						SSOP, TSSOP
P16616	56						SSOP, TSSOP
E16616	56						SSOP, TSSOP
PE16616	56						SSOP, TSSOP

National Semiconductor

Low Voltage Logic Ordering Information

LCX Family Ordering Information

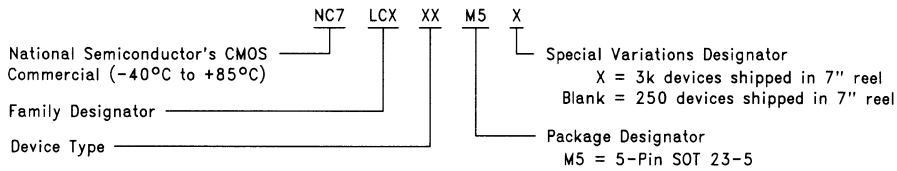
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–5

LCX Single Gate Family Ordering Information

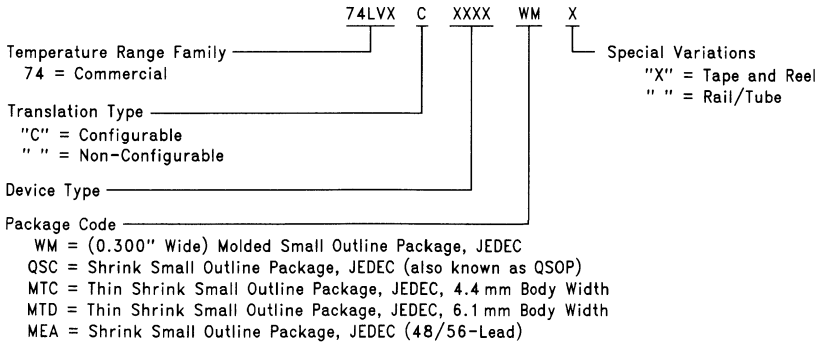
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–32

LVX Translator Family Ordering Information

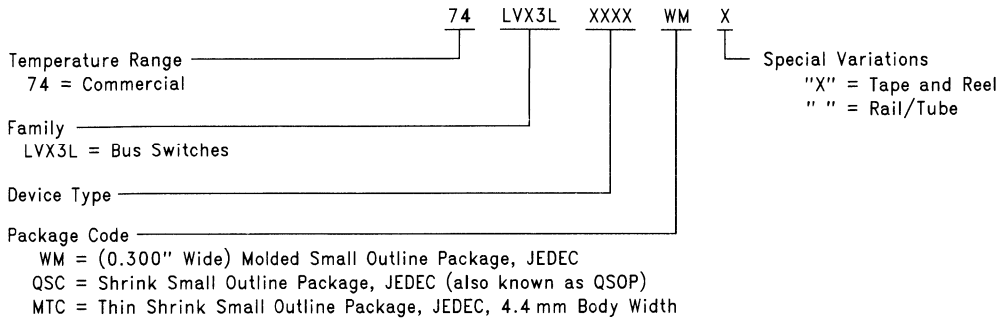
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–3

LVX Bus Switch Family Ordering Information

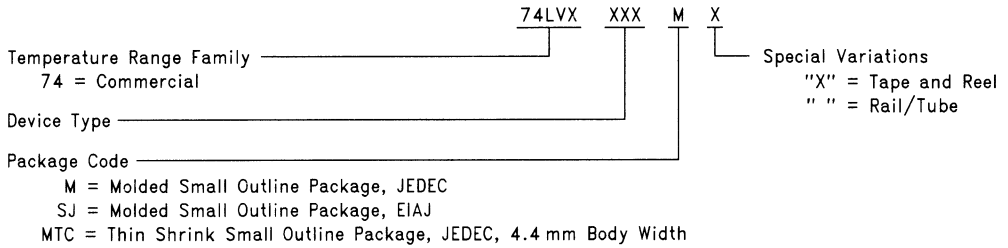
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–4

LVX Family Ordering Information

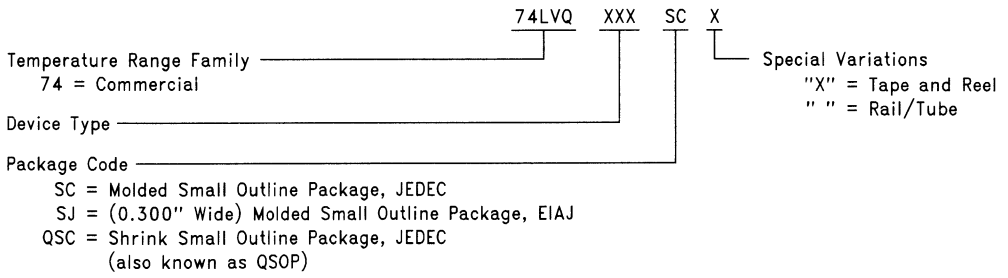
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–2

LVQ Family Ordering Information

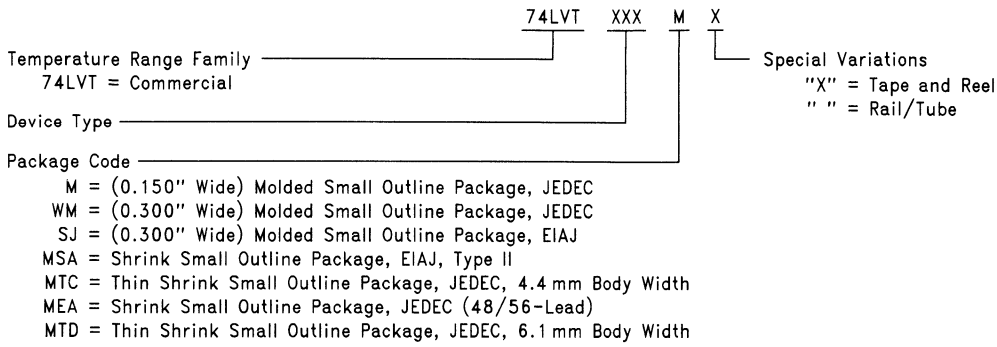
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–1

LVT Family Ordering Information

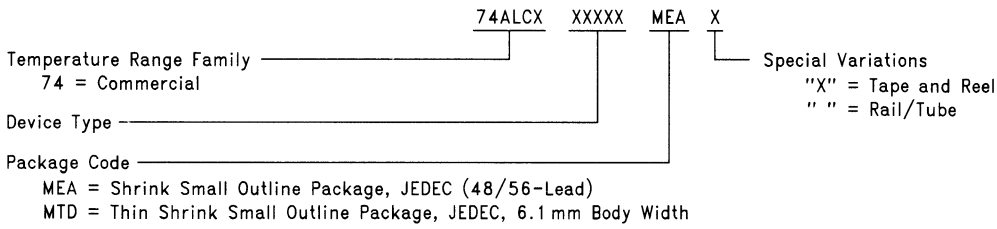
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–6

ALCX Family Ordering Information

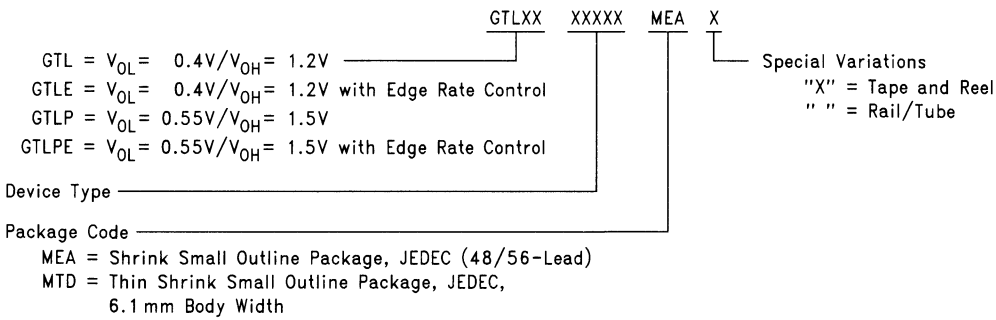
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12540–7

GTL Family Ordering Information

The device number is used to form part of a simplified purchasing code where the device and package types are defined as follows:

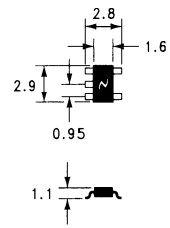


TL/F/12540–8

Package Comparison Summary

Dimensions in millimeters. (To scale but not actual size.)

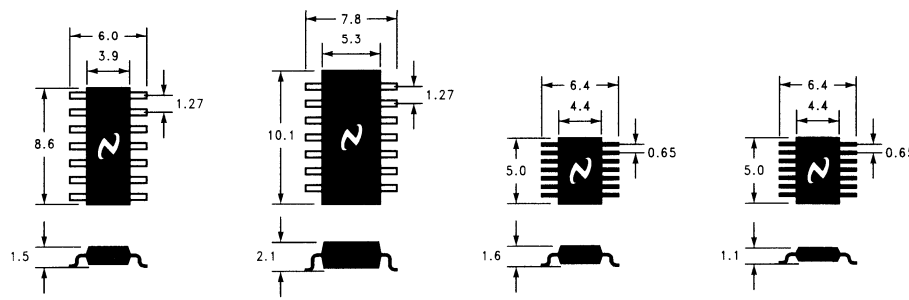
5-Lead Package Options



5-Lead SOT-23
(M5, M5X)
Area = 8.12 sq mm

TL/F/12540-33

14-Lead Package Options



SOIC (JEDEC)
(M, MX)
Area = 52 sq mm

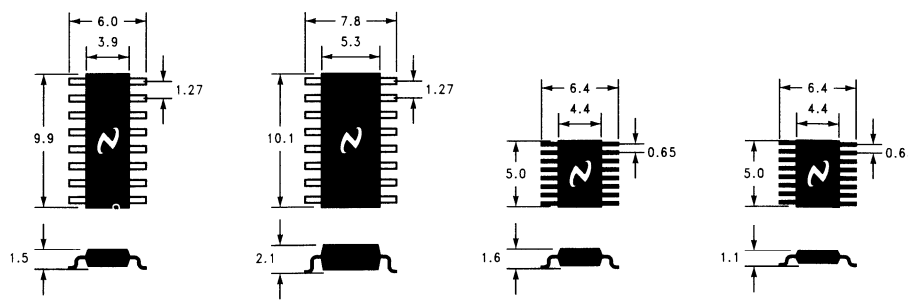
SOP (EIAJ)
(SJ, SJX)
Area = 79 sq mm

SSOPI
(MSCX)
Area = 32 sq mm

TSSOP
(MTC, MTCX)
Area = 32 sq mm

TL/F/12540-10

16-Lead Package Options



SOIC (JEDEC)
(M, MX)
Area = 59 sq mm

SOP (EIAJ)
(SJ, SJX)
Area = 79 sq mm

SSOPI
(MSCX)
Area = 32 sq mm

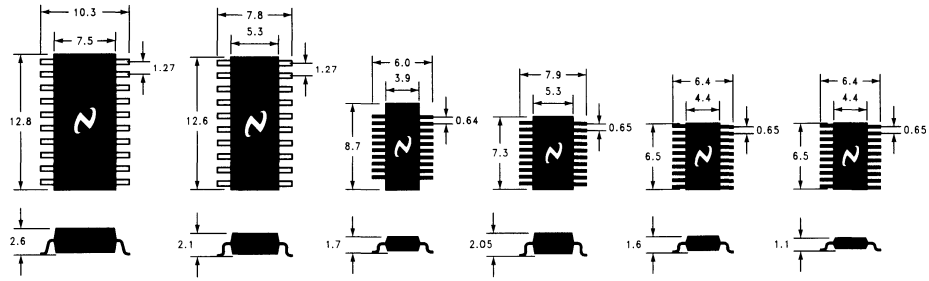
TSSOP
(MTC, MTCX)
Area = 32 sq mm

TL/F/12540-11

Package Comparison Summary (Continued)

Dimensions in millimeters. (To scale but not actual size.) (Continued)

20-Lead Package Options



SOIC (JEDEC) (WM, WMX) Area = 132 sq mm

SOP (EIAJ) (SJ, SJX) Area = 98 sq mm

QSOP (QSC, QSCX) Area = 52 sq mm

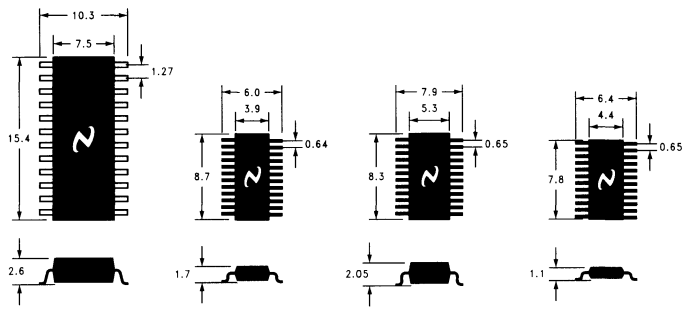
SSOPII (MSA, MSAX) Area = 58 sq mm

SSOPI (MSCX) Area = 42 sq mm

TSSOP (MTC, MTCX) Area = 42 sq mm

TL/F/12540–12

24-Lead Package Options



SOIC (JEDEC) (WM, WMX) Area = 159 sq mm

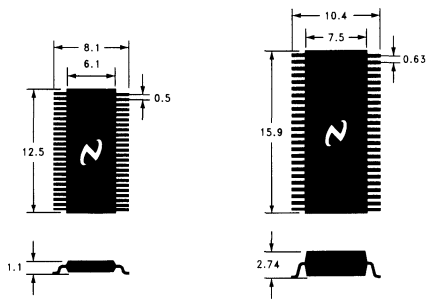
QSOP (QSC, QSCX) Area = 52 sq mm

SSOPII (MSA, MSAX) Area = 66 sq mm

TSSOP (MTC, MTCX) Area = 50 sq mm

TL/F/12540–13

48-Lead Package Options

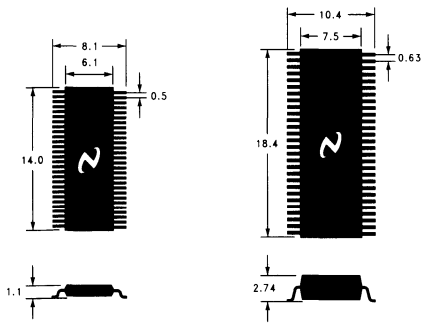


TSSOP (MTD, MTDX) Area = 101 sq mm

SSOP (MEA, MEAX) Area = 165 sq mm

TL/F/12540–14

56-Lead Package Options



TSSOP (MTD, MTDX) Area = 113 sq mm

SSOP (MEA, MEAX) Area = 191 sq mm

TL/F/12540–15

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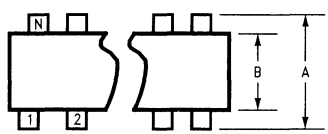
Small Outline Package Comparison

Package (Code)	Dim	14-Pin		16-Pin		20-Pin		24-Pin	
		Min	Max	Min	Max	Min	Max	Min	Max
SOIC JEDEC (M, WM)	A	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65)
	B	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
SOP EIAJ (SJ)	A	0.295 (7.50)	0.319 (8.10)	0.295 (7.62)	0.319 (8.89)	0.295 (7.62)	0.319 (8.89)		
	B	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)		
SSOP EIAJ Type I (MSC)	A	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)		
	B	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)		
SSOP EIAJ Type II (MSA)	A	— —	— —	— —	— —	0.301 (7.65)	0.311 (7.90)	0.301 (7.65)	0.311 (7.90)
	B	— —	— —	— —	— —	0.205 (5.2)	0.212 (5.38)	0.205 (5.2)	0.212 (5.38)
TSSOP (MTC)	A	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)
	B	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)
SSOP JEDEC (aka QSOP) (QSC)	A					0.231 (5.87)	0.241 (6.12)	0.231 (5.87)	0.241 (6.12)
	B					0.151 (3.84)	0.157 (3.99)	0.151 (3.84)	0.157 (3.99)

Units: Inch (mm)



TL/F/12540–9

48/56 Lead Package Comparison					
	Dim	48-Pin		56-Pin	
		Min	Max	Min	Max
SSOP (MEA)	A	0.395 (10.04)	0.420 (10.66)	0.395 (10.04)	0.420 (10.66)
	B	0.291 (7.40)	0.299 (7.59)	0.291 (7.40)	0.299 (7.59)
TSSOP (MTD)	A	0.313 (7.95)	0.325 (8.25)	0.313 (7.95)	0.325 (8.25)
	B	0.236 (6.00)	0.244 (6.20)	0.236 (6.00)	0.244 (6.20)

Package Ordering Code vs National Semiconductor Package Drawing Number

Package Code	Description	National Semiconductor Package Drawing Number						
		5-Lead	14-Lead	16-Lead	20-Lead	24-Lead	48-Lead	56-Lead
M5	5-Lead SOT-23	MA05B						
M	Molded Small Outline Package, JEDEC		M14A	M16A	M20B	M24B		
WM	Molded Small Outline Package, JEDEC				M20B	M24B		
SJ	Molded Small Outline Package, EIAJ		M14D	M16D	M20D			
MSC	Molded Shrink Small Outline Package, EIAJ, Type I		MSC14	MSC16	MSC20			
MSA	Molded Shrink Small Outline Package EIAJ, Type II				MSA20	MSA24		
MTC	Molded Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width		MTC14	MTC16	MTC20	MTC24		
QSC	Molded Shrink Small Outline Package, JEDEC (also known as QSOP)				MQA20	MQA24		
MEA	Molded Shrink Small Outline Package, JEDEC						MS48A	MS56A
MTD	Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width						MTD48	MTD56

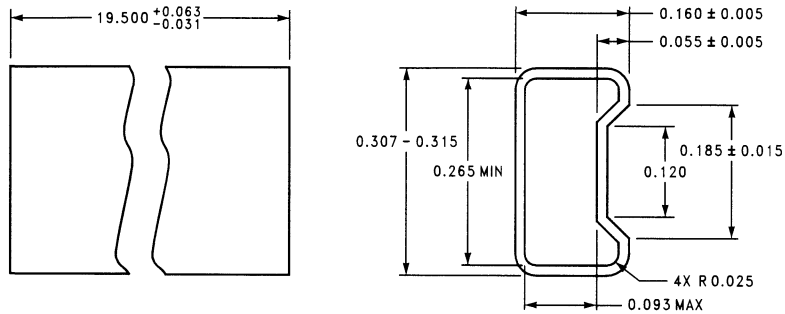
Tube/Tape-and-Reel Quantities

Package Code	Package Description	Package Number	Immediate Container Quantity	
			Tube/Rail	Tape and Reel
M5	5-Lead SOT-23	MA05B	Not Available	250 or 3000
M	Small Outline Package, JEDEC (SOIC)	M14A	55	2500
M		M16A	48	2500
WM		M20B	36	1000
WM		M24B	30	1000
SJ	Small Outline Package, EIAJ (SOP)	M14D	47	2000
SJ		M16D	47	2000
SJ		M20D	38	2000
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	54	2500
QSC		MQA24	54	2500
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	66	2000
MSA		MSA24	58	2000
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOPI)	MSC14	Not Available	2000
MSC		MSC16	Not Available	2000
MSC		MSC20	Not Available	2000
MTC	Thin Shrink Small Outline Package, JEDEC, 4.4mm (TSSOP)	MTC14	94	2500
MTC		MTC16	94	2500
MTC		MTC20	73	2500
MTC		MTC24	61	2500
MEA	Shrink Small Outline Package (SSOP)	MS48A	29	1000
MEA		MS56A	25	1000
MTD	Thin Shrink Small Outline Package, 6.1mm (TSSOP)	MTD48	38	1000
MTD		MTD56	34	1000

Tube Specifications and Drawings

14/16 Lead SOIC, JEDEC and QSOP

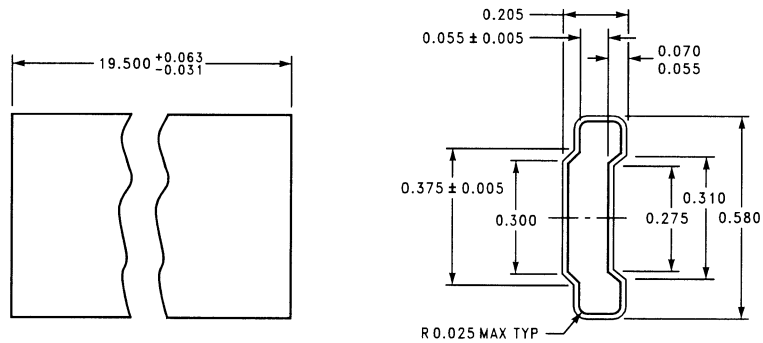
Package Number: M14A, M16A, MQA20, MQA24



TL/F/12540–16

20/24 Lead SOIC, JEDEC

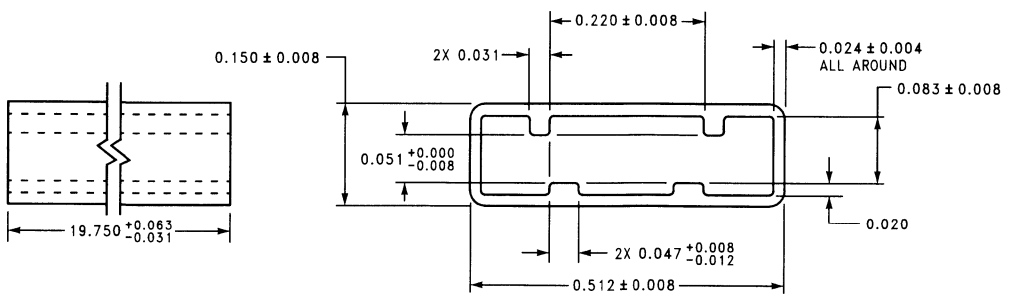
Package Number: M20B, M24B



TL/F/12540–17

SOP, EIAJ and SSOP II, EIAJ

Package Number: M14D, M16D, M20D, MSA20, MSA24



TL/F/12540–18

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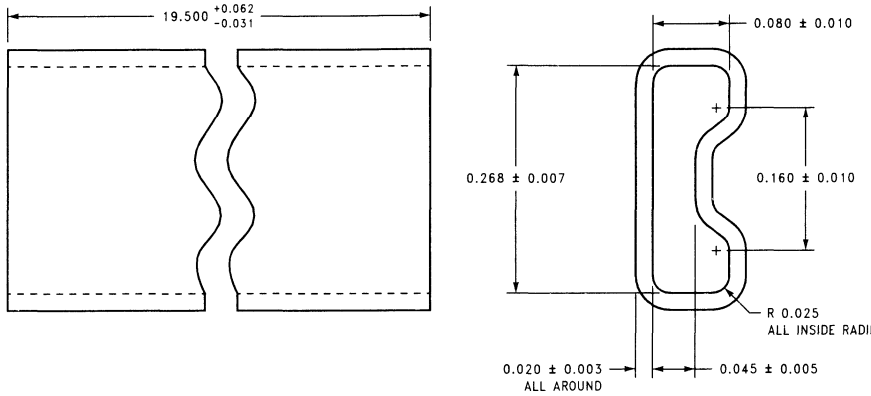
Tube Specifications and Drawings (Continued)

TSSOP, JEDEC, 4.4 mm Body Width

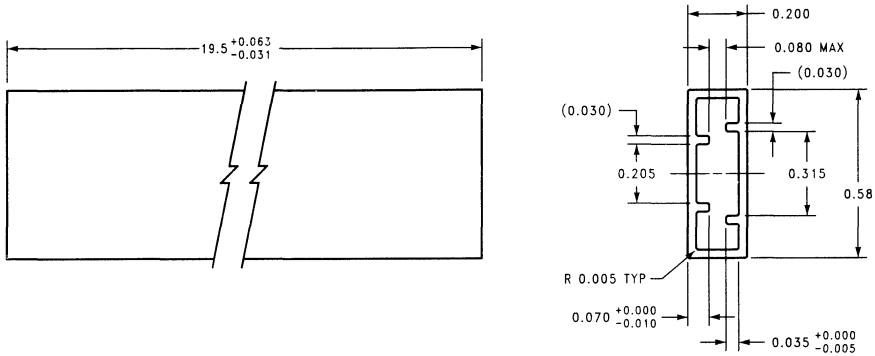
Package Number: MTC14, MTC16, MTC20 and MTC24



TL/F/12540–20

SSOP

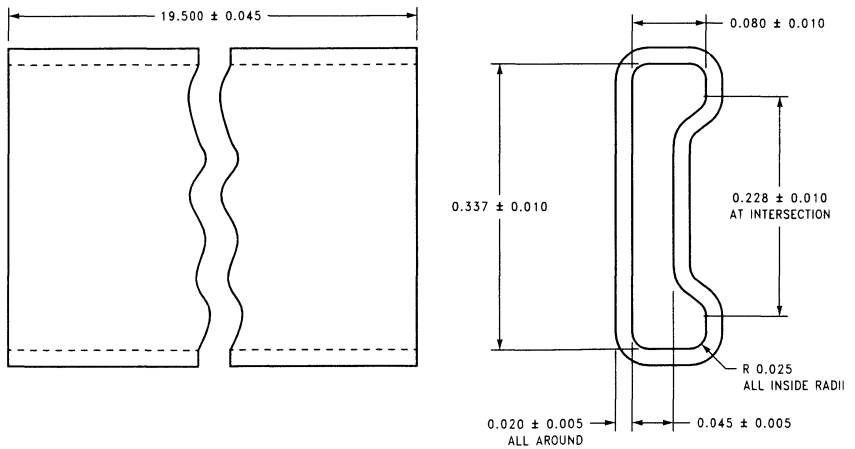
Package Number: MS48A, MS56A



TL/F/12540–21

TSSOP

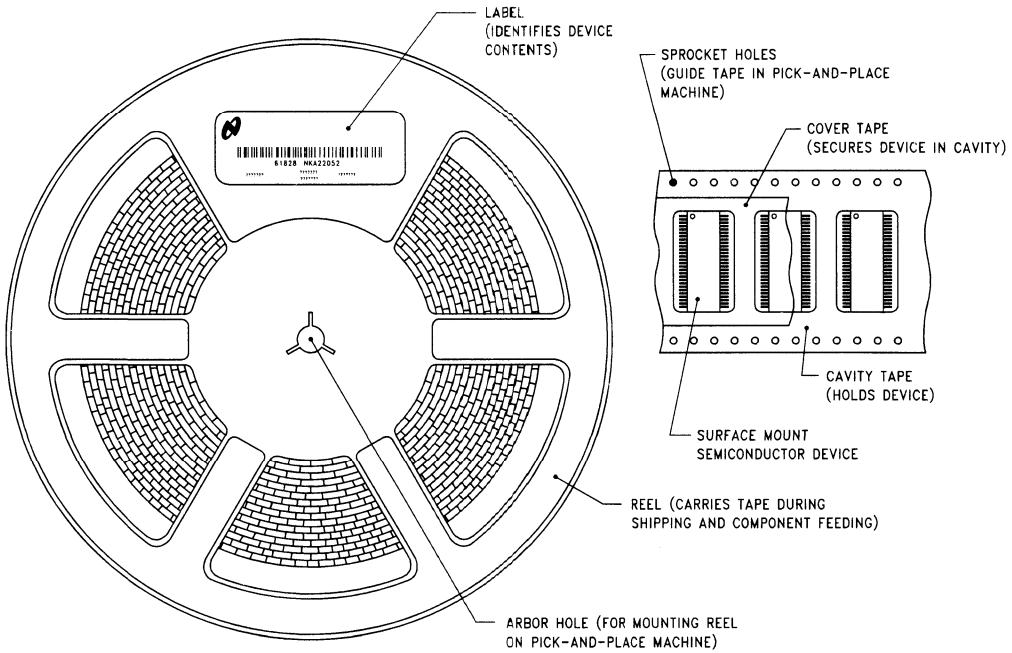
Package Number: MTD48, MTD56



TL/F/12540–22

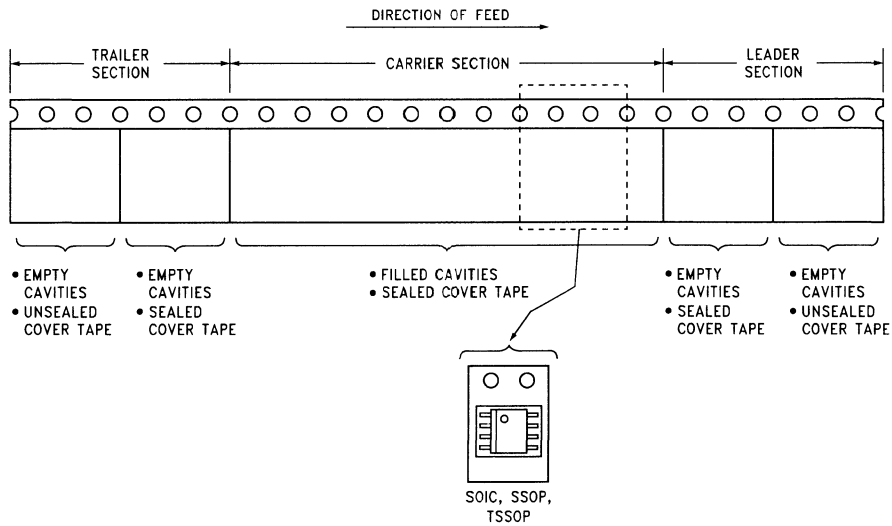
Tape-and-Reel Overview and Technical Information

Tape-and-Reel Diagram



TL/F/12540–23

Tape Format and Device Orientation



TL/F/12540–24

Tape and Reel Overview and Technical Information (Continued)

MATERIALS

- Cavity Tape: Static Dissipative PVC or Polystyrene
- Cover Tape: Static Dissipative Polyester or Polyethylene
- Reel: Static Dissipative PVC or Polystyrene
- Surface Resistivity: 10^5 Ω/□ to less than 10^{12} Ω/□ all materials.

COVER TAPE PEEL STRENGTH

- The force required to peel off the cover tape from the carrier tape will fall within the range of 0.1 Newton to 1.3 Newton (10 grams to 130 grams) at a peeling speed of 300 mm per minute. This complies with the EIA standard.

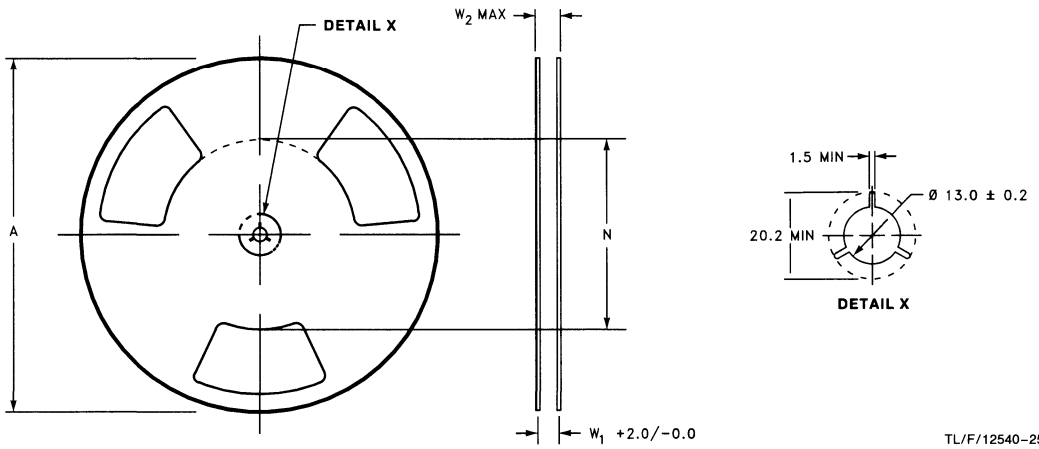
TAPE STORAGE

- It is recommended that the sealed tape be stored in conditions where the environment does not exceed:
  - → Temperature: 40°C maximum
  - → Relative humidity: 90% maximum
  - → No direct exposure to sunlight.

ELECTROSTATIC CHARGES

National Semiconductor uses only static dissipative tape and reel materials (surface resistivity of $10^5\Omega$ to 10^{12} Ω/□) to avoid damaging static charges building up during the peeling off of the cover tape prior to pick and place. National Semiconductor ran extensive evaluations on cover tape materials and found that static charge build up was very low (less than 200V) on static dissipative cover tapes. In comparison, commonly used insulative cover tapes had readings consistently in excess of 3000V.

Reel Specifications and Drawings (All dimensions in millimeters)



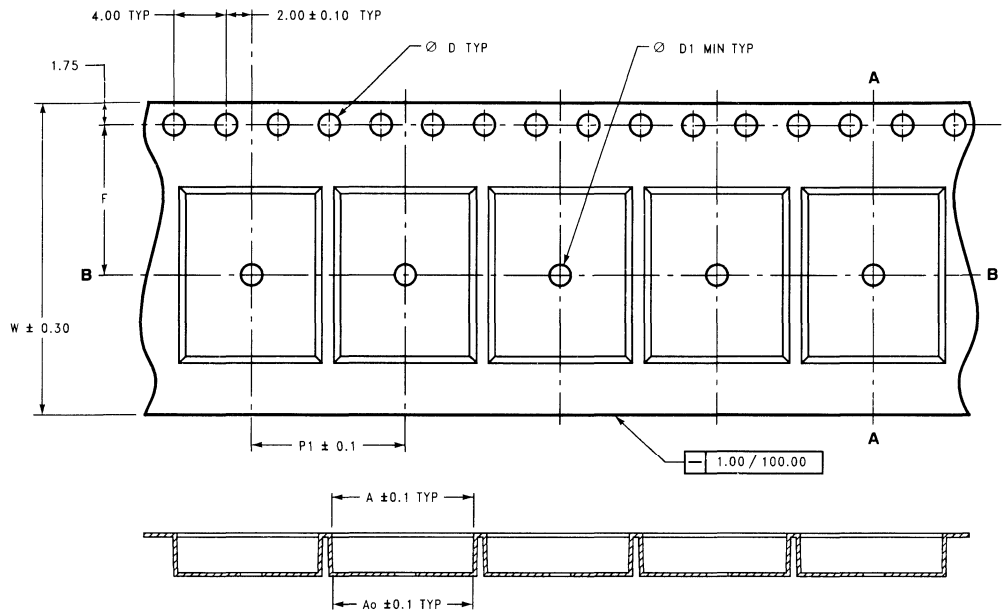
TL/F/12540–25

Plastic Reel Dimensions for 8mm, 12mm, 16mm, 24mm and 32mm Tape

Package Drawing	Tape Size	A	N (Typical)	W1	W2 (Max)
MA05B	8mm	178 (7″)	55	8.4	14.4
MTC14 MTC16	12mm	330 (13″)	178	12.4	18.4
M14A M16A MQA20 MQA24 MSA20 MSA24 MTC20 MTC24	16mm	330 (13″)	178	16.4	22.4
MSC14 MSC16 MSC20	16mm	330 (13″)	80	16.4	22.4
M14D M16D	16mm	330 (13″)	100	16.4	22.4
M20B M24B M20D MTD48 MTD56	24mm	330 (13″)	178	24.4	30.4
MS48A MS56A	32mm	330 (13″)	100	32.4	38.4

Tape Specifications and Drawings

TinyPak™, SOIC, SOP, QSOP, SSOP II, SSOP I



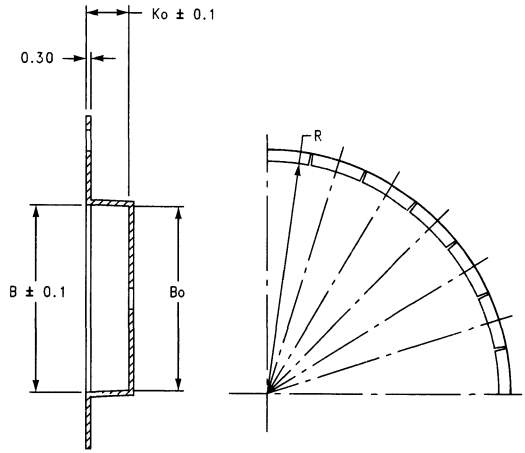
SECTION B – B

TL/F/12540–26

Package Code	Package Description	Package Number	W	F	D	D1	P1	A	A0
M5	5-Lead SOT-23	MA05B	8.0	3.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.04	4.0	3.3	3.15
M	Small Outline Package, JEDEC (SOIC)	M14A	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
M		M16A	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
WM		M20B	24.0	11.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	12.0	11.08	10.9
WM		M24B	24.0	11.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	12.0	11.10	10.9
SJ	Small Outline Package, EIAJ (SOP)	M14D	16.0	7.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.70	8.4
SJ		M16D	16.0	7.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.80	8.4
SJ		M20D	24.0	11.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.70	8.4
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
QSC		MQA24	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0		8.6
MSA		MSA24	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0		8.6
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOP I)	MSC14	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8
MSC		MSC16	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8
MSC		MSC20	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8

Tape Specifications and Drawings (Continued)

TinyPak, SOIC, SOP, QSOP, SSOP II, SSOP I (Continued)



SECTION A – A **BEND RADIUS**

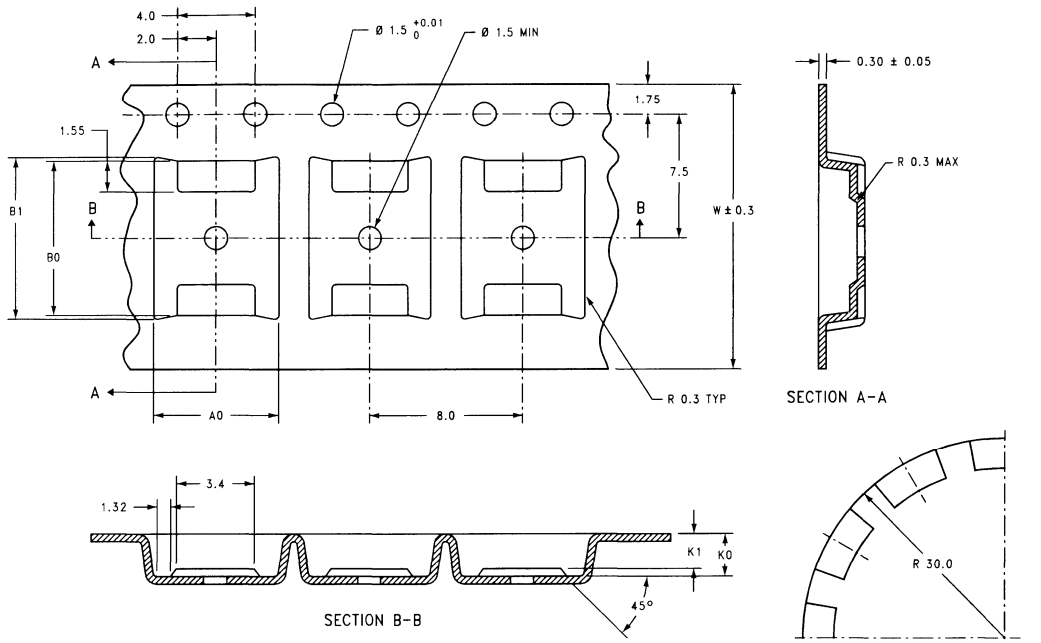
SMALLEST ALLOWABLE BENDING RADIUS.

TL/F/12540–27

Package Code	Package Description	Package Number	B0	B	K0	R (min)
M5	5-Lead SOT-23	MA05B	3.2	3.3	1.4	30.00
M	Small Outline Package, JEDEC (SOIC)	M14A	9.5	9.65	2.1	30.00
M		M16A	10.3	10.45	2.1	30.00
WM		M20B	13.3	13.45	3.0	30.00
WM		M24B	15.9	16	3.0	30.00
SJ	Small Outline Package, EIAJ (SOP)	M14D	10.7	11	2.4	50.00
SJ		M16D	10.7	11	2.4	50.00
SJ		M20D	13.2	13.5	2.4	50.00
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	9.5	9.65	2.1	30.00
QSC		MQA24	9.5	9.65	2.1	30.00
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	7.6		2.5	30.00
MSA		MSA24	8.9		2.5	30.00
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOP I)	MSC14	5.5		1.9	
MSC		MSC16	5.5		1.9	
MSC		MSC20	7.0		1.9	

Tape Specifications and Drawings (Continued)

TSSOP 14, 16, 20 and 24-Lead

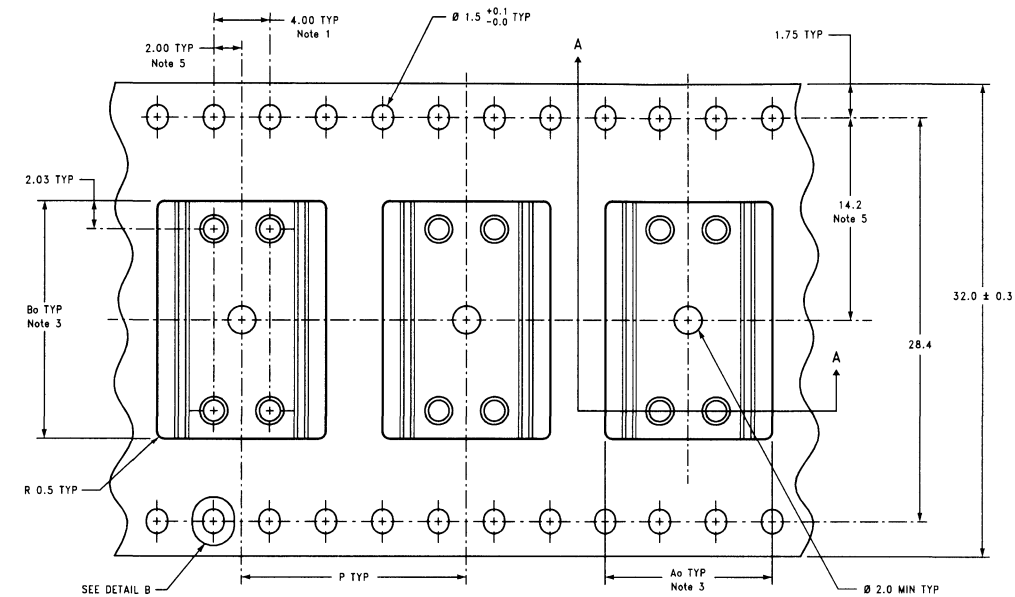


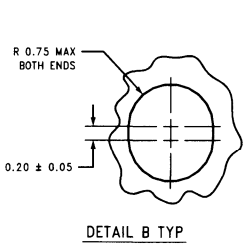
TL/F/12540–28

Package Code	Package Description	Package Number	W	A0	B0	B1	K0	K1
MTC	Thin Shrink Small Outline Package, JEDEC, 4.4mm (TSSOP)	MTC14	12.0	6.95 ± 0.1	5.6 ± 0.1	6.3	1.6	1.2
MTC		MTC16	12.0	6.95 ± 0.1	5.6 ± 0.1	6.3	1.6	1.2
MTC		MTC20	16.0	6.95 ± 0.1	7.1 ± 0.1	7.8	1.6	1.3
MTC		MTC24	16.0	6.95 ± 0.1	8.3 ± 0.1	9.0	1.6	1.3

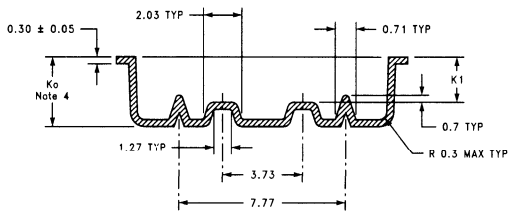
Tape Specifications and Drawings (Continued)

SSOP 48 and 56-Lead

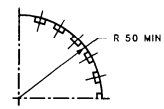




DETAIL B TYP



SECTION A-A



BEND RADIUS

Tape with components shall pass around mandril radius R without damage.
(NOT TO SCALE)

TL/F/12540-29

Note 1: 10 sprocket hole pitch cumulative tolerance ±0.2.

Note 2: Camber not to exceed 1mm in 100 mm.

Note 3: A_0 and B_0 measured on a plane 0.3 mm above the bottom of the pocket.

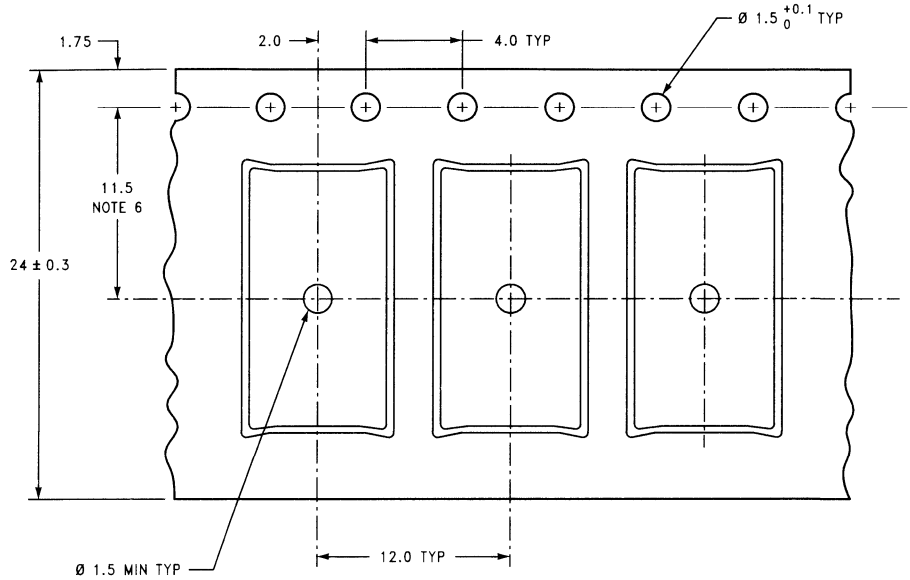
Note 4: K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.

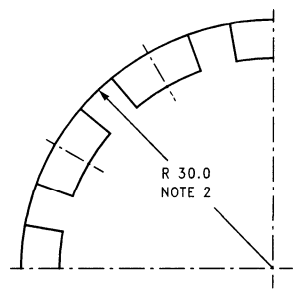
Note 5: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Package Code	Package Description	Package Number	A0	B0	K0	K1	P
MEA	Shrink Small Outline Package, JEDEC (SSOP)	MS48A	12.0	16.2	3.2	2.4	16.0
MEA		MS56A	12.0	18.7	3.2	2.4	16.0

Tape Specifications and Drawings (Continued)

TSSOP 48 and 56-Lead





BEND RADIUS
(NOT TO SCALE)

TL/F/12540–30

Note 1: Cumulative pitch tolerance for feeding holes and cavities (chip pockets) not to exceed 0.2 mm over 10 pitch span.

Note 2: Smallest allowable bending radius.

Note 3: Camber not to exceed 1 mm in 100 mm.

Note 4: Dimensions A_0 and B_0 measured on a plane 0.3 mm above the bottom of the pocket.

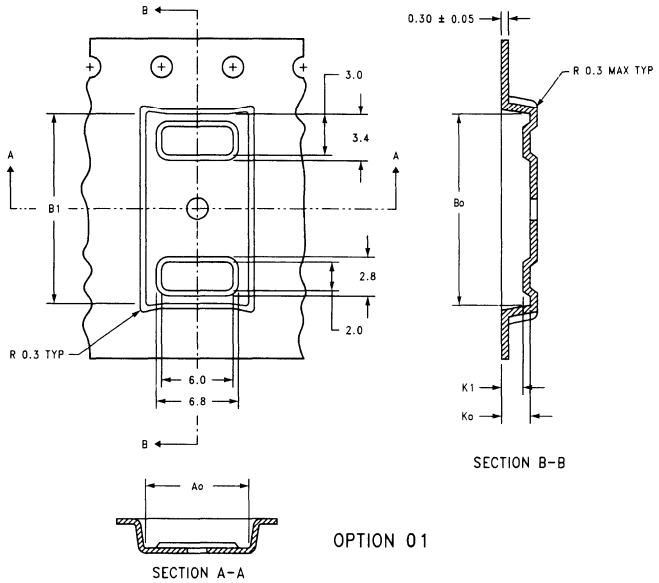
Note 5: Dimension K_0 measured from a plane on the inside bottom of the pocket to the top of the carrier.

Note 6: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

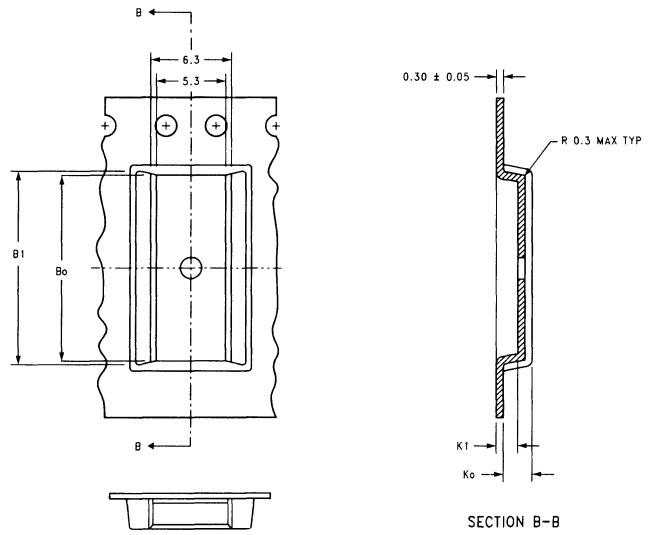
Note 7: Both Option A and Option B pocket designs are acceptable.

Tape Specifications and Drawings (Continued)

TSSOP 48 and 56-Lead (Continued)



OPTION 01



OPTION 02

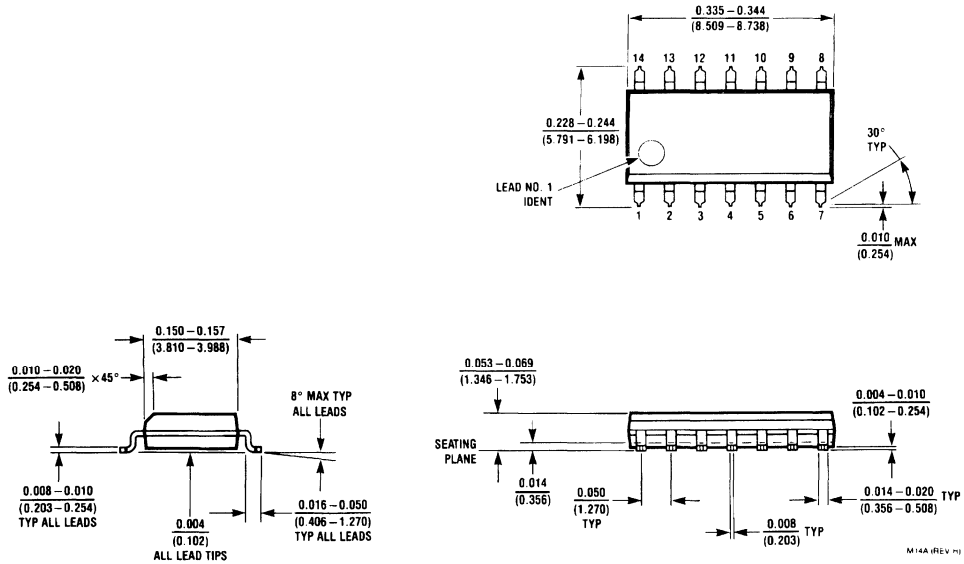
TL/F/12540–31

Package Code	Package Description	Package Number	A0	B0	B1	K0	K1
MTD	Thin Shrink Small Outline Package, JEDEC, 6.1mm (TSSOP)	MTD48	8.6	13.2	13.9	1.6	1.2
MTD		MTD56	8.6	14.5	17	1.8	1.3

National Semiconductor

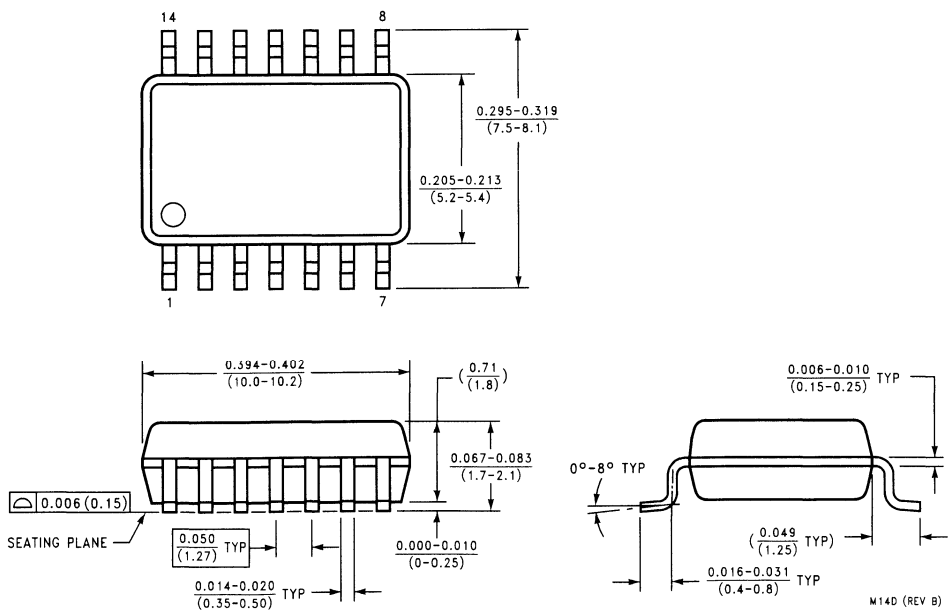
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



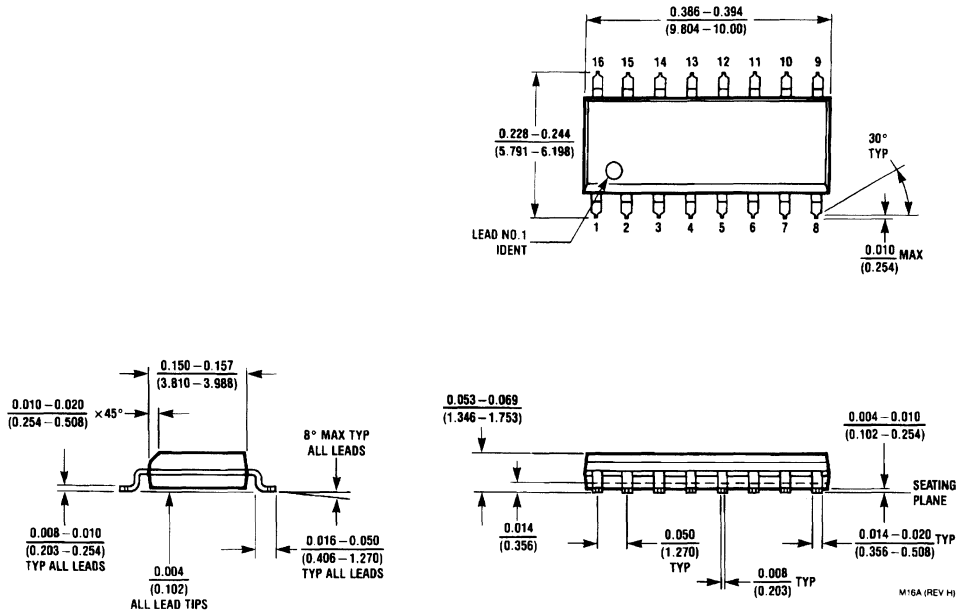
14 Lead Molded Small Outline Package, EIAJ Type II
NS Package Number M14D

All dimensions are in inches (millimeters)



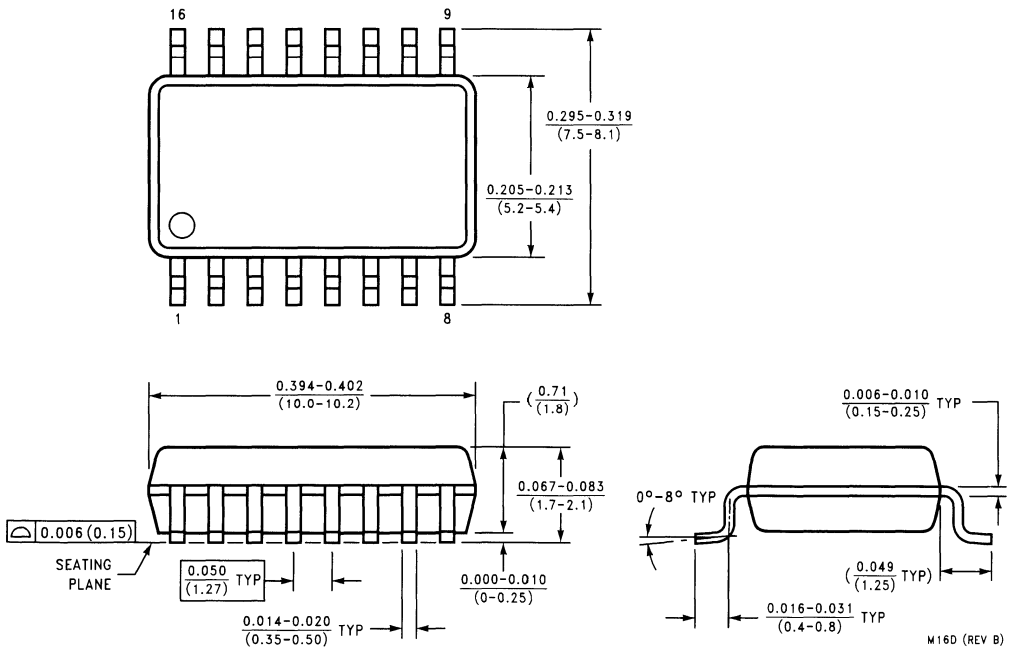
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)



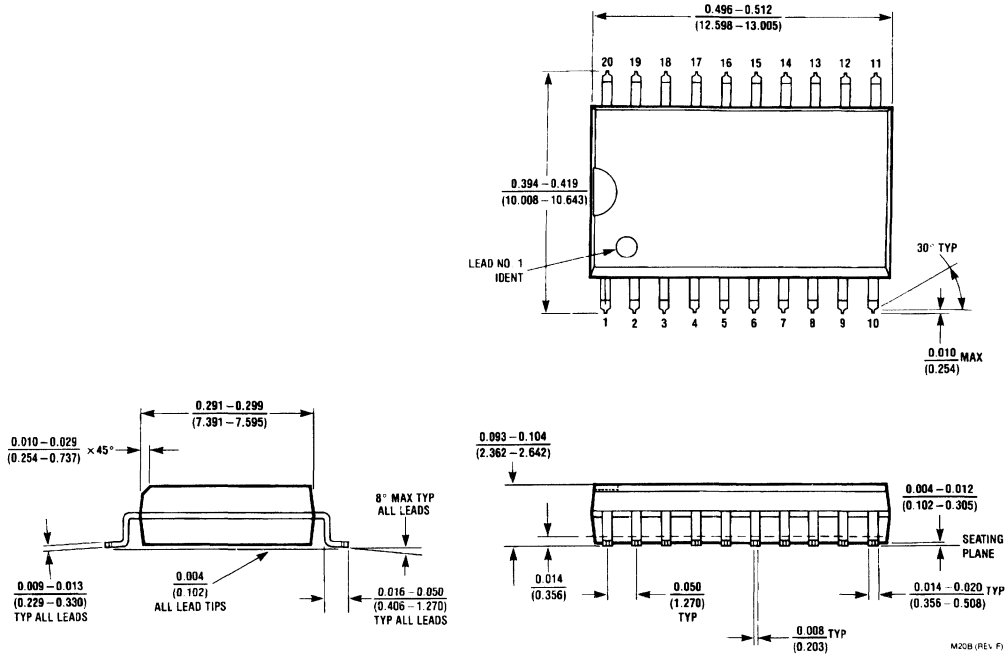
16 Lead Molded Small Outline Package, EIAJ Type II
NS Package Number M16D

All dimensions are in inches (millimeters)



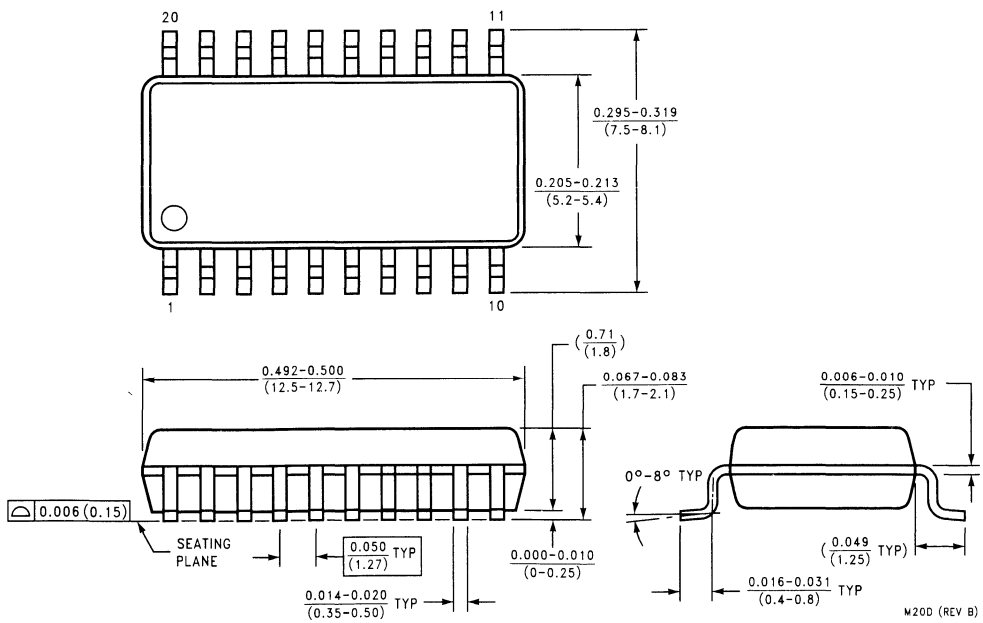
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

All dimensions are in inches (millimeters)



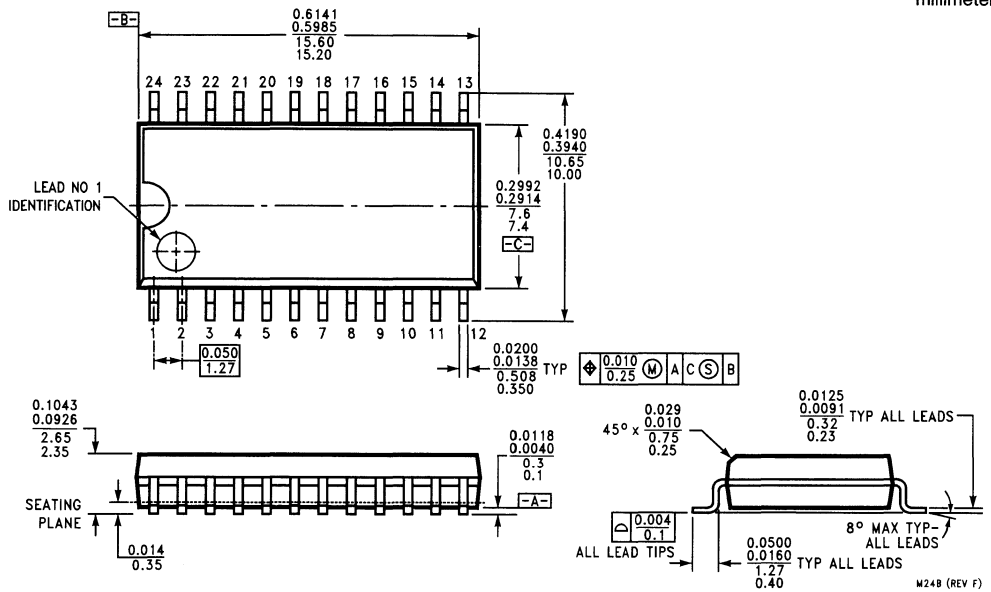
20 Lead Molded Small Outline Package, EIAJ Type II
NS Package Number M20D

All dimensions are in inches (millimeters)



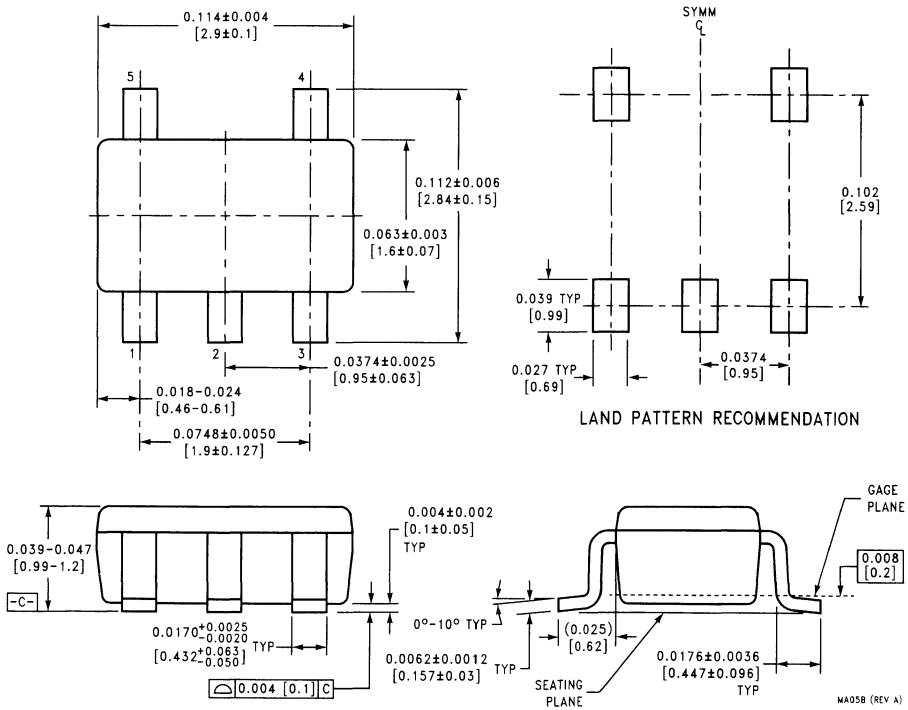
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

All dimensions are in inches / millimeters



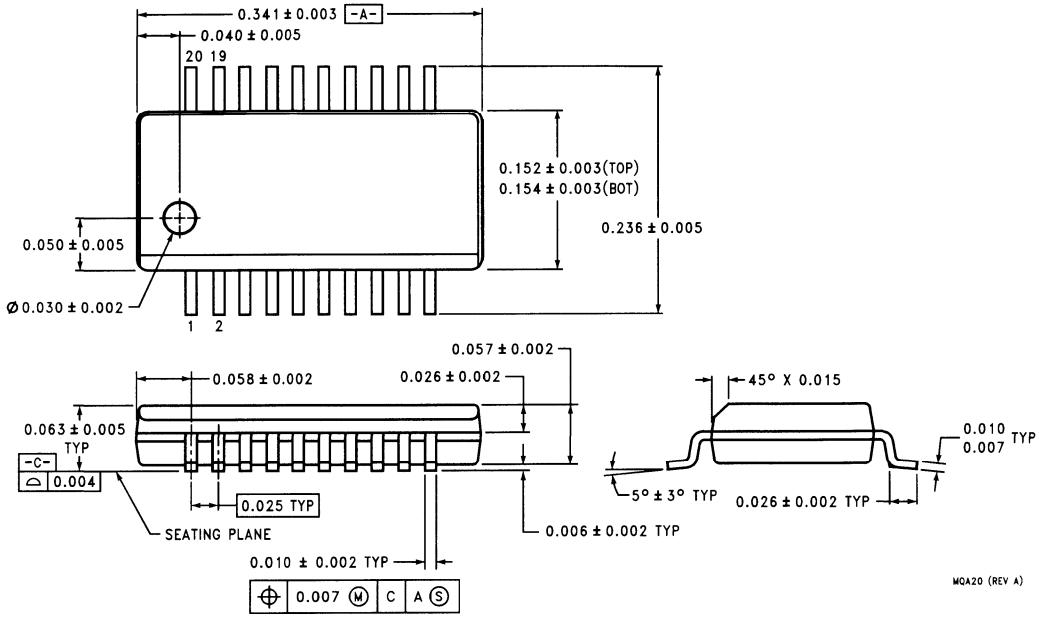
5 Lead Molded SOT-23-5, Enhanced Thermal
NS Package Number MA05B

All dimensions are in inches [millimeters]



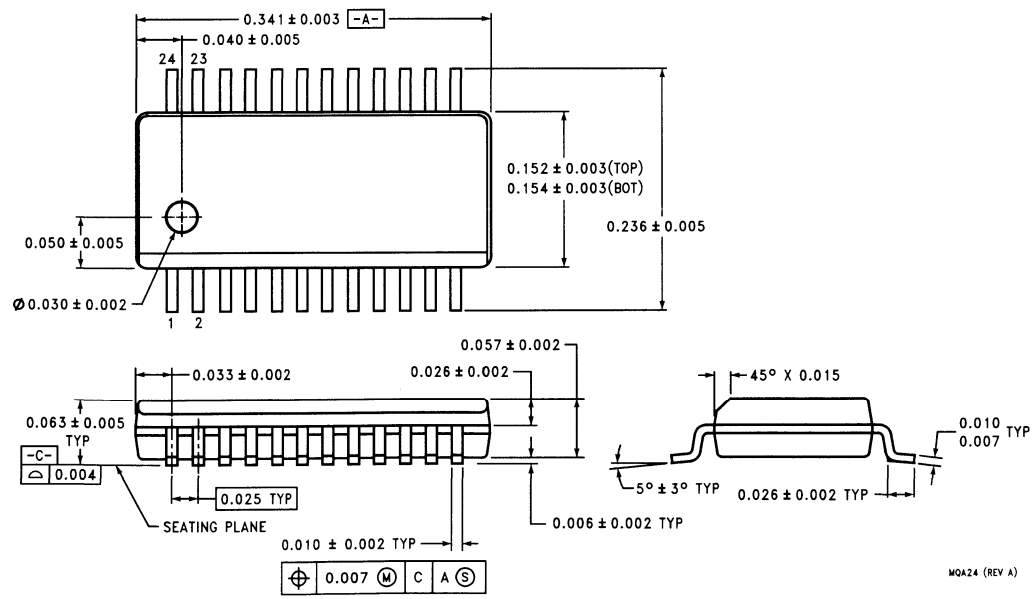
20 Lead (0.150" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MQA20

All dimensions are in inches



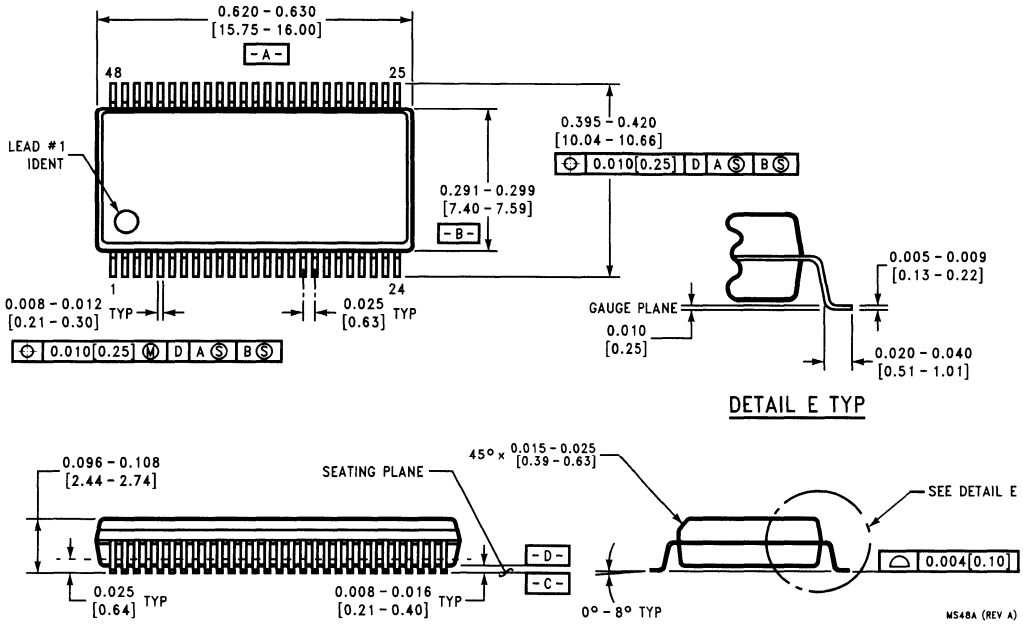
24 Lead (0.150" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MQA24

All dimensions are in inches



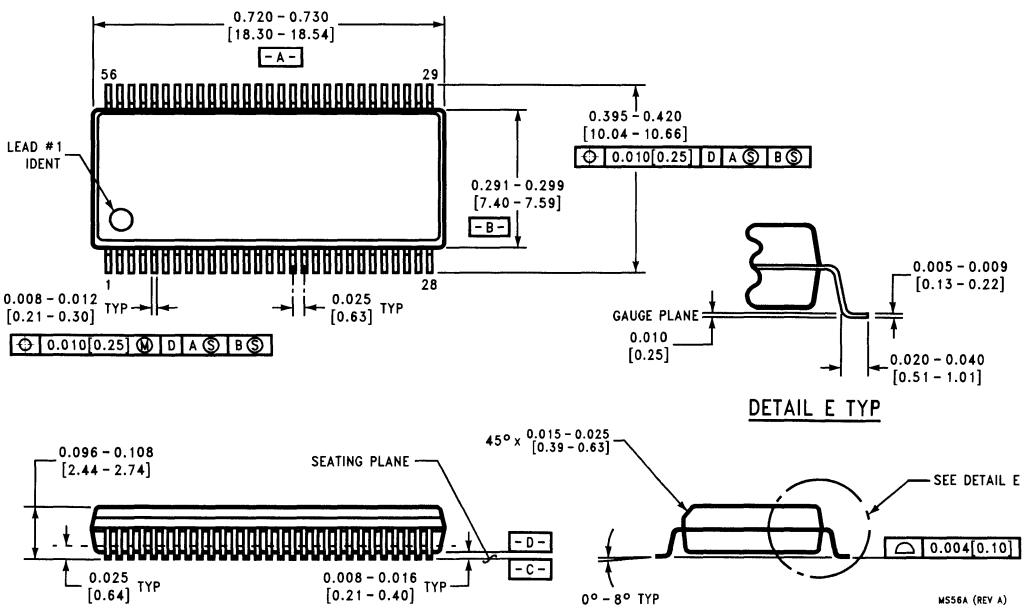
48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS48A

All dimensions are in inches [millimeters]



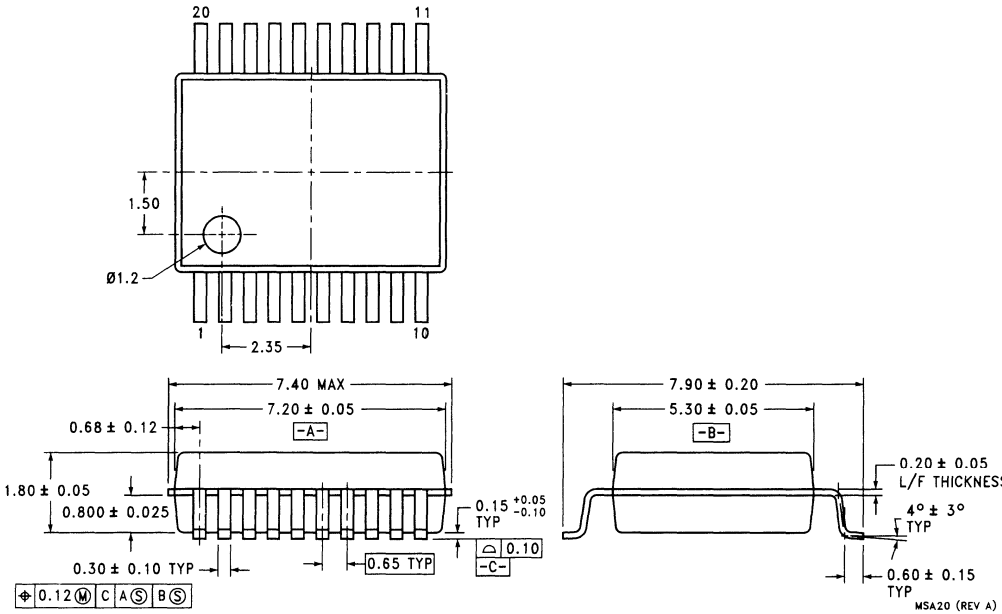
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS56A

All dimensions are in inches [millimeters]



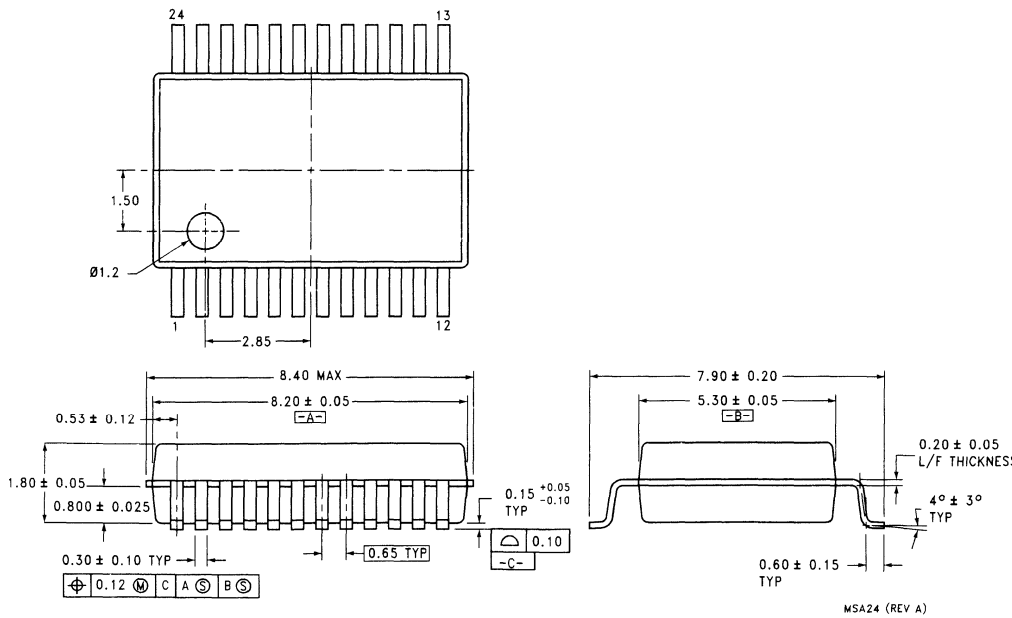
20 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA20

All dimensions are in millimeters



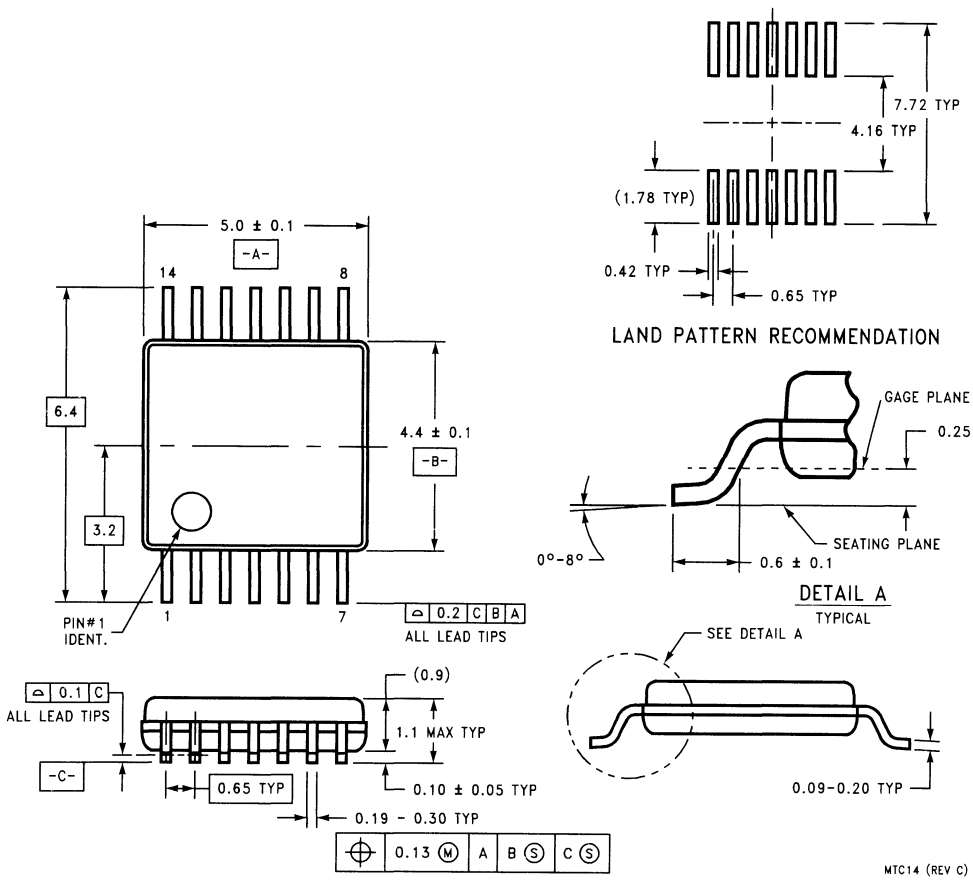
24 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA24

All dimensions are in millimeters



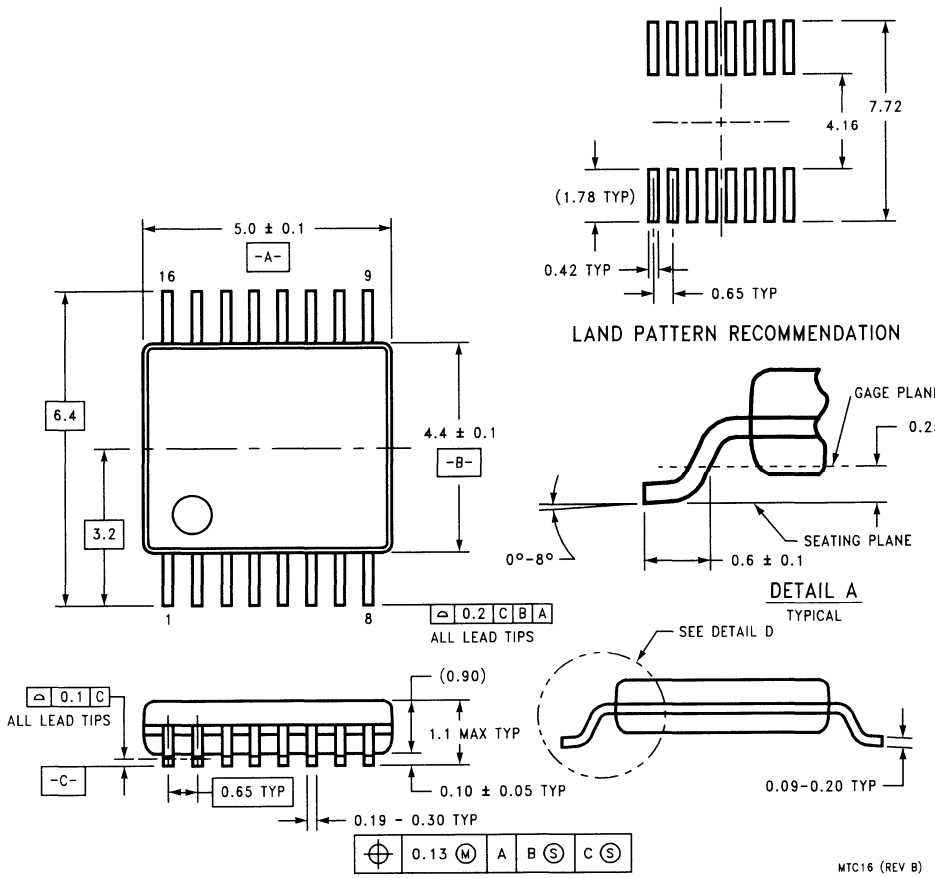
14 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC14

All dimensions are in millimeters



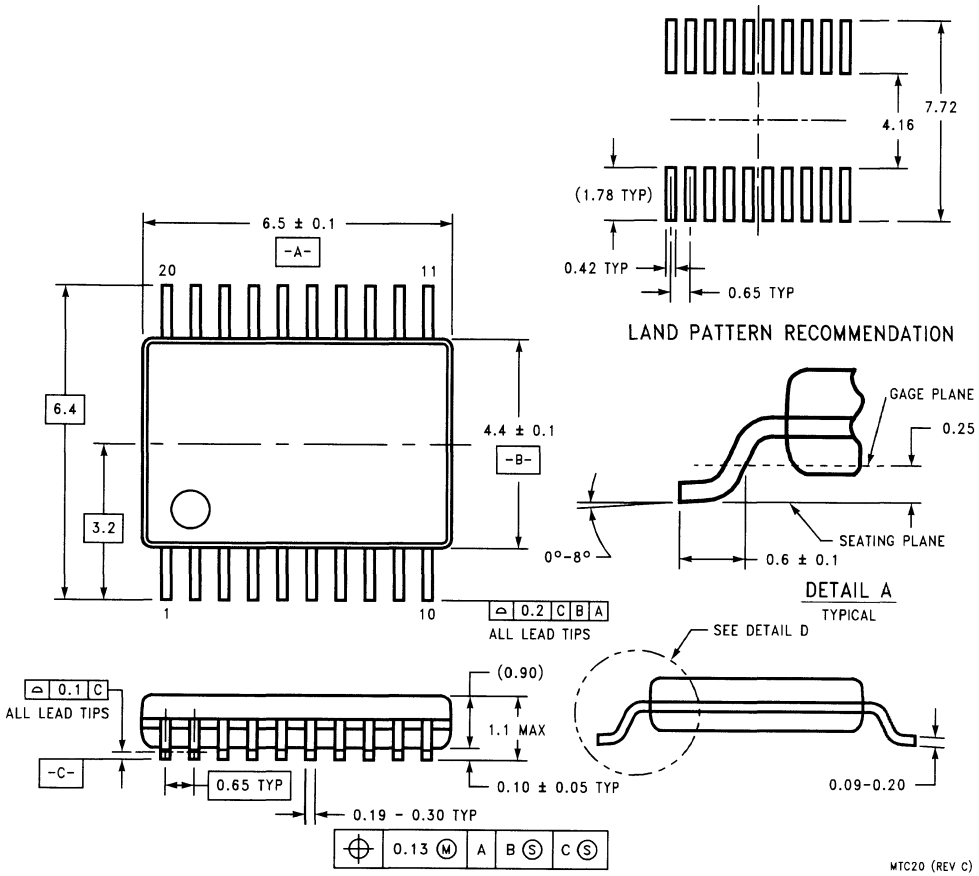
16 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC16

All dimensions are in millimeters



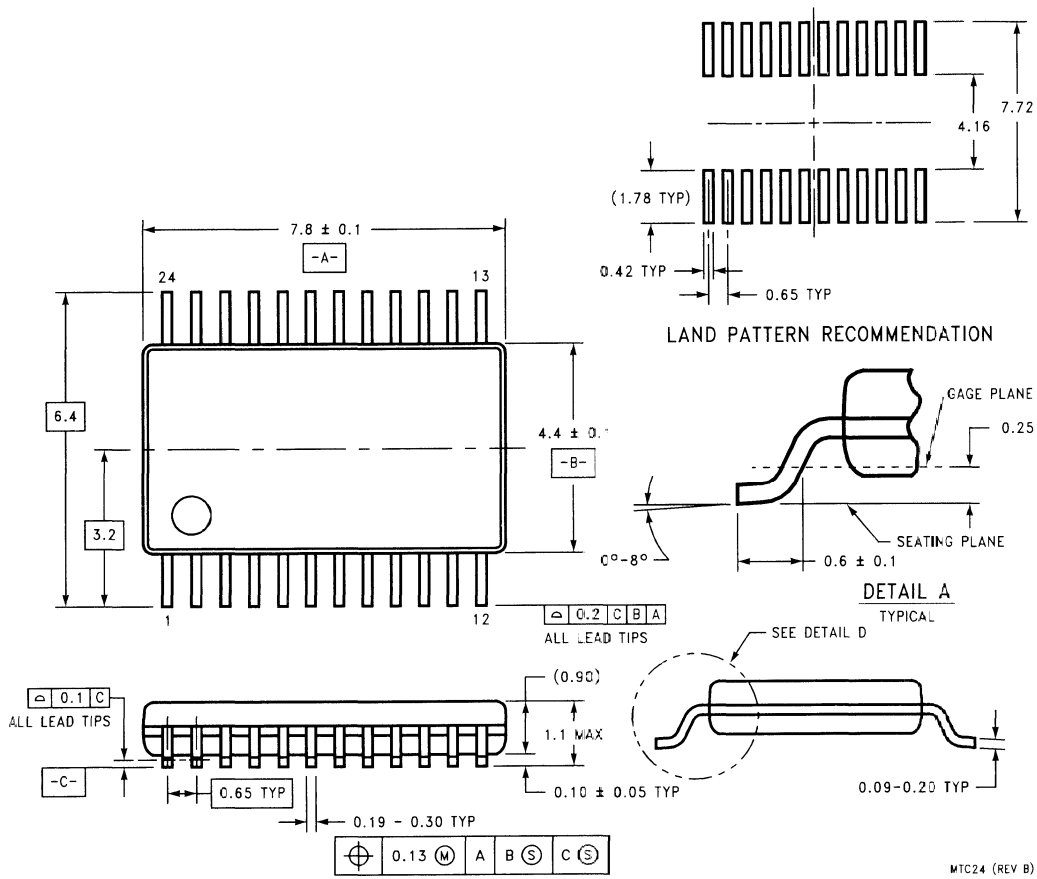
20 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20

All dimensions are in millimeters



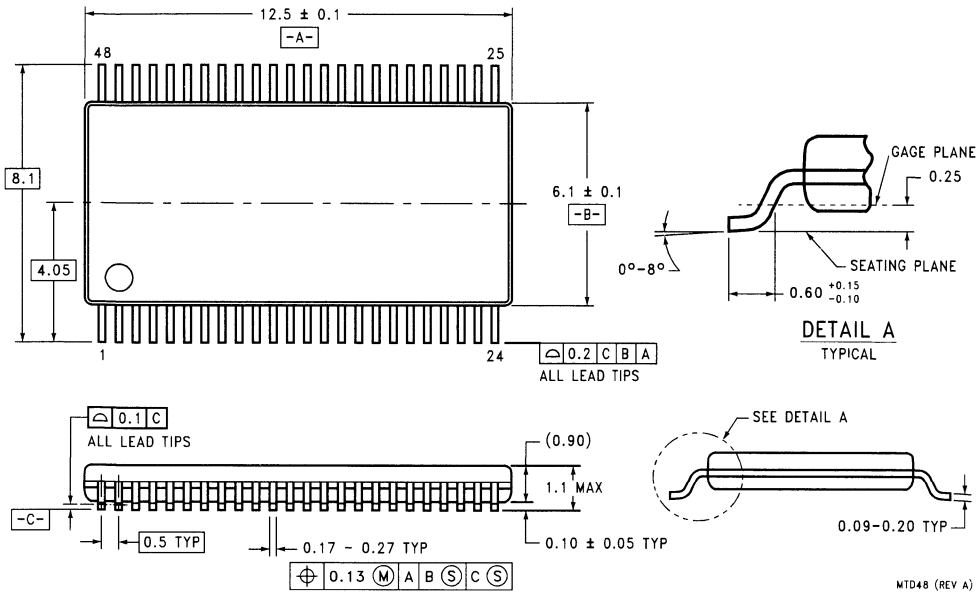
24 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC24

All dimensions are in millimeters



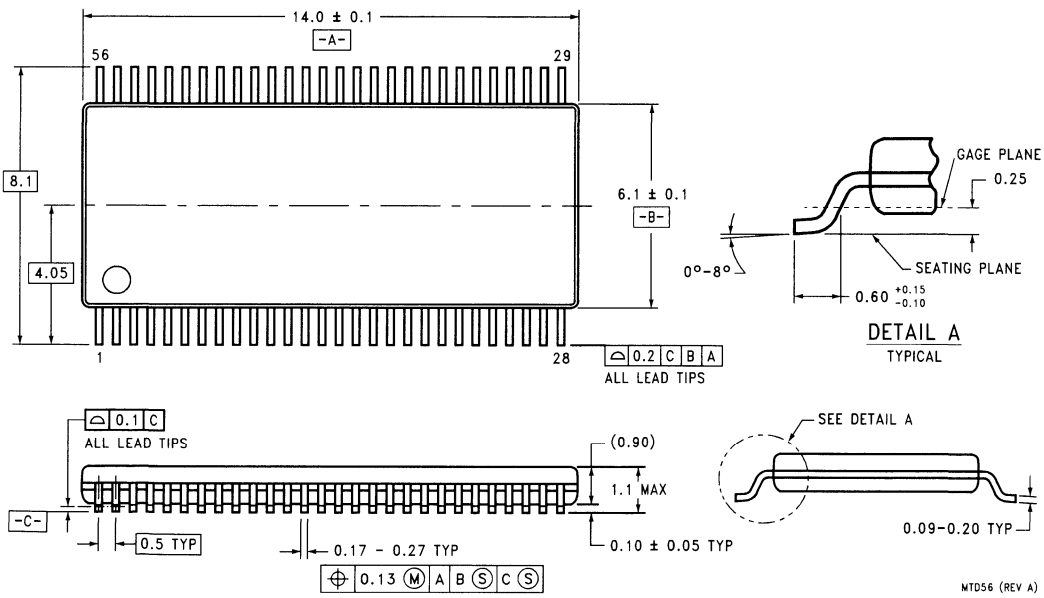
48 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

All dimensions are in millimeters



56 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56

All dimensions are in millimeters



Section 13

Low Voltage Product Reference Guide

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Introduction

For many years, National has been taking a lead in introducing a broad range of new products to meet the needs of designers of portable, battery-operated, and low power systems for all applications.

As the system designer's requirements have evolved in recent years, we have seen the need for not just low-voltage solutions, but more importantly, low-power solutions. As the definitions of "Low Power" have evolved, we have found that lower voltage is not the only path to lower power.

The "Low Power" designer is not always looking for just lower voltage. In addition to lower voltages, lower power can be obtained today using techniques such as: On-board or on-chip power management; Built-in power down capability; New lower-power processes; and Ultra-small packaging.

National offers low power solutions implementing all of these techniques, so whether you are designing with Low-voltage, Mixed-voltage, or 5V only, you can find a National solution that meets your needs.

Format and Usage

This document compiles National's most current low-power/low-voltage/portable applications products in an easy-to-understand format for distribution to National personnel and customers. Updates will be periodically released. This document is intended as a convenient reference to assist in decision making, but does not include all product details.

All products are "Low Power" and are arranged by general application, with individual products grouped by operating voltage levels of 5V, Low Volt (3–3.6V), Very Low Volt (sub 3.0V), and by power consumption (Very Low, Ultra-Low).

The product information is listed in both narrative and chart form so as to include as many critical specifications as possible to assist in making a decision.

For a complete listing of National Semiconductor's broad product line, including recent additions to our line of low-power system solutions, contact your local distributor or call the National Semiconductor Customer Response Group at 1-800-272-9959.

Unless otherwise noted, all products operate at 3.3V V_{CC}, Vin max = V_{CC} (approx.), and are currently available for sale. Literature numbers (#xxxx) are provided at the end of each part description. Contact the National Customer Response Center at 1-800-272-9959, or your local distributor for samples and literature.

Voltage Regulation and Control

SWITCHING REGULATORS; DC TO DC CONVERTERS

Easy-to-use, efficient switching regulators for DC to DC conversion. All feature 4.76–37V inputs, fixed or adjustable outputs, *Switchers Made Simple* Design Software, thermal shutdown and current limit protection.

SIMPLE SWITCHER® Family

- DC to DC converters
- Fixed or Adjustable outputs
- *Switchers Made Simple* Design Software
- Only 4 external components needed
- 150 kHz internal oscillator
- New features: Shutdown/Soft-start, Power Good, Programmable Delay
- Evaluation boards available

Part Number	Output V		Output I	Type	Comments
LM2594	3.3V/5V/12V/Adj	1.23–37V	0.5A	Step-Down	8p SO/DIP; 50% Smaller Solution than LM2574, Lit #107870-001
LM2597	3.3V/5V/12V/Adj.	1.23–37V	0.5A	Step-Down	8p SO/DIP; Features: Power Good Indicator, Programmable Delay, Shutdown/Soft-start; Lit #107467-001
LM2595	3.3V/5V/12V/Adj.	1.23–37V	1.0A	Step-Down	5p TO-220/TO-263; Lit #107871-001
LM2598	3.3V/5V/12V/Adj.	1.23–37V	1.0A	Step-Down	7p TO-220/TO-263; Features: Power Good Indicator, Programmable Delay, Shutdown/Soft-start; Lit #107874-001
LM2596	3.3V/5V/12V/Adj.	1.23–37V	3.0A	Step-Down	5p TO-220/TO-263; Lit #107872-001
LM2599	3.3V/5V/12V/Adj.	1.23–37V	3.0A	Step-Down	7p TO-220/TO-263; Features: Power Good Indicator, Programmable Delay, Shutdown/Soft-start; Lit #107875-001
LM2587	3.3V/5V/12V/Adj.	3.3–60V	5A	Step-Up	Flyback; 5p TO-220/TO-263; Lit #107860-002
LM2588	3.3V/5V/12V/Adj.	3.3–60V	5A	Step-Up	Flyback with Features: ON/OFF, Freq, Adj., Freq. Sync; 5p TO-220/TO-263; Lit #107861-002

LOW DROPOUT (LDO) LINEAR REGULATORS; DC TO DC CONVERTERS

The MICROPOWER family of linear regulators offers: 5V and Low Volt outputs; Very low quiescent current; Electronic shutdown; Built-in thermal shutdown; Current limit protection. Specified for Industrial temperatures.

MICROPOWER Family

- DC to DC converters
- Fixed 3V, 3.3V, 5V or Adjustable outputs
- Electronic Shutdown Mode
- Ultra-small SOT23-/SOIC packages
- Lit #400062, Power ICs Databook

Part Number	Output V	I out	I quies.	Dropout	Comments
LP2980	3V/3.3V/5V	50 mA	65 µA	120 mV	±0.5%or 1%;1 µA in shutdown; SOT23-5; **NEW**: Lit #108590-002
LP2950/2951	3V/3.3V/5V/Adj 1.24–29V	100 mA	75 µA	380 mV	8p DIP/SO; Lit #108568-004 datasheet
LP2952/2953	3.3V/5V/ Adj./1.23–29V	250 mA	130 µA	470 mV	Aux comparator (2953); DX4/P24C apps; 16p DIP/SO; Lit #108569-003
LP2956	Dual Reg @ 5V/Adj 1.23–29V	250 mA/ 75 mA	170 µA	470 mV	16p SO/DIP; Lit #108575-001
LP2960	3.3V/5V/Adj 1.23–29V	500 mA	450µA	470 mV	**NEW**: 16p SO/DIP; Error Flag, Shutdown, Aux comparator; Lit #108585-001
LM3940	3.3V	1A	10 mA	500 mV	**NEW**: TO220/263; Lit #108049-001

PRECISION LINEAR REGULATOR CIRCUIT[1]

The LM3460 is an adjustable, precision controller that is used to build a very high current linear regulator. The output voltage is adjustable between 1.2–3.6V. With good DC accuracy and transient response, this circuit is a very cost effective voltage regulator.

High Current Adjustable Regulator

- Minimal Input/Output Capacitance needed
- Extremely Good Transient Response
- Good DC accuracy (1%)
- Adjustable Output Voltage and Output Current
- SOT23-5 Package
- 50% savings over monolithic solutions

Part Number	Output V	Output I	Type	Comments
LM3460	1.2/1.5/Adj. 1.2–3.6V	Adj 3–8A	Linear	NEW

PRECISION SHUNT VOLTAGE REFERENCES

The MICROPOWER family of Shunt Voltage References offers: Ultra-small SOT-23, and TO-92/SO-8 packages for space-critical applications; No external stabilizing caps; Capacitive load tolerance; Low quiescent current.

MICROPOWER Family

- Low quiescent current
- Ultra small packages
- No external stabilizing caps
- High capacitive load tolerance
- Industrial temperature specs
- Lit #400062, Data Acquisition Databook

Part Number	Type	Vr	Ir	Tolerance ±	Noise	Comments
LM4040-2.5	Precision	2.500V	65 µA–15 mA	.1/.2/.5/1/2%	35uV/rms	150ppm/C max; Lit #108150-003
LM4041-1.2/-Adj	Precision	1.225V/Adj 1.24–10V	60 µA–12 mA	.1/.2/.5/1/2%	20uV/rms	100/150 ppm/C max; Lit #108051-003
LM4431	Standard	2.5V	100 µA–15 mA	2.0%	35uV/rms	SOT23 only; 0°C to 70°C only; Lit #108052-003
LM9140-2.5	Precision	2.5V	60 µA–15 mA	0.5%	35uV/rms	25ppm/C max; TO-92 only; Lit #108310-001

3-TERMINAL ADJUSTABLE REGULATORS

Adjustable Regulators

- Only 3 terminals
- Adjustable outputs down to 1.2V
- Only 2 external resistors needed
- Overload Protection
- 80 dB ripple rejection
- Current limit

Part Number	Output V	Output I	Type	Comments
LM117/317/317A	Adj down to 1.2V	1.5A	Step-Down	Various packages; Lit #106490-001
LM317L	Adj down to 1.2V	100 mA	Step-Down	Various packages; Lit #106490-001
LM138/338	Adj down to 1.2V	5A	Step-Down	TO3, TO220
LM150/350/350A	Adj down to 1.2V	3A	Step-Down	Various packages; Lit #106500-001

1. This application circuit requires the LM3460, a power transistor, and other components to complete the circuit.

PRECISION SECONDARY DRIVER

Ultra-Small TinyPak™—SOT23-F

- 3.3V or 5V
- No external pots or resistors
- Opto-driver
- ±0.5% or 1% initial tolerance
- SOT23-5, 8 DIP
- Lit #108044-001, datasheet

Part Number	Type	Output	Comments
LM3411	Secondary driver	3.3V or 5V	**NEW**: Lit #108044-001 datasheet

SMALL SIGNAL MOSFETS

These MOSFETs feature extremely low threshold voltage making them suitable to be driven by 3V gate drive. Offered in a SOT23 package, these parts are ideal for portable applications.

Very Low Vas

- Fast switching
- Low threshold (3V operation)
- Ultra small package (SOT23)

Part Number	V_{DS} (V)	R_{DS} (ON) Max (W)		ID (A)	P_S (W)
		V_{OH} @ 16V	V_{OH} @ 4.5V		
N-Channel					
2N7002	60	7.5	7.5 @ 5V	0.115	0.2
BSS123	100	6		0.17	0.36
BSS138	50	3.5	6	0.22	0.36
MMBF170	60	5		0.5	0.3
NDS7002A	60	2	3 @ 5V	0.28	0.3

Operational Amplifiers

LOW VOLT AND VERY-LOW VOLT CMOS OP-AMPS

- Single supply operation
- High Speed; Special Functions
- Rail-to-Rail operation
- Industrial/Military
- DIP/SOIC and Ultra-small SOT23
- Lit #400061, Op Amps Databook

Part Number	GBW	Type	Supply	Is/chnl	Ib Max	Vos Max	Comments
LM6142/4	17 MHz	2/4	1.8–24V	650 µA	526 pA	1/2.5 mV	CMR=3.2V typ; DIP/SO; Lit #108245-002 datasheet
LMC6582/4	1.2 MHz	2/4	1.8–10V	700 µA	10 pA	1/3 mV	**NEW**: CMR=3.2V typ; 8/14p DIP/SO; Lit #108487-002
LMC6681/2/4	1.2 MHz	1/2/4	1.8–10V	700 µA	10 pA	1/3 mV	**NEW**: LMC6582 plus Shutdown; Lit #108489-002
LM7121	235	1	5–30V	5.3 mA	12 µA	15 mV	**NEW:** VFA; SOT23-5; Lit #108303-002
LM7131	70 MHz	1	3–10V, ±5V	8 mA	40 µA	2/7 mV	Flash A/D; Video Cable driver; CMR=3.2V typ; SOT23; 8pSO; Lit # 108305-001 datasheet
LMC6482/4	1.5 MHz	2/4	3–15V	500 µA	4/10 pA	.75/3 mV	**CMR=5V typ**; 8/14p DIP/SO; Lit #108480-002 datasheet
LMC6492/4	1.5 MHz	2/4	3–15V	500 µA	200 pA	3/6 mV	Not guaranteed at 3.3V; Mil temp; 8/14p DIP/SO; Lit #108485-001
LMC7101	1.0 MHz	1	3–15V	500 µA	64 pA	4/7 mV	SOT23 TinyPak; Lit #108491-002 datasheet
LM6132/4	10 MHz	2/4	2.7–24V	360 µA	300 nA	2/6 mV	**NEW**: Rail-To-Rail Input and Output; Lit #108244-001

ULTRA-LOW POWER; LOW VOLT AND 5V CMOS OP-AMPS

The MICROPOWER Family of op amps offers: 5V and Low Volt operation; Very low quiescent current; Built-in thermal shutdown; Current limit protection. (A wide range of other op-amps is also available).

MICROPOWER Family

- Low Volt and 5V operation
- Very low quiescent current
- Rail-to-Rail operation
- Industrial temperatures
- Lit #400061, Op-Amps Databook

Part Number	GBW	Type	Supply	Is/chnl	Ib Max	Vos Max	Comments
LMC7111	.04 MHz	1	2.7–10V	25 µA	20 pA	5/7 mV	**NEW**: SOT23; Lit #108493-002
LMC6462/4	.050 MHz	2/4	3–15V	20 µA	10/200 pA	.5/3 mV	NEW: CMR=5.2V typ; Lit #108478-001
LMC6572/4	0.22 MHz	2/4	2.7–5V	40 µA	10 pA	3/7 mV	**NEW**: CMR-2.2V typ; Lit #108490-002
LMC6022/4	0.35 MHz	2/4	5–15V	40–43 µA	200 pA	9 mV	LOW COST; 0.5 mW; 8/14p DIP/SO; Lit #108447-001
LMC6041/2/4	75/.1 MHz	1/2/4	5–15V	10–14 µA	4 pA	3/6 mV	8/14p DIP/SO; Lit #108469-001
LMC6061/2/4	0.1 MHz	1/2/4	5–15V	16–20 µA	4/100 pA	.35/.80 mV	Precision; 8/14p DIP/SO; Lit #108454-002
LPC660/1/2	0.35 MHz	1/2/4	5–15V	43–55 µA	4/100 pA	3/6 mV	Rail-To-Rail Output; Lit #108565-002

ULTRA-SMALL PACKAGING OP AMPS AND COMPARATORS

The first of our **TinyPak™ Family** of op-amps packaged in **SOT-23**: **The smallest available package in the industry.** On Tape & Reel only.

- LM7131—70 MHz GBW; Single; 3–10V; See low volt CMOS Op Amps above for details
- LMC7101—1.0 MHz GBW; Single; 3–15V; See low volt CMOS Op Amps above for details
- LMC7111—Dual/Quad; 2.2–10V; See Ultra-low Power, Low Volt and 5V CMOS Op Amps above for details
- Lit #400061, Op Amps Databook

Part Number	Type	Supply	$I_{s/chnl}$	I_B typ	V_{OS} typ	t_r/t_f	t_{PHL}/t_{PLH}*	Comments
LMC7211	single	2.7–15V	7 µA	0.04 pA	5 µA	0.3µ sec	4µ sec	Micropower; RR input; push-pull output; Lit #108495-003
LMC7221	single	2.7–15V	7 µA	0.04 pA	5 mA	0.3µ sec	4µ sec	Micropower; RR input; open drain output; Lit #108497-002
LMC6762	dual	2.7–15V	6 µA	0.04 pA	5 mA	0.3µ sec	4µ sec	Micropower; push-pull output; Lit #108486-001
LMC6772	dual	2.7–15V	6 µA	0.04 pA	5 mA	0.3µ sec	4µ sec	Micropower; open drain output; Lit #108488-001
LM7121	single	2.7–15V	5.3 µA	5.5 pA	8 µA	0.3µ sec	4µ sec	High speed; low power; voltage feedback amp; Lit #108303-001

* overdrive = 100 mV

VOLTAGE COMPARATORS; LOW POWER CMOS; SINGLE SUPPLY

A wide variety of other comparators are also available. ■ Lit #400012, Op Amps Databook

Part Number	Type	Supply	I typ	Bias	Leak	Off V	Off I	Comments
LM1801	9V battery	8–14V	7 µA	2 nA	5nA	5 mV	0.5 nA	1yr standby; On chip zener, clamps, 2 refs; Low battery detect; Horn driver; 14p DIP; 500 mA o/c output
LM339A/ LM393A	quad/dual	2–28V	800 µA/ 400 µA	25 nA	0.1nA	±1 mV	±5 nA	Precision; Near GND sensing; TTl/CMOS in; All types outputs; 14p DIP/SO
LP339	Precision quad	2–36V	60 µA	na	0,1 nA	±2 mV	±0.5 nA	Ultra Low Power LM339A
LP311	Industry Standard	3–36V	150 µA	15 nA	0.2 nA	2 mV	2 nA	1.2uS response; 25 mA o/c output; 900 mW max@5V; 8p DIP; Low Pwr
LP365/A	Quad	4–36V	215 µA/ 225 µA	15 nA/ 10 nA	2 nA	±3/1 mV	±4 nA/ 2 nA	TTL/CMOS inputs; All type outputs; Single R configurable; Near GND sensing; 14p DIP/SO

Audio Power Amplifiers

AUDIO AMPS; LOW VOLT CMOS

The first of our **Boomer® Family** of audio power amplifiers designed for portable, low power applications; Thermal shutdown; Headphone I/O; Single supply operation.

BOOMER® Family

- Bridge-Connected (BTL) or Stereo Single-Ended
- Unity-gain stable
- External 1–10 selectable gain
- No external capacitors or snubbers
- Lit #108154-001, LM4860 datasheet
- Lit #108153-001, LM4861 datasheet
- Lit #108156-001, LM4862 datasheet
- Lit #108170-001, LM4880 datasheet

Part Number	Type	Power (cont.)	Supply	Icc/standby	THD	Comments
LM4860/ LM4861	Single Single	1W @ 8ohms/ 0.5W @ 8ohms	2.7–5.5V	6.5 mA/0.6 µA	<1%	**NEW**: 16p SO; 8p SO; Lit #108154-001, #108153-001
LM4862	Single	400 mW	2.7–5.5V	6 mA/0.7 µA	<1%	SO8 or DIP 8; Lit #108156-001
LM4880	Stereo	325 mW	2.7–5.5V	6 mA/0.7 µA	<1%	SO8 or DIP; Lit #108170-001
Other audio amplifiers; Lit #400060, Linear Applications Specific Databook						
LM1896	Stereo& BTL	250 mW @4ohms	3–9V	15 mA/na	.09% typ	Sensitive AM apps; No "pop"; 14p DIP, 11p SIP
LM386	Single	325 mW @8ohms	4–12V	4 mA/na	10%	20–200 adj gain; 8p SO
LM390	Single	1W @ 8ohms	4–9V	10 mA/na	10%	20–200 adj gain; 14p SO

Video Amplifiers

LOW VOLT; HIGH SPEED VIDEO AMPLIFIER

Part Number	GBW	Type	Supply	Is/chnl	Ib max	Vos max	Comments
LM7131	70MHz	Single	3–10V, ±5V	8 mA	40 µA	2,7 mV	Flash A/D; Video Cable driver; CMR=3.2V typ; SOT23-5; 8pSO; Lit #108305-001 datasheet

13

Timing, Clock Management, Frequency Dividers

REAL TIME CLOCKS (RTC); LOW VOLT SUPPLY

This family of **CMOS RTCs** has an architecture that looks like a contiguous block of memory or I/O ports, organized as 2 software selectable pages of 32 bytes (unused on-board RAM may be used as system CMOS RAM). All devices include: Day of week/years counter; 4 selectable osc frequencies; Parallel resonant osc; On-chip interrupt structure; Integrated power failure logic and control.

CMOS RTC Family

- Single Supply or Battery operation
- 3–3.6V V_{CC}, or 2.2V min battery
- 12/24 hr timekeeping to 1/100s
- On-board system RAM
- 4 selectable oscillator frequencies
- Lit #400009, Real-Time Clock Handbook

Features	LV8571A	LV8572	LV8573A
TimeKeeping			
Mode	12 or 24 Hour	12 or 24 Hour	12 or 24 Hour
Range	0.01 sec thru Years	0.01 sec thru Years	0.01 sec thru Years
Leap Year	Yes	Yes	Yes
Rollover	Status Bit	Status Bit	Status Bit
Bus			
Mode	Parallel	Parallel	Parallel
Address (# Bits)	5	5	5
Data (# Bits)	8	8	8
Max Access Time (Address to Data Valid)	100 ns	100 ns	100 ns
RAM			
On-Chip	44 Bytes	44 Bytes	14 Bytes
Timer	2 16-Bit	No	No
Interrupts			
Programmable	0.001 sec thru 1 min	0.001 sec thru 1 min	0.001 sec thru 1 min
Alarm Compare	Yes	Yes	Yes
Standby Mode	Yes	Yes	Yes
Status Register	Yes	Yes	Yes
Timer	Yes	No	No
Timebase			
Oscillator Frequency	4 Selectable (Note 1)	4 Selectable (Note 1)	32.768 kHz
Buffered Oscillator Output	Yes	Yes	Yes
Power Supply			
Voltage			
Operational	3–3.6V	3–3.6V	3–3.6V
Standby	2.2V min	2.2V min	2.2V min
Current (32.768 kHz)			
Operational	5 mA	5 mA	5 mA
Standby (I_{DD} Max)	8 µA	8 µA	8 µA

Note 1: 32 kHz, 32.768 kHz, 4.194304 MHz, 4.9152 MHz.
Note 2: Socket equivalent pinouts.

Features	LV8571A	LV8572	LV8573A
Process Technology	microCMOS	microCMOS	microCMOS
Packaging			
Pins/Type	24 DIP (Note 2)	24 DIP (Note 2) 28 PLCC (Note 2)	24 DIP (Note 2) 28 PLCC (Note 2)

Note 1: 32 kHz, 32.768 kHz, 4.194304 MHz, 4.9152 MHz.
Note 2: Socket equivalent pinouts.

LOW SKEW CLOCK BUFFER/DRIVERS; LOW VOLT SUPPLY

- 2.0–6.0V, or 3.0–3.6V CMOS
- Very low power
- Commercial/Industrial
- Designed for signal generation and clock distribution
- Lit #400046, CGS™ Design Databook

Part Number	Outputs	V_{CC}	Drive	f Max	tpd, ns	Out skew	Package
CGS74LCT2524	1 to 4@1X	3–3.6V	±12 mA	75 MHz	15 max	300 ps	8p SOIC
CGS74C2525 single clock input	1 to 8@1X	2–6V	±24 mA	65 MHz	12.5 max	600 ps max	14p DIP/FP/SO, 20p LCC
CGS74C2526 dual, mux'd clk in.	1 to 8@1X	2–6V	±24 mA	65 MHz	14 max	600 ps max	14p DIP/FP/SO, 20p LCC

MEMORY ARRAY CLOCK DRIVERS; LOW VOLT OR 5V SUPPLY

These devices are specifically designed for high speed arrays with large fanouts; Quad 1 to 4 outputs; 3.3V or 5V operation (max V_{CC}=7V); 5V tolerant inputs; TTL/CMOS compatible; ±24 mA; fmax=125MHz (typ @ –40/+85, 50pf); 350ps max pin-to-pin skew; 650ps max part-to-part skew; 1.5ns max tr/tf; 2kV ESD; 28p PLCC.

- 3.3V or 5V CMOS
- 5V tolerant inputs
- Very low power
- Quad 1-to-4 outputs
- fMax = 125 MHz typical
- Commercial/Industrial
- Lit #400046, CGS™ Design Databook

Part Number	Output	I_{OH}/I_{OL}	tpd, ns	tr/tf, ns	Out skew	3V Fmax	Package
CGS2535	16 @1X non invert	±24 mA	3.5 max	1.0 max	350 ps max	100 MHz	28p PLCC
CGS2536	4 @1X + 4 @0.5X inverting 4 @1X + 4 @0.5X non inverting	±24 mA	4.5 max	1.0 max	350 ps max	100 MHz	28p PLCC

Family Logic and Logic Converters

LCX HIGH-PERFORMANCE CMOS LOGIC; LOW VOLT SUPPLY; 5V TOLERANT

High performance logic for use in low voltage and mixed voltage systems; Popular 8 and 16 bit, gates, and MSI functions; 4.5ns and 6.5ns max t_{PD}; ±24 mA drive; 10 µA I_{CCQ}; Power-down high-Z; TTL compatible I/Os; Commercial/Industrial; SOIC/SSOP/TSSOP; (Alternate sourced by Toshiba, Motorola, and SGS-Thomson).

CROSSVOLT™ LCX Family

- 4.5 ns and 6.5 ns max t_{PD} (16-bit and octal)
- 2.0–3.6V supply
- 5V tolerant inputs/outputs
- Power down high impedance for power management and live insertion
- 10 µA I_{CCQ}; ±24 mA drive
- 1996 *CROSSVOLT* Logic Series Databook

LVX MEDIUM-PERFORMANCE CMOS LOGIC; LOW VOLT SUPPLY; 5V TOLERANT

Medium performance logic for use in low voltage and mixed voltage systems; Popular 8 bit, gates, and MSI functions; 12.0 ns max t_{PD}; ±4 mA drive; 40 µA I_{CCQ}; TTL compatible I/Os; Commercial/Industrial; SOIC/SSOP/TSSOP; (Second sourced by Toshiba).

***CROSSVOLT*™ LVX Family**

- 12.0 ns max t_{PD}
- 2.0–3.6V supply
- 5V tolerant inputs
- 40 µA I_{CCQ}; ±4 mA drive
- 1996 *CROSSVOLT* Logic Series Databook

LVQ MEDIUM-PERFORMANCE CMOS LOGIC; LOW VOLT SUPPLY; LOW VOLT ONLY

Medium performance logic for use in low-volt only systems; Most 8 bit, gates, and MSI functions; 10.5 ns max t_{PD}; ±12 mA drive; 50 µA I_{CCQ}; TTL compatible I/Os; Commercial/Industrial; SOIC/QSOP; Military CDIP/FPAK/LCC; (Alternate sourced by Toshiba, Motorola, and SGS-Thomson).

***CROSSVOLT*™ LVQ Family**

- 10.5ns max t_{PD}
- 2.0–3.6V supply
- 50 µA I_{CCQ}; ±12 mA drive
- 1996 *CROSSVOLT* Logic Series Databook

LVT HIGH-PERFORMANCE BICMOS LOGIC; LOW VOLT SUPPLY; 5V TOLERANT

Very high output drive logic for use in backplane driving applications; Popular 8 and 16 bit functions; Sub 4 ns typical; +64/–32 mA drive; Power up/down high-Z; TTL compatible I/Os; SOIC/SSOP/TSSOP; (Replaces Philips LVT and TI LVT/LVTZ).

***CROSSVOLT*™ LVT Family**

- Sub 4 ns typ tpds
- 2.7–3.6V operation
- 5V tolerant inputs/outputs
- Low I_{CC}; +64/–32 mA drive
- 1996 *CROSSVOLT* Logic Series Databook

SPECIALIZED 3V/5V TRANSLATORS

74LVX3245/4245 dual supply translators will level shift 0–3.3V LVTTL input swings to 0–5V CMOS-level swings. 74LVXC3245/4245 configurable dual supply translators also allow V_{CCB} to be either 3V or 5V and allow floating B-port for modular applications. 74LVX3L383/384 bus switch devices provide switching, bus exchange, and 5V to 3V translation functions; SOIC/QSOP/TSSOP.

***CROSSVOLT*™ Translators**

- Special purpose translation
- Low power
- High speed
- 1996 *CROSSVOLT* Logic Series Databook

Part Number	Description	Bits	t_{PD}	I_{CC}	Drive
74LVX3245/4245	Dual supply translators	8	7.5 ns	80 µA	±24 mA
74LVXC3245/4245	Configurable dual supply translators	8	7.5 ns	80 µA	±24 mA
74LVX3L383/384	Bus switches (replaces QuickSwitch®)	10	0.25 ns	10 µA	None

Memory

CMOS EPROM; LOW POWER; LOW VOLT SUPPLY

The high performance LOW VOLTAGE (LV) Family is available now in 3.0–5.5V, or 2.7–3.6V operation; 2kV ESD; 200 mA latchup immunity; Very low power; TSOP and PLCC (OTP) packaging.

LOW VOLTAGE (LV) Family

- 3.0–5.5V, or 2.7–3.6V (B) operation
- Very low power
- 200 mA latchup immunity
- Commercial/Industrial
- Lit #400073, Memory Databook

Part Number	Size	Config	Speeds, ns	Icc (typ)/st.by	Packages
NM27LV010	1M	128kx8	150–300	8 mA/15 µA	TSOP/PLCC
NM27LV010B	1M	128kx8	200/250	8 mA/15 µA	TSOP/PLCC
NM27LV020	2M	256kx8	150/250	10 mA/10 µA	PLCC/TSOP
NM27LV020B	2M	256kx8	200/250	10 mA/10 µA	PLCC/TSOP

CMOS SERIAL EEPROMS (SYNCHRONOUS BUS); VERY LOW VOLT

The MICROWIRE/I2C Families with industry standard serial interfaces; 256/1K/2K/4K/16K bits; 16bit registers; Read voltages of 2–5.5V (L), 2–6V (LZ), and 1.8–4.0V (XLZ); 40 year data retention; 1M data changes; Direct-write, no erase cycle required; Self-timed programming cycle (5ms typ), with programming status on output pin; Commercial and Industrial; 8 pin DIP/SO.

MICROWIRE/I2C Families

- 2–5.5V (L), 2–6V (LZ), 1.8–4V (XLZ)
- 16 bit registers
- 1M data changes/40 year data retention
- Direct Write (no erase required)
- Self-timed programming
- Commercial/Industrial
- Lit #400073, Memory Databook

Part Number	I/O	Size	Config	V_{CC} min Rd/Wr	Icc typ/st.by	wr.pr.	# inst
The MICROWIRE Family has a MICROWIRE bi-directional serial interface, 8 pin DIP and 8 pin SO.							
NM93C06/46/56/66L	MW	256–4K	16–256x16	2.0V/2.5V	400 µA/25 µA	no	7
NM93C46AL	MW	1K	128x8	2.0V/2.5V	400 µA/25 µA	no	7
NM93CS06/46/56/66L	MW	256–4K	16–256x16	2.0V/2.5V	400 µA/25 µA	yes	10
NM93C06/46/56/66LZ	MW	256–4K	16–256x16	2.0V/2.0V	400 µA/0.5 µA	no	10
NM93C46XLZ	MW	1K	64x16	1.8V/1.8V	400 µA/0.5 µA	no	10
The I2C Family has I2C Bi-directional I/O, 16 byte page-write mode. 8 pin DIP, 8/14 pin SO.							
NM24C02/4/8/16L	IIC	2K–16K	128–1Kx16	2.0V/3.0V	400 µA/25 µA	no	n/a
NM24C03/5/9/17L	IIC	2K–16K	128–1Kx16	2.0V/3.0V	400 µA/25 µA	yes	n/a

SuperI/O (Integrated Personal Computer I/O)

SINGLE CHIP PC I/O SOLUTION; LOW POWER; LOW VOLTAGE; 3.3V, 5V, OR MIXED 3.3V/5V OPERATION

The PC87332, PC87334, and PC87336 are single chip solutions for the most commonly used I/O peripherals in personal computers. They incorporate a floppy disk controller, two 16550 UARTs, and an IEEE 1284 parallel port. The PC87332 and 334 include an IDE interface. The PC87334 and 336 include an IrDA compliant infrared wireless interface. The PC87336 includes a Sharp IR mode and Plug 'n' Play features. All devices can operate at 3.3 Volts, all I/O pins are 5 Volt tolerant, have very low leakage current, and are reverse bias protected. These devices were designed for Notebook PC applications but have proved to be beneficial in Desktop PC and embedded applications as well.

Part Number	Package	FDC	UART	IR	Parallel Port	IDE	Plug 'n' Play	Bus	I_{CC} Standby	Notes
PC87332VLJ	100 PQFP	8477	2x16550		IEEE 1284	Yes	No	ISA	1 mA	Lit #113050
PC87334VLJ	100 PQFP	8477	2x16550	IrDA1	IEEE 1284	Yes	No	ISA	10 µA	Lit #113055
PC76334VJG	100 TQFP	8477	2x16550	IrDA1	IEEE 1284	Yes	No	ISA	10 µA	Lit #113055
PC87336VLJ	100 PQFP	8477	2x16550	IrDA + Sharp IR	IEEE 1284	No	Yes	ISA	10 µA	
PC87336VJG	100 TFQP	8477	2x16550	IrDA + Sharp IR	IEEE 1284	No	Yes	ISA	10 µA	

Data Transmission and Bus Interface

CMOS TIA/EIA DRIVER/RECEIVERS; LOW VOLTAGE; SINGLE 3.3V SUPPLY

National makes a wide assortment of other low-power, multi-voltage drivers and receivers for special applications.

- TIA/EIA- 232, 422, 422-A, 423, 485
- 3.3V single supply operation
- Lit #400042, Data Transmission Databook

Part Number	Type	Config.	Icc max/shutdown	Comments
DS14C335	232	3 x Tx 5 x Rx	20 mA/10 µA	**NEW**: Compatible with 5V UARTs; Only 4 external caps; 28p DIP/SSOP
DS14C561	562	4 x Tx 5 x Rx	6 mA/10 µA	**NEW**: Only 4 ext caps; 28p DIP; Lit #103310 datasheet

CMOS TIA/EIA DRIVER/RECEIVERS; LOW POWER; SINGLE 5V SUPPLY

National makes a wide assortment of other low-power, multi-voltage drivers and receivers for special applications.

- 5V single supply operation
- Industrial Temperatures
- Lit #400042, Data Transmission Databook

Part Number	Type	Config.	Icc max/ shutdown	tpd typ	Comments
DS14C232	232	2 x Tx 2 x Rx	3 mA/	na	CCIT V.28; Internal slew; Rx Noise filter; 16p DIP/SOIC; Comm/Indust.
DS14C241	232	4 x Tx 5 x Rx	10 mA/ 10 µA	0.6 us	Only 4 ext caps; 28p DIP; Comm/Indust.
DS14C535	232	**NEW**: Same as DS14C241 except 1 Rx active in Shutdown; Pin compatible with 3.3V DS14C335; 28p DIP/SSOP			
DS34C86	422	4 x Rx	0.5 mA	9 ns	IOL=48 mA; 4ns max skew; CMR= ±7V
DS89C386	422/CCIT	12 x Rx	1.5 mA	9 ns	
DS34C87	422	4 x Tx	0.5 mA	6 ns	IOL=48 mA; 3ns max skew; TRI-STATE™
DS89C387	422/CCIT	12 x Tx	1.5 mA	6 ns	
DS89C21	422/423	1 x Tx 1 x Rx	6 mA	30 ns	
DS36C278	485	1 x Tx 1 x Rx	500 µA	50 ns	Wide common mode, receiver open input fail-safe, less than 1/4 unit load (Typ)
DS36C279	485	1 x Tx 1 x Rx	500 µA/10 µA	50 ns	All above with sleep mode
DS36C280	485	1 x Tx 1 x Rx	500 µA	50 ns	278 with slew rate control to minimize EMI effects

CMOS LINE DRIVERS; LOW VOLT SUPPLY

- MM88C29—Single ended x 4; 3–15V supply
- MM88C30—Differential x 2; 3–15V supply

LVDS/SCI LINE DRIVER/RECEIVERS; ULTRA LOW POWER CMOS; 5V SUPPLY

These are the first of a new series of LVDS (Low Voltage Differential Signaling) devices designed to meet the high performance, low power requirements of the IEEE 1596.3 LVDS/SCI standard. Constant current outputs at ±350 mV swings; 400ps max skew; CMOS/TTL I/Os; Industrial; Replaces AT&T 41LF/G, Fujitsu MB571/0, 26LS31/2.

TTL/LVDS Translators for SCI

- Point-to-point, differential RS-422
- Meets IEEE 1596.3 and TIA/EIA PN 3357
- >77.7MHz (155Mbps) over 10m twp cable
- Only 1/8 power consumption of PECL
- Low Noise, Skew, EMI; 3.5KV ESD
- Easy interface to 3.3V systems
- Lit #400042, Data Transmission Databook
- Lit #550063-001, Pitch Pak

Part Number	Config.	Icc typ nl/fl	pwr typ	V, mV	tpd max	diff skew	c/c skew	Comments
DS90C031	quad TTL/LVDS	1.7 mA/ 15.4 mA	11 mW	±350 output	3.5 ns	400 ps max	1.8 ns max	**NEW**: 16p SO; Lit #103662 datasheet
DS90C032	quad LVDS/TTL	1.7 mA/ 15.4 mA	11 mW	±350 inputs	5 ns	600 ps max	6.0 ns max	**NEW**: 16p SO; Lit #103665 datasheet
DS90CX581	TTL/LVDS transceiver	28 mA/ 10 µA	1.2 W	290 mV	9.7 ns		350 ps	**NEW**: 8-bit 40 MHz rising; Lit #103720-001
DS90CX582	LVDS/TTL receiver	37 mA/ 10 µA	1.2 W	290 mV	9.7 ns		700 ps	**NEW**: 8-bit 40 MHz falling; Lit #103695-001
DS90CX561	TTL/LVDS transceiver	28 mA/ 10 µA	1.2 W	290 mV	9.7 ns		350 ps	**NEW**: 8-bit 40 MHz rising; Lit #103700-001
DS90CX562	LVDS/TTL receiver	37 mA/ 10 µA	1.2 W	290 mV	9.7 ns		700 ps	**NEW**: 8-bit 40 MHz rising; Lit #103680-001

X = R–"Rising Edge;" F–"Failling Edge"

PI-BUS TRANSCEIVER; BTL BICMOS; VERY LOW POWER; 5V SUPPLY

Designed to meet the Low Power PI-bus (Parallel Interface) needs of the military at about 1/4 the power of competing devices. Ideal for Avionics applications.

DS1776 - Octal Bidirectional Transceiver; 37 mA max Icc; Mil-Std-883C; Latched, open collector B outputs (2.5ns typ controlled ramp rates; 4ns typ noise immunity; 100 mA max I_{OL}); Tri-State A outputs with V_{OH} level control for Low Volt bus compatibility (20 mA max IOL); 28p DIP/CLCC/QFP; (Replaces Signetics 54F776).

I/O CONTROLLERS/PCMCIA MULTIFUNCTION INTERFACE

Refer to the PERIPHERAL CONTROL AND I/O PROCESSORS section for more low-power data transmission devices.

PCMCIA

PCMCIA CONFIGURABLE MULTIPLE FUNCTION INTERFACE CHIPS

PCM16C00VNG

Acts as a standard interface between the PCMCIA bus and the card-side local bus for I/O and memory PCMCIA cards. Supports two independent concurrent I/O functions on a PC Card. Can be configured to interface to any two (2) ISA compatible I/O functions. Chip also supports logic necessary to simplify interfacing to National's DP83902A ST-NIC Ethernet Controller as one of its functions.

- PCMCIA Bus Interface
- Compliant with multi-function extension to PCMCIA Standard 3.X
- Supports two concurrent I/O Functions and Memory
- 3.3 and 5.0V Operation
- Supports NSC ST-NIC Ethernet Controller on one port
- 144 pin TQFP
- Lit #113200-001 datasheet, AN-970, 975, 981 App Notes
- Design kit available for a LAN/Fax-modem multi-function PC Card (DP83903DAP) (Kit incorporates PCM160C00, DP83903A ST-NIC, and a V.34 modem)
- Can be ordered as part of a chip set DP83903CS which includes the ST-NIC Ethernet Controller and the PCM16C00

PCM16C00VNG	Interfaces two independent I/O functions and memory on a PC Card to the PCMCIA bus.

PCM16C02VJG

Acts as a standard interface between the PC Card Host bus and local buses found on I/O and memory PC Cards. Provides a PC Card interface for any two (2) generic ISA like functions on a PC Card. In addition provides the capability to configure function 0 as a NAND Flash interface, supporting all of the necessary control signals required to handshake with NAND Flash (NM2916) memory devices.

- PC Card Bus Interface
- Compliant with multi-function extension to PCMCIA Standard 3.X
- Supports two concurrent I/O functions plus memory
- 3.3 and 5.0V Operation
- Supports NAND Flash Interface
- 100 pin TQFP
- Lit #113202-001 datasheet, AN-975, 976, 980, 981 App Notes

PCM16C02VJG	Interfaces two independent I/O functions and memory on a PC Card to the PCMCIA bus.

COP800 Basic Family

8-BIT MICROCONTROLLERS; LOW POWER; LOW VOLT OR 5V SUPPLY

Memory mapped core architecture; 70% of multiple-function instructions are Low Power; Low single-cycle (1us)/single-byte; 4 MHz at 2.5V; 16 bit timer/counter with input Volt or 5V Supply capture register; Watchdog; illegal condition detect; MICROWIRE/PLUS serial I/O; Software program I/Os; High current outputs; Industrial (8xx), Commercial (9xx), Military (6xx, 5V only); DIP/SO; Development tools available.

Features

- 2.3-6.0V operation
- Very low power
- HALT/IDLE modes
- Multi-Input Wake Up
- 4 MHz at 2.3V
- Watch Dog
- Full OTP Support (2.7-5.5V)
- Lit #400007-001, COP8 Databook

Part Number	ROM	RAM	I/O	Timers	Interrupts	W/D	OTP
823CJ	1k	64	11	1	3	yes	
822CJ	1k	64	15	1	3	yes	87L22CJ
820CJ	1k	64	23	1	3	yes	87L20CJ
842CJ	2k	128	15	1	3	yes	87L42CJ
840CJ	2k	128	23	1	3	yes	87L40CJ
822C	1k	64	15	1	3	no	8782C
820C	1k	64	23	1	3	no	8781C+
842C	2k	128	15	1	3	no	8782C
840C	2k	128	23	1	3	no	8781C+
881C	4k	128	23	1	3	no	8781C+
880C	4k	128	35	1	3	no	8780C

COP800 Feature Family

8-BIT MICROCONTROLLERS; LOW POWER; LOW VOLTAGE

The COP8 family of 8-bit microcontrollers uses an single chip core architecture. All of the members of this expandable 8-bit microcontroller family include MICROWIRE/PLUS serial communications, 77% of instructions are single-cycle/single byte, software programmable I/O, and high current I/O. All devices are supported with OTP and masked ROM, with user friendly development tools from Metalink.

Features

- 2.3–6.0V operation (masked ROM)
- Full OTP Support (2.7–5.5V)
- No power mode (0.8 µW)
- Multi-Input Wake Up
- Lit #400007-001, COP8 databook
  Lit #630006-002, COP8 Selection Guide
- Watch Dog

Part Number	ROM	RAM	Pins	Timers	Interrupts	Comparators	A/D	UART	OTP
885BC	2K	64	20	1	12	2			
884BC	2K	64	28	1	12	2			87L84BC+
884GD	16K	256	28	3	12		YES		87L84GD+
888GD	16K	256	40/44	3	12		YES		87L88GD+
884CF	4K	128	28	2	10		YES		87L84CF
888CF	4K	128	40/44	2	10		YES		87L88CF
884CG	4K	192	28	3	14	2		1	87L84EG
888CG	4K	192	40/44	3	14	2		1	87L88EG
884EG	8K	256	28	3	14	2		1	87L84EG
888EG	8K	256	40/44	3	14	2		1	87L88EG
888GG	16K	512	40/44	3	14	2		1	87L88GG+
888HG	20K	512	40/44	3	14	2		1	87L88HG+
884EK	8K	256	28	3	12	1	YES		87L84EK
888EK	8K	256	40/44	3	12	1	YES		87L88EK
884CL	4K	128	28	2	10				87L84CL
888CL	4K	128	40/44	2	10				87L88CL
884CS	4K	192	28	1	12	1		1	87L84EG
888CS	4K	192	40/44	1	12	1		1	87L88EG
888GW	16K	512	68	2	14			1	87L88GW+

Data Acquisition

12 BIT SERIAL I/O A/D CONVERTERS; LOW VOLT SUPPLY; LOW POWER

ADC12L03x Family

- 12-bit plus sign
- 3–3.6V supply with Standby modes
- Self calibrating
- MICROWIRE and SPI serial interface
- Configurable/2/4/8 differential or Single-Ended mux
- Sample/Hold
- Use LM4040/4041/9140 voltage references
- Sample kit #570085
- 5V versions available
- Lit #400033, Data Acquisition Databook

Part Number	Sample	13 bit conv.	Supply	Pwr/Stby	Comments
ADC12L030/2/4/8	73 kHz max	8.8 us max	3–3.6V	15 mW max/ 40 uW	± 1 LSB max linearity error; /2/4/8 channel configuration; Lit #101070-004

16 BIT A/D CONVERTER; 5V SUPPLY; LOW POWER

DELTA-SIGMA Converters

- Ultra-fast 192 kHz output data rate
- Single 5V supply
- Internal voltage reference (ADC16471)
- Power down modes
- 24p PDIP/SOIC
- Lit #400033, Data Acquisition Databook

Part Number	Type	Sample	Supply	Pwr/Stby	Comments
ADC16071/16471	Delta-Sigma	192 kHz	5V	Very Low	No external volt reference required for ADC16471; Lit #101095-002

DATA ACQUISITION SYSTEMS (DAS); 3V OR 5 VOLT; LOW POWER

These low-power, true Systems-on-a-Chip offer: A/D and Watchdog operation; Zero-glue-logic interfaces; Sample/hold; Programmable acq. times and conversion rates; User programmable sequencer; Timer, Internal 8 word RAM and 32x16 FIFO; 13 bit 7.3 us max conversion time (9 bit = 3.5 us); ±1 LSB linearity error; (5V versions also available).

DAS-on-a-Chip

- 8/12-bit plus sign ADC, and Watchdog
- Self calibrating and diagnostic mode
- 3.0–3.6V single supply with Standby mode
- CMOS compatible Serial or Parallel I/O
- Fully Programmable
- 13 bit, 7.3us max conversion time
- Lit #400033, Data Acquisition Databook

Part Number	External Bus	Sample	Supply	Pwr/Stby Max	Comments
LM12L454/458	8/16 bit parallel	106kS/s	3.0–6V	15 mW/5 uW	Configurable 4/8 mux; High-speed DMA; 44p PLCC; Lit #570032, #108350-001
LM12L434/438	6MHz serial; Selectable protocols	105kS/s	3.0–6V	20 mW/16 uW	MICROWIRE/PLUS, SPI/QSPI, TMS320, I^2C, 8051, SCI protocols; 28p PLCC/SO; Lit #108315-001

TEMPERATURE SENSORS

SOT-23 Centigrade Temperature Sensor

- Output scale factor of ±10 mV/°C
- No external calibration signal conditioning, or linearization
- Ultra-small, TinyPak™ packaging
- –40 to +125°C
- 4.5–10V single-supply; 130 µA max
- Guaranteed accuracy
- Lit #106485-001 datasheet

Part Number	Temp	Accuracy	Supply	Pwr	Comments
LM50	–4/+125°C	±2C @ 25°C	4.5–10V	130 µA max	**NEW**: 3p SOT23; Lit #106485-001

Wireless Communication; AM; FM

PLL FREQUENCY SYNTHESIZERS; LOW POWER; WIDE VOLTAGE SUPPLY

The PLLatinum™ Family of frequency synthesizers for personal communication applications to 2.5 GHz. Low power consumption, very low noise, small surface-mount package sizes, and up to 15 times faster "lock time" performance than competing devices.

PLLatinum Series

- 2.7–5.5V operation
- Very low power; Power-down mode
- Very low noise
- DECT, AMPS, ETACS, CT-1/CT-1+, CATV, CT2, ISM, GSM, IS-54/95, RCR27/28, NMT WLAN, DCS1800 Applications
- Lit #550240-003, Selection Guide

Part Number	Type	Freq	Icc	I_{CC} pwrdn	Ido TRI-STATE	Prescaler	Package	Notes
LMX1501A/ LMX1511	RF single	1.1 GHz	6 mA		5 nA @ 25C	64/65, 128/129	16p SO, 20p TSSOP	AMPS; NMT; CT2; CT1; I SM; ETACS; Lit #108500-002
LMX2301	RF single	160 MHz	2 mA		5 n @ 25C		20p TSSOP	
LMX2305	RF single	550 MHz	3 mA		5 n @ 25C	64/65, 128/129	20p TSSOP	
LMX2315	RF single	1.2 GHz	6 mA	30 µA	2.5 nA @85C	64/65, 128/129	20p TSSOP	GSM; IS-54/95; RCR27; ISM; Lit #108530-002
LMX2320/ LMX2325	RF single	2.0 GHz/ 2.5 GHz	10/11 mA	30 µA	2.5 nA @85C	64/65, 128/129 32/33, 64/65	20p TSSOP	DECT; DCS1800; Lit #108535-002
LMX2330A	RF/IF dual	2.5 GHz/ 510 MHz	13 mA	1 µA	2.5 nA @85C	32/33, 64/65 8/9, 16/17	20p TSSOP	ISM; DECT; CATV; WLAN; Lit #108545-002
LMX2331A	RF/IF dual	2.0 GHz/ 510 MHz	12 mA	1 µA	2.5 nA @85C	64/65, 128/129 8/9, 16/17	20p TSSOP	DECT; DCS1800; RCR28; RCR27; Lit #108545-002
LMX2332A	RF/IF dual	1.2 GHz/ 510 MHz	8 mA	1 µA	2.5 nA @85C	64/65, 128/129 8/9, 16/17	20p TSSOP	GSM; IS-54/95; RCR-27; ISM; Lit #108545-002
LMX2335	RF/RF dual	1.1 GHz/ 1.1 GHz	9 mA	1 µA	5 nA @ 25C	64/65, 128/129	16p SO	AMPS; NMT; ISM; CT2; CT1; ETACS; Lit #108548-001
LMX2336	RF/RF Dual	2.0 GHz/ 1.1 GHz	13 mA	1 µA	5 nA @ 25C	64/65, 128/129	TSSOP 20	CATV Dual Mode PLS; Lit #108548-001
LMX2337	IF/IF Dual	550 MHz 550 MHz	9 mA	1 µA	(Typ) 5 nA @ 25C	64/65, 128/129	SO16-JEDEC	1/2 Freq; ISM; AMPS; NMT 45; Lit #108548-001

DIGITAL CORDLESS INTEGRATED CHIP-SET; LOW POWER BICMOS; LOW VOLT SUPPLY

Wireless applications include: WPBX; Cordless phones; WLANs; Radio local loop.

SiRF (Silicon Radio Frequency) Family

- Designed for 1.9GHz pan-European DECT standard
- 3V operation
- Four surface mount devices
- Complete DECT™ reference design available

Part Number	Comments
LMX2216	Low noise amplifier/mixer; See next page for details
LMX2240	IF demodulator; See next page for details
LMX2320/LMX2315	PLL frequency synthesizer; See above for details
LMX2411	Baseband processor; See next page for details

LOW NOISE AMPLIFIER/MIXER; LOW VOLT SUPPLY; LOW POWER

LMX2216

- Wideband operation 0.1–2.0 GHz
- 2.7–3.6V supply
- Low Power
- Power down feature
- Double balanced Gilbert cell mixer
- LNA I/O ports at 50 ohms
- Mixer input at 50 ohms/Output at 200 ohms
- No biasing or matching components needed
- 16p SO
- Lit #108516-002

Part Number	Freq	Supply	Comments
LMX2216	0.1–2.0 GHz	2.7–3.6V	16p SO; Part of DECT chip-set

IF DEMODULATOR; LOW VOLT SUPPLY; LOW POWER

RF sensitivity to –75 dBm; RSSI sensitivity to -82dB; 70 dB limiter gain; 480 µA Icc avg for DECT burst mode; Demodulator operates to 150 MHz; Use with LMX2216, LMX2315/20, and LMX2411 for complete receiver solution.

LMX2240

- 2.7–3.6V supply
- Low Power
- 40–150 MHz operation
- 70 dB limiter gain
- Power down mode
- Lit #108540-002

Part Number	Freq	Supply	Comments
LMX2240	10–150 MHz	2.7–3.6V	16p SO; Part of DECT chip-set

BASE BAND PROCESSOR; LOW POWER; LOW VOLT SUPPLY

2.5 mA transmit; 5 mA receive; Total: (0.6 mA avg in burst mode); Integrated voltage comparator; High-speed data slicer and DC compensation circuit; Gaussian filter ROM-DAC for transmit; VCO modulation; Compatible with Sitel SC14401/20 DECT Burst Mode Controllers.

LMX2411

- 2.85–3.6V supply
- Power down feature
- 1 Kb/s–1.2 Mb/s Transmit/Receive
- Integrated Data Comparator
- 10/13/18 MHz system clocks
- Lit #108550-001

Part Number	Supply	Tx/Rx	Tx Current	Rx Current	Comments
LMX2411	2.7–3.6V	1 Kb/s–1.2Mb/s	3.5 mA Total 0.6 mA burst mode	6 mA	Data comparator; 16p SOIC; Part of DECT chip-set

1.9 GHZ POWER AMPLIFIER; LOW VOLTAGE SUPPLY; HIGH EFFICIENCY

450 mW, Class A amplifier; >30% power added efficiency (3.6V V_{CC} +2 dBm input); single +3V supply, no external negative bias required; eliminates >30 components relative to discrete design; 50Ω input and output impedance; 16-pin SOIC package.

Part Number	Supply	Frequency	Efficiency	Comments
LMX2119M	2.8–4.8V	1.88–1.9 GHz	>30%	No negative bias; 16p SOIC; Part of DECT chip-set

Section 14

LCX Designer's Guide

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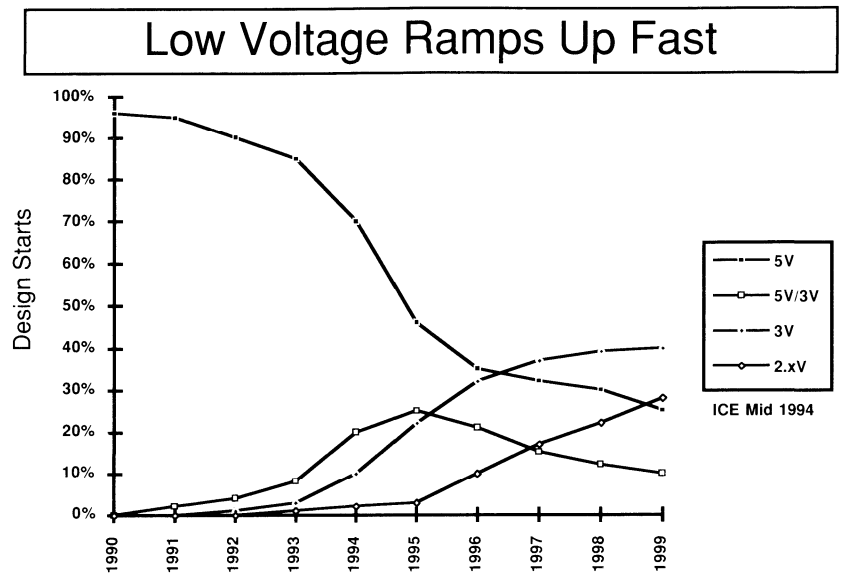
Chapter 1
Introduction

This is an introduction to National Semiconductor's advanced **L**ow Voltage (3V) **C**MOS logic product family with Translation (**X**) called LCX.

The LCX family is the most user-friendly 3-volt CMOS logic product family available today. LCX is fabricated on National's advanced 0.8µm CMOS process. The 5 volt tolerant inputs and outputs make the LCX family the logical choice for mixed voltage (3V/5V) systems as well as for pure 3V systems. National's new LCX series products will complement your system design with substantial power reduction, low noise performance, overvoltage protection, power up/down high impedance, as well as improved ESD protection and latch-up characteristics.



Market research firms predict rapid growth of sub 5V systems. During the next several years we should see a decline in percentage of 5V-only systems, a transition period of mixed 3V/5V systems, and the growth of 3V and sub-3V systems. LCX is well-suited to this era of changes, since LCX can interface to 5V devices and can also be powered from supply voltages down to 2.0V.

3V Adoption: Drivers and Barriers

- **Drivers**
  - Lower Power Consumption (save power up to 60%)
    - * Longer battery life
    - * Less heat
      - – Higher reliability
      - – Smaller power supplies, fans = lower cost, less weight, more compact packaging
  - Reduced Noise
    - * Lower EMI, crosstalk, ground bounce, etc.
  - Smaller Process Geometries (<0.5u)
    - * Higher intergration, yield
    - * More performance
- **Barriers**
  - Interfacing to 5V Signals
    - * LCX interfaces directly to 5V devices
  - Price and Availability
    - * LCX is price competitive with 5V families
    - * LCX is available from 4 major suppliers

There are many reasons for moving to a 3V supply, including dramatic power savings, lower noise due to reduced output swings, and the ability to use advanced sub-0.5μ process geometries.

As with anything new, there are always concerns over compatibility with existing technologies as well as cost and availability of the new technology.

LCX was created with these issues in mind: provide a cost effective 5V tolerant family available from an alliance of major logic suppliers.

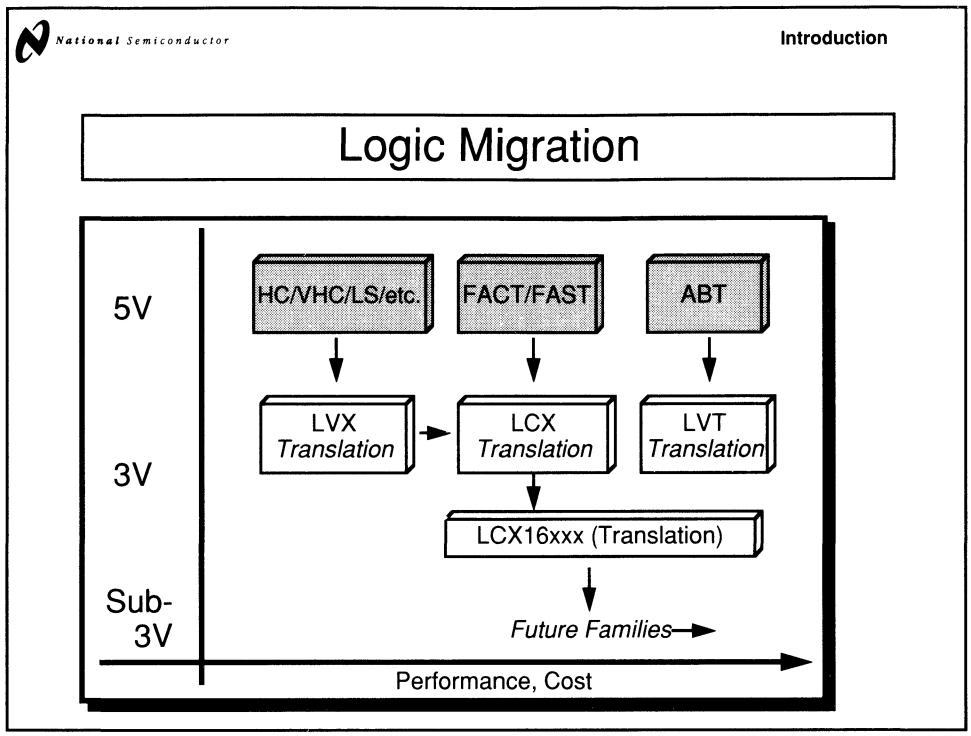
CROSSVOLT™ (krôs'vōlt) ***adj.***

[cross+voltage] providing translation (not frustration) between different digital signal levels (e.g. 5V to 3.3V translation) in order to ease the migration from one signal level to another

National Semiconductor's LCX High Speed CMOS Low Voltage Logic Family is a member of National's *CROSSVOLT*™ Low Voltage Logic Series which provides low voltage logic families and specialized translators for low supply voltage and mixed supply voltage applications. Currently this means most of our 3.3V logic, while designed for 3.3V operation, will interface to 5V signals.

By offering this 5V tolerance feature at no extra cost, National's *CROSSVOLT* logic allows system designers the flexibility to choose either 3.3V or 5V system components based on performance, price, availability, etc. This shortens time to market, allows the use of components with the latest features, and removes single supply cost/availability constraints, so that you can provide your customers high value systems quickly and at a low cost.

As supply voltages drop and new signalling technologies are adopted, National's *CROSSVOLT* series of products will continue to provide translation to help you move quickly into the future.



Despite having an abundance of families with three letter acronyms beginning with the letter "L," the 3V logic market is really not that complicated. When choosing a *CROSSVOLT* logic family, the customer has three main performance choices: low cost (LVX), high performance (LCX), and high speed/drive (LVT). These correspond very well to the 5V families listed below each family. (Exception: LCX 16-bit products are much faster than the octals, with speeds (4.5ns) approaching LVT/ABT speeds) In addition to these generic logic families, two specialty translator families, dual supply translators and bus switches also exist.

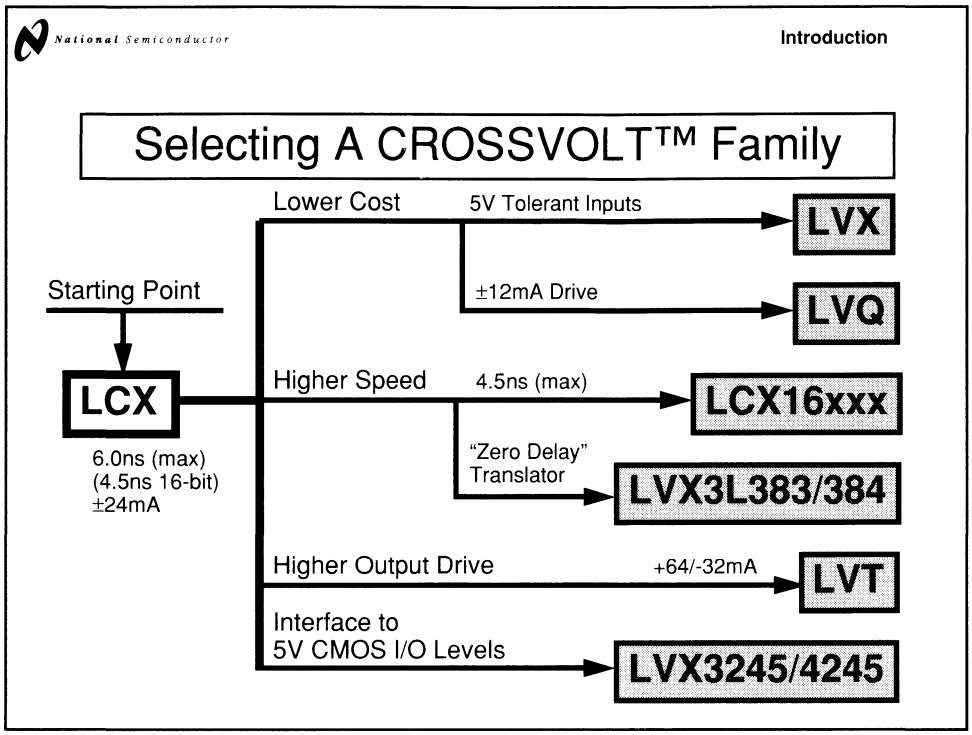
The important thing to note is that National, consistent with its *CROSSVOLT* philosophy, provides translation capability across the performance spectrum, while our competitors do not. Ask yourself whether you will ever possibly interface to a 5V signal with 3V logic. The answer is probably "yes." With National's *CROSSVOLT* logic series you can have a 5V tolerant 3V logic family that gives you the best combination of price/performance.

Selection By Application

	General Purpose	High Performance	Backplane Driving	Special Translation
LV Family	LVX	LCX	LVT	LVX3L384 & LVX4245
5V Equiv.	HC/VHC	AC/ACQ/FAST	ABT	None
Functions	Full Family	Full Family	Bus Functions	Translating Bus
Process	CMOS	CMOS	BiCMOS	Varies
t_{PD} (max)	11.5ns	6.5ns/4.5ns	4ns	Varies
Drive	±4mA	±24mA	+64/-32mA	Varies
Competitive Solution	LV	LVC/ALVC	LVT	Quickswitch FCT164245
Price (Normalized)	1	1.5	2	2

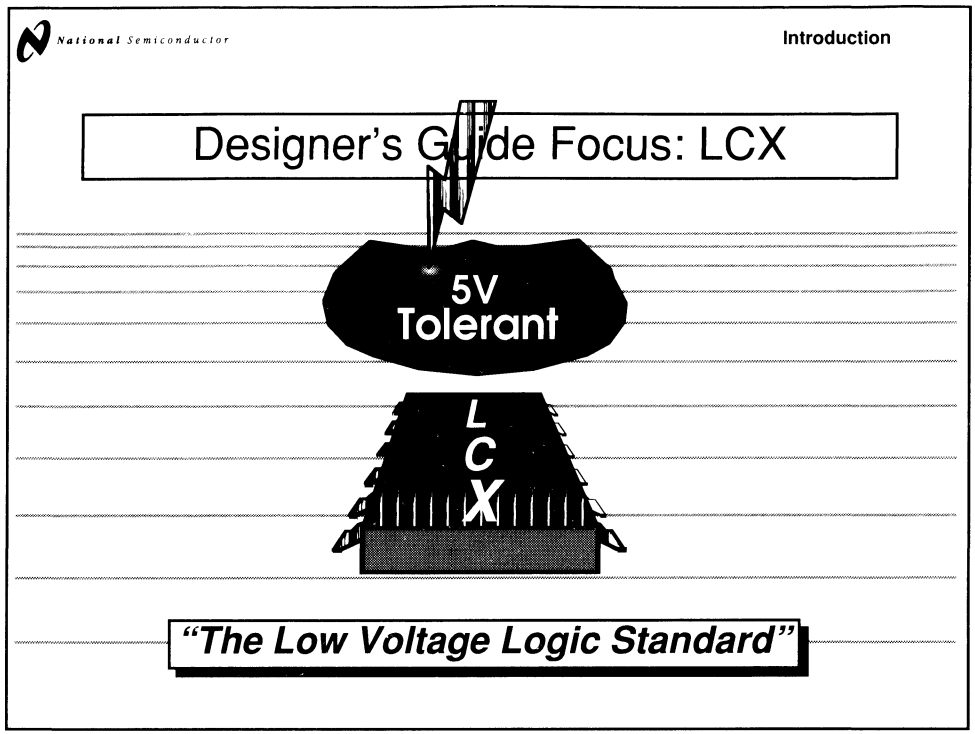
Data reflects '245 octal transceiver

Here is another way to choose a *CROSSVOLT* low voltage logic family. This table shows three general-purpose families (LCX, LVX, and LVT) and two special-purpose translator families (LVX bus switches and LVX dual supply translators).



LCX is well suited for a very broad number of applications. In fact it is probably the most versatile 3V logic family. Sometimes, however, another *CROSSVOLT* family is more appropriate for a given application. In this situation use the chart shown above to chose an alternate family. If you would like a lower cost, lower performance family, then choose LVX or LVQ. LVX has 5V tolerant inputs, while LVQ has ±12mA output drive. If more drive is needed, then choose LVT.

If a special purpose translator is needed, then you may want to use a dual supply translator or a bus switch. When interfacing to digital IC's which require a 5V CMOS rail-to-rail swing, then a dual supply translator is the best choice. For "zero delay" (250ps) translation, then you may want to use our low power bus switches.



LCX High-Speed CMOS Low Voltage Logic Family is National Semiconductor's flagship 3.3V logic family, and the remainder of this designer's guide is devoted to LCX.

We believe LCX will become the de facto standard 3.3V logic family because it offers the best combination of high speed (4.5ns max for 16-bitters), very low power consumption (less than 10μA max for octals), and is available from multiple sources in multiple packages. In addition, LCX has 5V tolerant inputs and outputs which allows LCX to not only talk to 3V devices, but 5V devices as well thereby easing the migration from 5V to 3V systems. LCX also has power-down high impedance capability which is useful in power managed applications.

Historical Overview

- National, Motorola and Toshiba join forces to establish the new 3.3V logic world standard with common datasheet specifications
- LCX partnership announcement in 1993: National, Motorola, and Toshiba, the Low Voltage Logic Alliance
- LCX family introduced in 1994
- February 1995, SGS-Thompson joins the LCX standard
- Joint National, Motorola, and Toshiba LCX ad runs April 1995
- Future joint product development and promotion continue

In 1993 the need for a new specially designed 3.3V logic family was clear. It was also recognized that the world needed logic standards, not a proliferation of logic families. From these ideas, the Low Voltage Logic Alliance and LCX were born. In February 1995, based on customer input, SGS-Thompson joined the LCX standard. Together National, Motorola, Toshiba, and SGS-Thompson serve most of the CMOS logic market. And, as LCX becomes the world standard, the partners are actively at work on future logic standards.

LCX Features

- Optimized for 3V operation
- 3V/5V Translation
- Low Power Consumption
- High Performance
- Power-Up/Down High Impedance
- Extended Operating Voltage
- ±24 mA Balanced Output Drive
- Proprietary Noise-Control Circuitry
- Alternate Sources

5V tolerant inputs and outputs allow LCX to interface to 5V, as well as 3V, system components.

LCX has almost zero quiescent power dissipation and the lowest dynamic power for '245 devices.

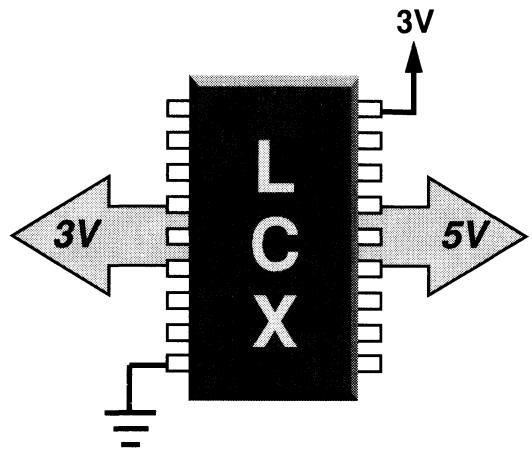
Power down high impedance enables LCX as an ideal product family used in power management and live insertion applications.

Extended operating voltage range (2.0-3.6V) provides operation even in unregulated battery systems.

National's proprietary noise control circuitry effectively reduce noises such as ground bounce, system undershoot/overshoot, and EMI.

There are currently four major LCX suppliers: National Semiconductor, Motorola, Toshiba, and SGS-Thomson.

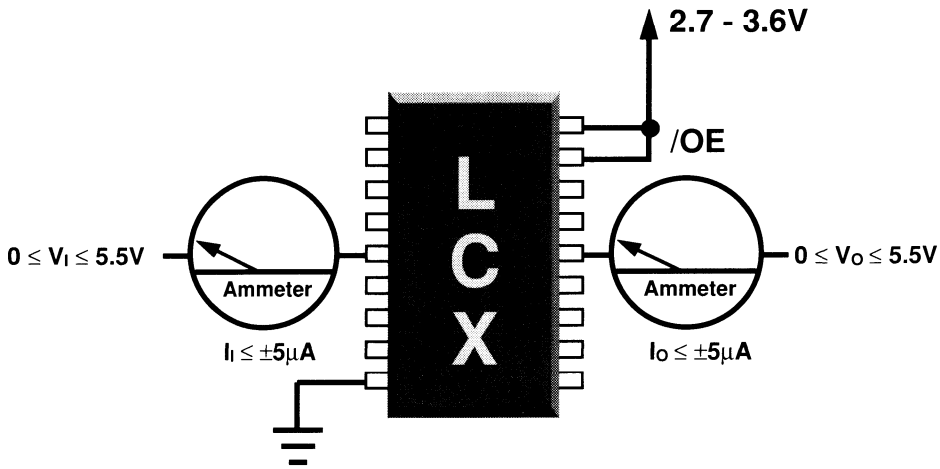
3V/5V Translation



One of the benefits of any overvoltage tolerance is birdirectional 3V/5V translation. LCX devices will tolerate 5V signals on inputs, control pins, I/O pins configured as inputs, and TRI-STATE® outputs. In other words, all signal pins are 5V tolerant, though outputs and I/O pins should be TRI-STATE in the face of 5V signals to avoid (bus) contention.

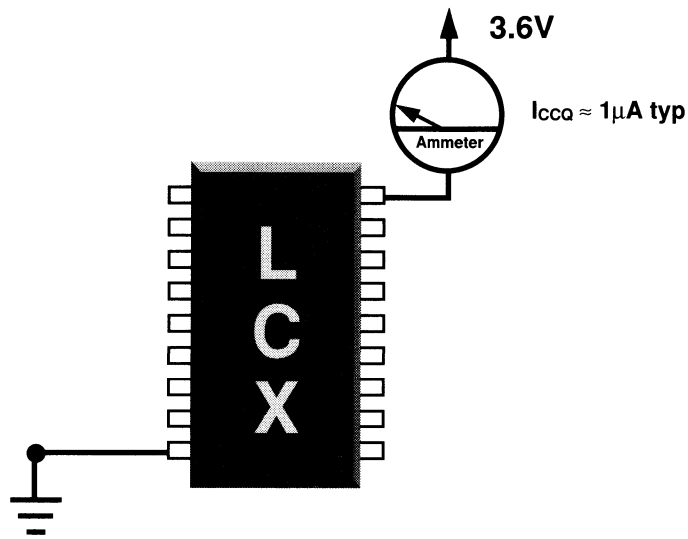
See Chapter 2 for more information about translation.

Overvoltage Tolerance Leakage



Input and TRI-STATE outputs or I/O leakage is specified to be less than ±5μA. This very small leakage specification assures the system designer that interfacing LCX devices to 5V devices is safe and does not degrade system performance or signal fidelity.

Low Power Consumption

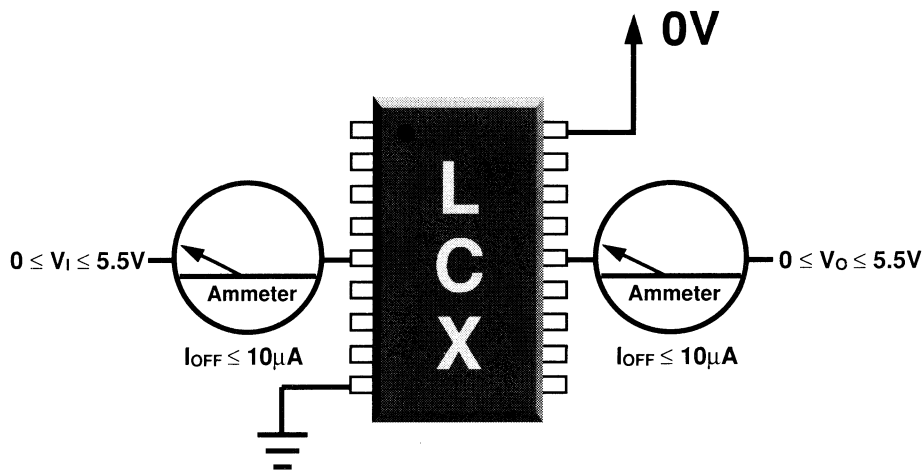


Since the LCX family is pure CMOS it has near zero static power consumption, giving LCX possibly the lowest I_{CCQ} in the industry.

The LCX family's extremely low power consumption and high speed make LCX perfect for all portable applications.

In addition to low quiescent power consumption, the LCX family also features extremely low dynamic power consumption (see dynamic I_{CC} graphs in Chapter 4) for low active system power consumption.

Power Down Overvoltage Protection

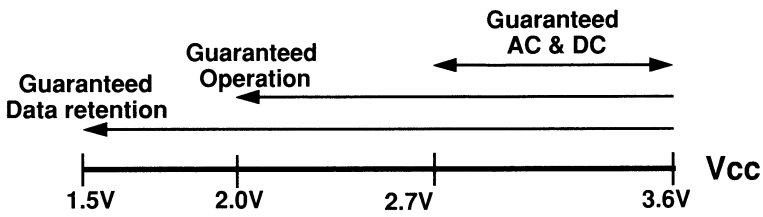


When an LCX device is powered down, that is when Vcc is at 0V, the power off Input/Output leakage current (I_{OFF}) is guaranteed to be less than 10uA for voltages from 0V to 5.5V applied on any input or output pin.

This means LCX can be used in power managed and live insertion applications. For instance, LCX devices can be powered down along with other devices in power managed applications. While powered down, however, LCX devices can interface safely with active devices. In fact, LCX devices can be used to isolate the active portions of the system from powered down portions of the system.

See Chapter 3 for more information about power up/down high impedance.

Extended V_{CC} Range



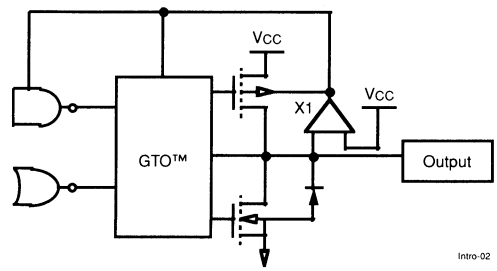
There are three (3) V_{CC} ranges specified. The first specified V_{CC} range 2.7–3.6V is where the AC and DC spec limits are guaranteed. It is compatible with extended JEDEC standard No. 8-1B and is fully characterized for unregulated battery operation. The second specified V_{CC} range, 2.0–2.7V is the lowest limit of device operation but where the AC and DC spec limits are not specified. The third V_{CC} limit, 1.5V is the lower limit where data will be retained, but operation is not guaranteed.

Although designed for low voltage operation, currently National's LCX family can be used at 5V V_{CC}. Some customers are using LCX devices at 5V to achieve very high speeds. Note that at 5V, LCX devices will exhibit more noise and inputs will be full-swing CMOS level (not TTL level) compatible. Some characterization of LCX devices at V_{CC} = 5V is available from National.

Note: Other vendors' LCX devices may not be recommended for 5V supply operation.

LCX Noise Control Circuitry

- **National's patented Graduated Turn-On (GTO™) noise control circuitry**



Typical LCX output circuitry - simplified

The LCX noise control circuitry is National's patented and proven Graduated Turn-On noise control circuitry used in our FACT Quiet Series logic family. This circuitry reduces the ground bounce of the device. The ground bounce of a quiet output is specified as V_{OLP} and V_{OLV}. V_{OLP} is the typical maximum VOL peak value and V_{OLV} is the typical minimum V_{OL} valley value. The LCX devices typically generate less than 800mV of ground bounce with V_{CC} = 3.3 at 25°C into a 50 pF/500Ω load.

The GTO circuitry accomplishes this by "rounding" output transition edges. This not only reduces ground bounce, but can also dramatically reduce system undershoot, overshoot, and EMI as shown in Chapters 6 and 7.

Alternate Sources

- Also sourced by
  - MOTOROLA
  - TOSHIBA
  - SGS-THOMSON

The LCX family is also sourced by three (3) other suppliers, Motorola, Toshiba, and SGS-Thomson.

Together National, Motorola, Toshiba, and SGS-Thomson service over 50% of the CMOS logic market. It seems clear from customer input that LCX will be the de facto standard 3.3V logic family.

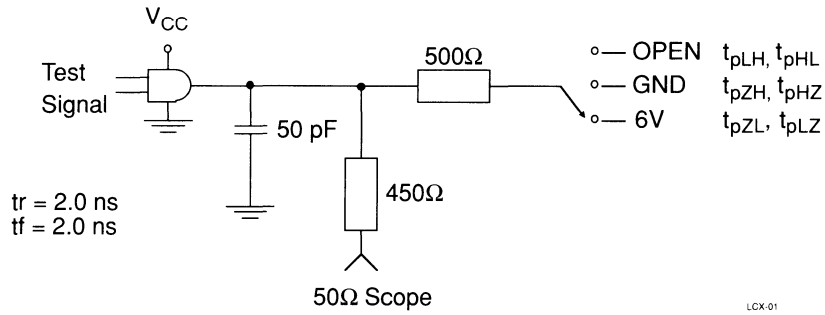
Performance Specifications

LCX Specification Conditions

- Three supply voltage ranges
  - 2.7 to 3.6V guaranteed AC/DC electrical characteristics
  - Guaranteed operation on down to 2.0V
  - Guaranteed data retention only—down to 1.5V
- Temperature range -40˚C to +85˚C
- AC propagation delays with standard 50pF and 500Ω load

LCX is specified with guaranteed limits at 3 supply voltage ranges. Ambient temperature range is specified from -40°C to +85°C which covers both commercial and industrial ranges.

AC Loading Test Circuit



- Switch is normally open for most circuits but is closed to establish a quiescent high level for testing tri-state enable and disable circuits

This is a schematic diagram of the standard test fixture AC load circuit used for testing the LCX series.

(More information on test procedures and conditions may be found in the *CROSSVOLT*™ Low Voltage Logic Series Databook.)

This is also the standard test fixture used by most logic families for many years.

LCX Input Specifications

–40°C Thru 85°C Guaranteed Values

	Parameter	V_{CC}	Limit	Conditions
V_{IH}	Input Voltage High	2.7–3.6V	≥ 2.0V	
V_{IL}	Input Voltage Low	2.7–3.6V	≤ 0.8V	
I_I	Input Leakage Current	2.7–3.6V	≤ ±5μA	$0 \le V_I < 5.5V$
C_{IN}	Input Capacitance	0V	Typical, 7 pF	V_I = 0V or V_{CC}
I_{OFF}	Power Off Leakage Current	0V	≤ 10 μA	V_I = 5.5V

These are the guaranteed LCX input specifications.

LCX Output Specifications

–40°C Thru 85°C Guaranteed Values

	Parameter	V_{CC}	Limit	Conditions
V_{OH}	Output Voltage High	2.7–3.6V	≥ VCC -0.2	I_{OH} = -100 µA
		2.7V	≥ 2.2V	I_{OH} = -12 mA
		3.0V	≥ 2.4V	-18 mA
		3.0V	≥ 2.2V	-24 mA
V_{OL}	Output Voltage Low	2.7–3.6V	≤ .2V	I_{OL} = 100 µA
		2.7V	≤ .4V	I_{OL} = 12 mA
		3.0V	≤ .55V	24 mA
I_{OZ}	Output Leakage Current TRI-STATE	2.7–3.6V	≤ ±5µA	$0 \le V_O < 5.5V$ $V_I = V_{IH}$ or V_{IL}
C_{OUT}	Output Capacitance	3.3V	Typical, 8 pF	V_O = 0V or V_{CC}
I_{OFF}	Power Off Leakage Current	0V	≤ 10 µA	V_O = 5.5V

V_{OH} and V_{OL} are specified from 2.7–3.6V V_{CC}. From 3.0 to 3.6V we guarantee ±24 mA static drive and ±12 mA drive is guaranteed with a supply voltage at 2.7V.

±24mA drive capability makes LCX suitable for most applications.

LCX Capacitance Information

Symbol	Parameter	LCX Typ	Units	Conditions
C_{IN}	Input Capacitance	7	pF	V_{CC} = Open V_I = 0V or V_{CC}
$C_{I/O}$	Input/Output Capacitance	8	pF	V_{CC} = 3.3V V_I = 0V or V_{CC}
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 3.3V V_I = 0V or V_{CC} F = 10 MHz

Here are typical input and power dissipation capacitances for LCX that may be used in generic power calculations.

LCX DC Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = -40°C to + 85°C		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7–3.6	2.0		V	
V_{IL}	Low Level Input Voltage	2.7–3.6		0.8	V	
V_{OH}	High Level Output Voltage	2.7–3.6 2.7 3.0 3.0	V_{CC} – 0.2 2.2 2.4 2.2		V	I_{OH} = -100 µA I_{OH} = -12 mA I_{OH} = -18 mA I_{OH} = -24 mA
V_{OL}	Low Level Output Voltage	2.7–3.6 2.7 3.0 3.0		0.2 0.4 0.55 0.4	V	I_{OL} = 100 µA I_{OL} = 12 mA I_{OL} = 24 mA I_{OL} = 16 mA
I_I	Input Leakage Current	2.7–3.6		±5.0	µA	$0 \le V_I \le 5.5V$
I_{OZ}	TRI-STATE Output or I/O Leakage Current	2.7–3.6		±5.0	µA	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}
I_{OFF}	Power Off Leakage Current	0		10	µA	V_I or V_O = 5.5V
I_{CC}	Quies. Supply Current (LCX245)	2.7–3.6		10	µA	$V_I = V_{CC}$ or GND
				±10	µA	$3.6 \le (V_I$ or $V_O) \le 5.5V$
ΔI_{CC}	Increase in I_{CC} per Input	2.7–3.6		500	µA	$V_{IH} = V_{CC}$ - 0.6V

This is direct reproduction of the LCX DC characteristics as published in the data book and applies generically for all LCX devices.

Note that all the DC characteristics are guaranteed at 2.7V–3.6V V_{CC} and across the full temperature range -40°C to +85°C.

LCX245 AC Electrical Characteristics

Symbol	Parameter	T_A = -40°C to + 85°C				Units
		V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V		
		Max	Min	Max	Min	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Here is an example of a typical octal (LCX245) AC data sheet.

LCX16245 AC Electrical Characteristics

Symbol	Parameter	T_A = -40°C to + 85°C				Units
		V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V		
		Max	Min	Max	Min	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	6.4 6.4	1.5 1.5	6.9 6.9	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Here is an example of a typical 16-bit (LCX16245) data sheet worst case AC performance figures.

Product Portfolio

LCX Portfolio

- 38 key products (some are in development)
  - Including:16-Bitters, Octals, Gates, and MSIs
- Various package choices are available
  - 16-Bitters: EIAJ SSOP and JEDEC TSSOP
  - Octals: SOIC (JEDEC & EIAJ), JEDEC TSSOP, and EIAJ SSOPII
  - Gates: SOIC (JEDEC & EIAJ) and JEDEC TSSOP
- Other new LCX functions based on customer interest

The ever-expanding LCX family currently include gates, MSI, octals, and 16-bitters.

New functions are in development, so contact your local National Semiconductor representative for a current list of LCX products.

LCX Portfolio (continued)

Octals	16-Bit	Function/Description
74LCX240	74LCX16240	Inverting Buffer/Line Driver
74LCX244	74LCX16244	Buffer/Line Driver
74LCX245	74LCX16245	Bidirectional Transceiver
74LCX373	74LCX16373	Transparent D-Latch
74LCX374	74LCX16374	D Flip-Flop
74LCX540		Buffer/Line Driver (Inverting with flow-through pinout)
74LCX541		Buffer/Line Driver (Non-Inverting with flow-through)
74LCX543	74LCX16543	Registered Transceiver
74LCX573		Transparent D-Latch (Flow-Through pinout)
74LCX574		Transparent D-Latch with Edge Trigger
74LCX646	74LCX16646	Transceiver/Register
74LCX652	74LCX16652	Transceiver/Register with Dual Enable
	18-Bit	
	74LCX16500	18-Bit Universal Bus Transceivers

This is a list of LCX buffers released or in development. Contact your local National Semiconductor representative for a current list of LCX products.

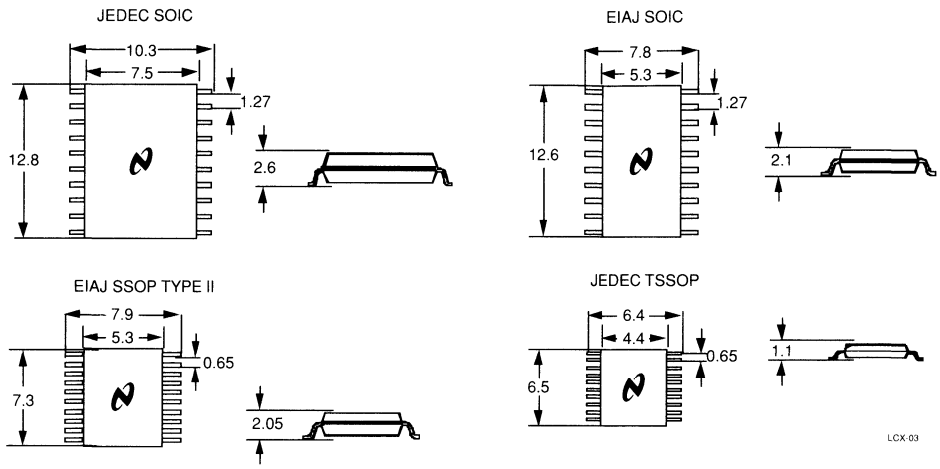
LCX Portfolio (continued)

Gates/Flip-Flops/Decoders/Multiplexers:

74LCX00	Quad 2-Input NAND
74LCX02	Quad 2-Input NOR
74LCX04	Hex Inverter
74LCX05	Open Drain
74LCX08	Quad 2-Input AND
74LCX10	Triple 3-Input NAND
74LCX11	Triple 3-Input AND
74LCX14	Hex Inverter with Schmitt Trigger Input
74LCX32	Quad 2-Input OR
74LCX74	Dual D-Type Positive Edge-Triggered Flip-Flop
74LCX86	Quad 2-Input Exclusive-OR
74LCX109	Dual J-K Flip-Flops with Preset and Clear
74LCX112	Dual J-K Flip-Flops with Preset and Clear
74LCX125	Quad Buffer
74LCX138	1-of-8 Decoder/Demultiplexer
74LCX157	Quad 2-Input Multiplexer
74LCX257	Quad 2-Input Multiplexer

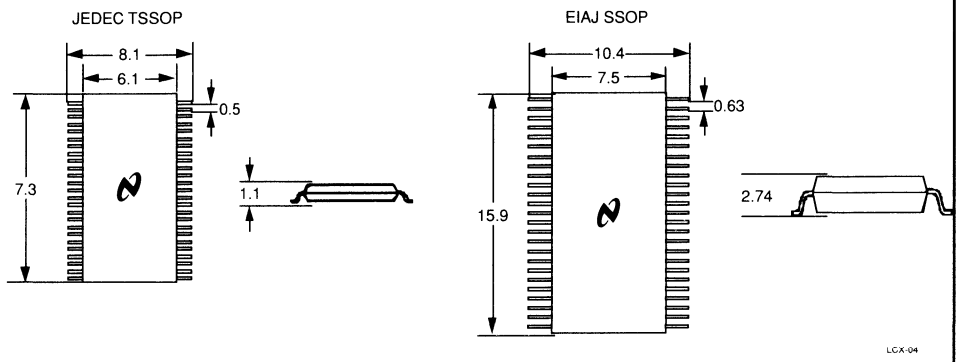
These LCX gates/MSI devices are released or in development. Contact your local National Semiconductor representative for a current list of LCX products.

Current Packaging Choices for Octals



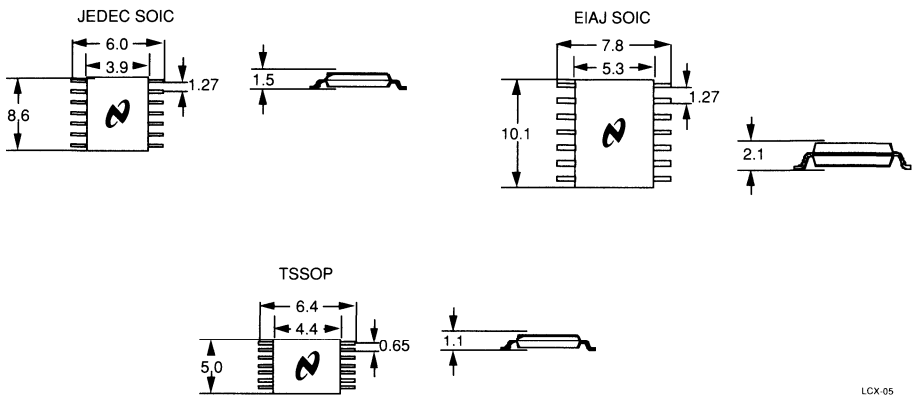
The four (4) packaging choices currently available for octals are:
JEDEC SOIC, EIAJ SOIC, EIAJ SSOP type II, and JEDEC TSSOP.

Current Packaging Choices for 16-bitters



The two (2) packaging choices currently available for 16-bit devices are:
EIAJ SSOP and JEDEC TSSOP.

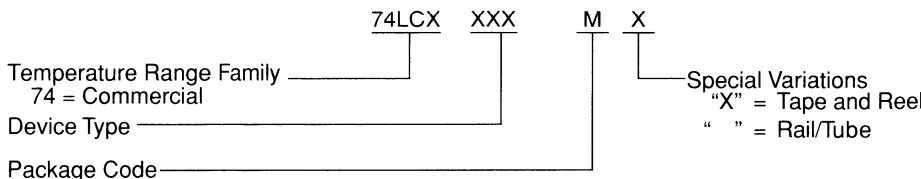
Current Packaging Choices for Gates



There are 3 packaging choices currently available for gates:

JEDEC SOIC, EIAJ SOIC, and JEDEC TSSOP

LCX Package Nomenclature



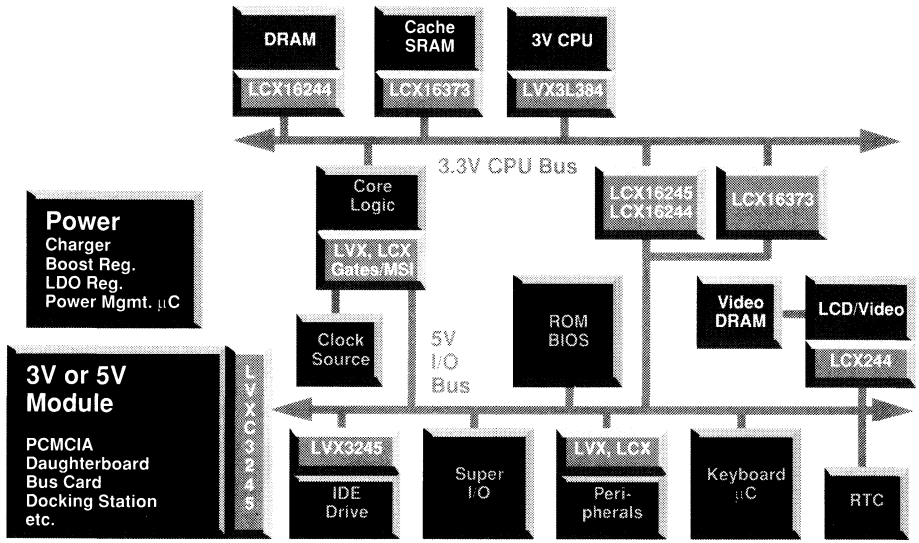
M = (0.150" Wide) Molded Small Outline Package, JEDEC (14/16 Lead)
WM = (0.300" Wide) Molded Small Outline Package, JEDEC (20/24 Lead)
SJ = (0.300" Wide) Molded Small Outline Package, EIAJ (14/16/20/24 Lead)
MTC = Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width (14/16/20/24 Lead)
MEA = Shrink Small Outline Package, JEDEC (48/56 Lead)
MTD = Thin Shrink Outline Package, JEDEC, 6.1 mm Body Width (48/56 Lead)
MSA = Molded Shrink Small Outline Package, EIAJ, TYPE II (24/24 Lead)

Intro-01

This chart shows how to order a LCX device with all of the various package codes.

For a complete list of available functions and advanced information consult your local sales representative or refer to a current product status guide.

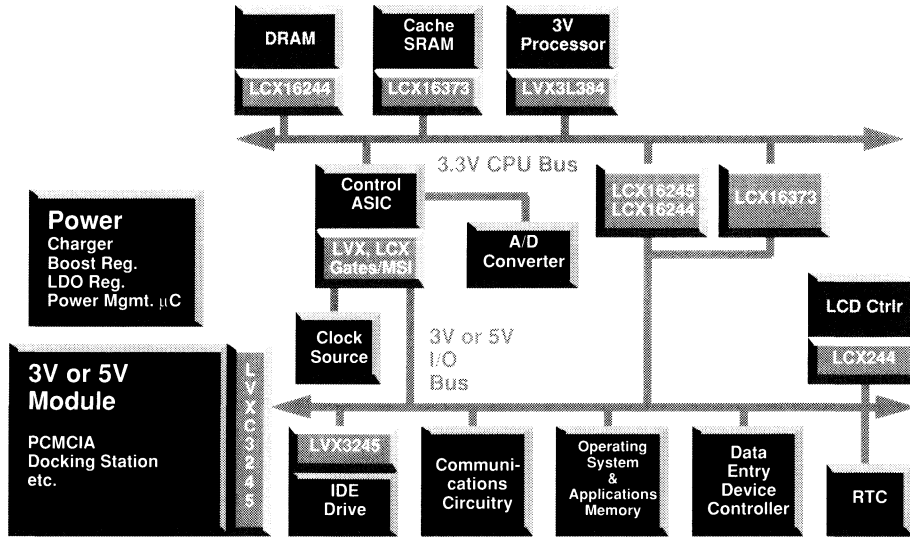
3V/5V Hybrid PC/Notebook LV Applications



Here's where you can find National's LCX family (and other National *CROSSVOLT* low voltage logicproducts) in a typical PC/notebook design:

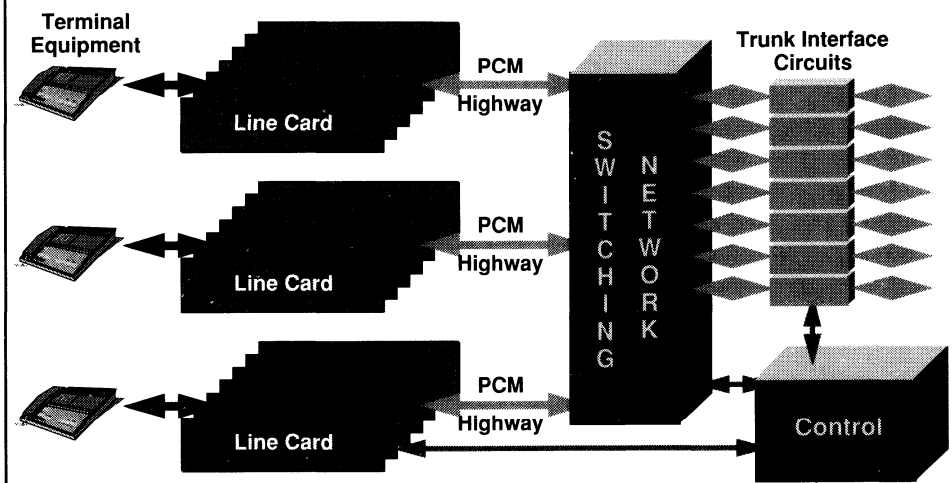
- Latches and transceivers are often used between the CPU bus and I/O bus. 5V tolerant LCX16245 and LCX16373 logic are perfect here.
- LCX16373 or LCX573 can be used for SRAM address latching, while LCX16244 can be used for driving large DRAM arrays.
- Look for 250ps bus switches (74LVX3L384/383) to interface between a 3V processor and low cost 5V memory. Bus switches have no drive and virtually no delay which makes them ideal in this application.
- Translation is sometimes required between peripherals such as video and drive chips and the rest of the system. LVX dual supply translating transceivers (LVXX) or 5V tolerant LCX244/245 functions can be used.
- There may be a need for glue logic and/or translation around the chipset. Use high speed LCX logic to handle the glue logic. Common functions include '08, '138, and '125.
- Use National's LVX configurable dual supply translating transceivers (LVXC) to interface to 3V and 5V plug-in (e.g. PCMCIA, daughterboard) cards or docking stations. The LVXC devices' B-port can be used to scale its signals for either 3V or 5V "on-the-fly."

Handheld Electronic Device Applications



National's LCX High Speed CMOS Low Voltage Logic has many applications in portable systems. Popular applications include bus buffering, address latching, 3V/5V translation, glue logic, etc.

Class 5 CO Switch or PABX LV Applications

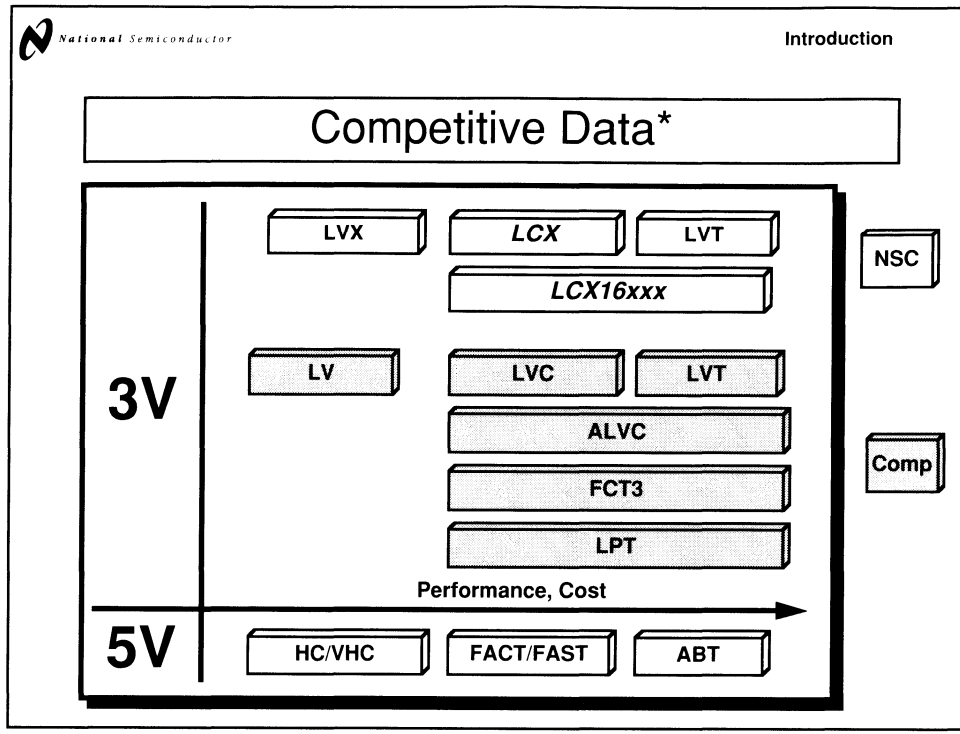


3V Uses:
- **Backplane Applications: LCX16245, LVT16245, 3V BTL, 3V GTL**
- **µP-Based Subsystems: LCX & LVX 16-bitters, octals, gates/MSI**
- **Terminal Equipment (cordless phones, fax, etc.): LVX, LCX, LVQ gates/MSI**

National's *CROSSVOLT*™ Low Voltage Logic can be found in three main areas in telecom systems:

- LCX logic can be used to drive the many backplanes in a telecom switching system.
- The switching network and control circuitry contain microprocessors that will need 3V logic in some of the same places as a PC/notebook system (see PC/notebook application foil). LCX is commonly used here for data buffering and glue logic.
- Portable terminal equipment such as cordless phones, car faxes, cellular phones, etc. are battery powered and will use 3V IC's to reduce power consumption. You may find some 3V logic that has not been integrated into an ASIC in these systems.

Note: PCM refers to Pulse Code Modulation.



In each of the following chapters, competitive comparison data for various tests is compared to National's LCX family. The families included in the test (if they were available at the time of the test) are shown above as "comp" or competition. These devices tested were purchased from local distributors around the time of the testing.*

* Competitive comparison data is omitted from this databook, but is available in the *LCX Designer's Guide*, Literature #585359.

Summary

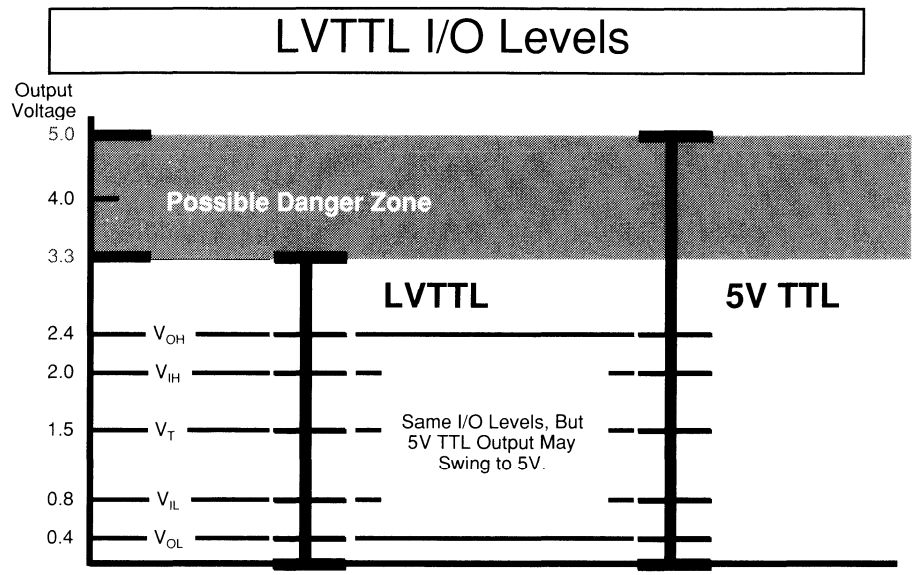
LCX, a 3V Logic family having the following advantages:

- The standard for Low Voltage Logic
- Supported by the Low Voltage Logic Alliance
  - Motorola, National, Toshiba
- Also supported by SGS-Thomson
- Ideal for both pure 3V and mixed voltage (3V/5V) systems
- Superior performance in various applications platforms
  - Notebooks, Handheld instruments & PDAs
  - PCs, Workstations, and Telecom
- Very low power consumption and noise

A brief discussion of how we have specified the performance of the LCX family has been presented. Listed below are the features and benefits of using this product family.

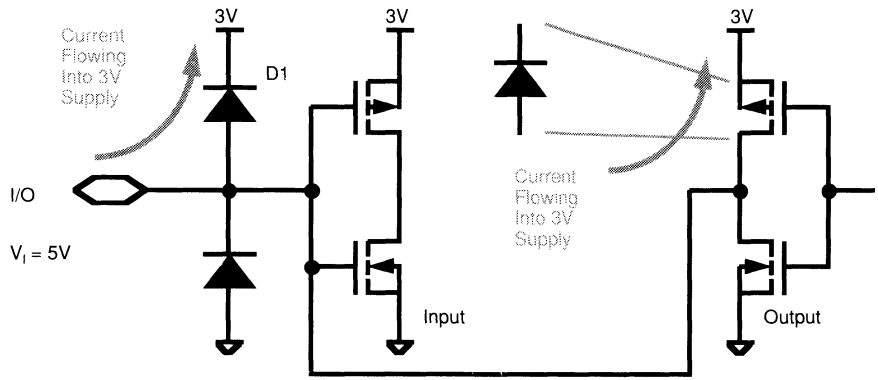
- Over-voltage tolerance on all inputs and outputs
  - — Allow direct interface of 3V and 5V systems
- Proprietary noise control circuitry (Graduated Turn-On)
  - — Reduce EMI, ground bounce, and system overshoot & undershoot
- Low power consumption
  - — Extend battery life
  - — Reduce heat generation
- Power up/down over-voltage protection
  - — Ideal for power-managed and live insertion applications
- Extended Vcc range
  - — Provides unregulated battery operation
- Alternate sources
  - — Readily available
  - — Low cost

Chapter 2
Interfacing 3V/5V Signals



Theoretically there should be no need to translate between 3V and 5V TTL signals since the JEDEC specifications governing the signals levels, 5V TTL and LVTTL (low voltage TTL), specify the same voltage levels for a valid "one" and a valid "zero." Sometimes problems do occur, however, because the outputs of 5V devices can swing to the 5V rail when in the high state, causing some 3V circuits which are not tolerant to 5V signals to be damaged.

Traditional 3V I/O (Type 1)



- ESD & Intrinsic Diodes Will Be Forward Biased When $V_I > V_{CC} + V_F$
  - Causing current flow from 5V to 3V supply

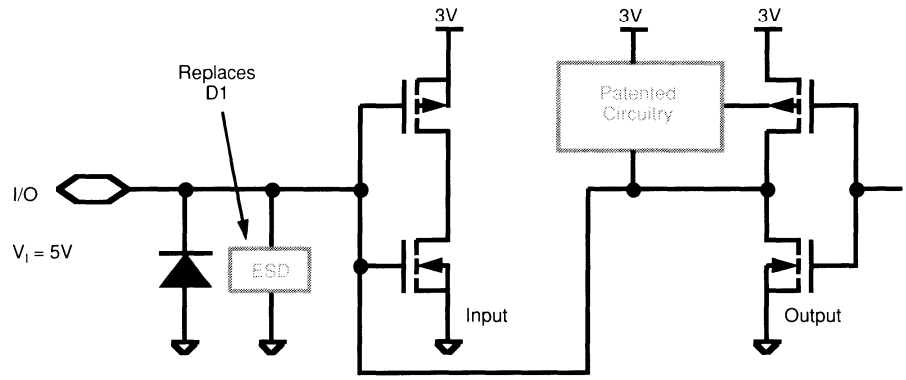
This is a classical digital CMOS I/O structure showing ESD protection diodes. This circuit contains an ESD diode D1 at the input which becomes forward biased when V_I is approaches $V_{CC} + \approx 0.7V$. This will cause large currents (sometimes > 1A) to flow into the 3V supply, possibly damaging the device.

Output drivers will experience a similar problem even if there is no ESD diode present between output and V_{CC} because such a diode exists intrinsically on the PMOS pull-up device. The diode consists of the pn-junction which is formed by the p+ drain to n-well connection. Note that bidirectional I/O pins contain not only an input structure but also an output structure, so they are likely to also have this intrinsic diode. This intrinsic diode will also be forward-biased if subjected to 5V.

Let us then, refer to a "type 1" input, output, or I/O pin as one which cannot tolerate 5V signals.

Note: IC wafer processes with geometries at or below 0.5μ usually cannot tolerate 5V signals for another reason: their thin gate oxide may break down, damaging the device. This is failure mechanism is not prevalent today but is mentioned because it will become an issue as IC performance demands process geometries in the ≤0.5μ range.

5V Tolerant I/O (Type 2)



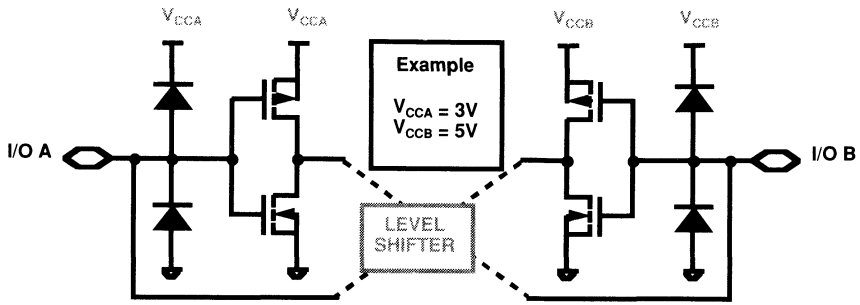
- Modified ESD Device Will Not Turn On ($I_I \approx 0$) For $V_I \geq V_{CC}$
- Tolerates 5V On Outputs When TRI-STATE
- Use This I/O to Interface to 5V TTL in Most Cases

The 5V tolerant I/O structure replaces the upper ESD diode D1 with one of many proprietary ESD protection schemes which will not turn on when 5V signals are applied. These new ESD structures, however, do provide ESD protection greater than 2000 volts (in fact we have tested LCX devices which pass 4000V). The outputs are similar, but also have special circuitry to keep the instrinsic diode at the PMOS pull-up and the PMOS itself from turning on when an overvoltage is applied. This is accomplished partially by biasing the bulk region of the PMOSFET with the higher of the 3V supply or output voltages.

Let us then, refer to a 5V tolerant I/O as "type 2" for the sake of this presentation. Most of National's low voltage logic families such as LCX, LVX, and LVT are 5V tolerant hence the name *CROSSVOLT*™. (LVX has 5V tolerant inputs only.)

5V tolerant I/O can be used in most mixed 3V/5V (as well as pure 3V) applications.

Dual Supply Translator I/O (Type 3)



- Input & Output Buffers Are Scaled To Either 3V or 5V
  - Outputs can drive to rail
- Use Dual Supply Translator to Interface to 5V non-TTL Inputs or 5V Bus With Pull-Ups, Otherwise Use Type 2

IC's with this I/O structure, let's call it "type 3," have dual supplies: one for 3V and one for 5V. Therefore, some I/O can be powered at 3V and others at 5V, scaling the input/output signals to match the external signal levels. The chip's internal circuitry may be either 3V or 5V and interfaces to the I/O through a level shifter.

Since the I/O are already scaled to match the external signals, no special ESD protection techniques are needed. No overvoltage tolerance is needed because the dual supplies and the level shifters perform the translation function. Since the 5V outputs are powered from a 5V supply, they can tolerate 5V signals and can pull the output up to the 5V rail in their high state.

This dual supply I/O structure needs extra Vcc pins, but is capable of amplifying a 0V-3V signal swing to 0V-5V a signal swing which is required in a two applications: driving non-T-compatible 5V devices and driving busses which are pulled up to 5V. Examples of dual supply translators include the 74LVX3245/4245/C3245/C4245 devices from National.

Examples of Logic Types

	5V		3V		
	TTL (Reduced Swing)	**CMOS (Rail-to-Rail Swing)**	**TTL/CMOS Pure 3V (Type 1)**	**TTL/CMOS 5V Tolerant (Type 2)**	**TTL/CMOS Dual Supply Translator (Type 3)**
Inputs	FAST® ABT ABTC BCT ACT ACTQ LS ALS etc.	AC HC VHC etc.	LVQ LV LVC ALVC	**LCX** LVX LVT	LVX3245 LVX4245 LVXC3245 LVXC4245
Outputs	FAST® LS ALS etc.	AC HC VHC ACT ABT etc.	LVQ LV LVC ALVC LVX	**LCX** LVT	LVX3245 LVX4245 LVXC3245 LVXC4245

Here are some examples of the various types of logic being discussed in this presentation.

In this case of outputs, CMOS here refers to full rail-to-rail swing of the outputs, while TTL means bipolar TTL or reduced level swing. In the case of inputs, CMOS refers to inputs which are non-TTL compatible and require a full 5V rail-to-rail swing to determine a valid "one" from a valid "zero." CMOS does not refer to the fabrication technology, though most CMOS and BiCMOS devices have CMOS rail-to-rail swings on their outputs.

Interfacing 3V/5V Logic

Receiver (Input or I/O)

Driver (Output)		5V		3V		
		TTL	CMOS (Non-TTL Compatible)	TTL/CMOS Pure 3V (Type 1)	TTL/CMOS 5V Tolerant (Type 2)	TTL/CMOS Dual Supply Translator (Type 3)
5V	TTL (Red. Swing)	Yes Direct	NO None	OK (Note 1)	Yes Direct	Yes Direct ← Interface? ← Method
	CMOS (Full Swing)	Yes Direct	Yes Direct	NO None	Yes Direct	Yes Direct
3V	TTL/CMOS Pure 3V (Type 1)	OK Pull-Down	NO None	Yes Direct	Yes Direct	Yes Direct
	TTL/CMOS 5V Tolerant (Type 2)	OK Tri-State	NO None	Yes Direct	Yes Direct	Yes Direct
	TTL/CMOS Dual Supply Translator (Type 3)	Yes Direct	Yes Direct	Yes Direct	Yes Direct	Yes Direct

Direct Interface Exceptions

Case 1
Case 2
Case 3
Case 4

Note 1: Regulate 3V & 5V supplies together.

This table summarizes the interface between 3V and 5V logic. Each box shows the following information:

Is it OK to interface?

What interface method should be used?

for the case of the device in the far left column driving the device in the top row. The four cases in which a direct interface is not recommended are highlighted and each will be discussed in the following foils.

As described in a previous slide, 5V CMOS refers to 5V rail-to-rail input/output swing not process technology.

3V/5V Direct Interface Exceptions

Case

1 5V Reduced Swing to 3V Non-5V Tolerant
2 5V CMOS (Full Swing) to 3V Non-5V Tolerant
3 3V Types 1 & 2 to 5V Non-TTL CMOS Inputs
4 3V Types 1 & 2 to IC's & Busses With Pull-Ups

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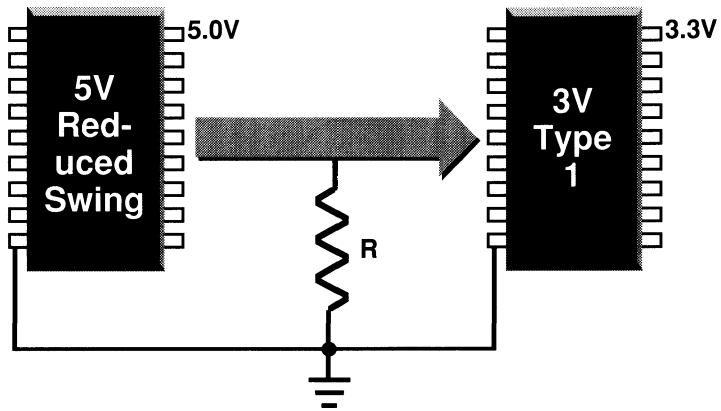
* All Other Interfaces Can Usually Be Handled Directly

As seen from the preceding table, most interfacing can be done directly. There are four exceptions, shown above. These four cases will be examined in further detail.

Case 1: Old Method



- 5V V_{OH} May Exceed 3V V_{CC} Causing Current To Flow To 3V Supply
  - *Use 5V tolerant (type 2) instead!*

Type 1 inputs should not interface directly to 5V TTL outputs, because the 5V TTL V_{OH} may be greater than the 3V supply voltage plus the 0.7V ESD diode drop. This will cause the ESD diode to turn on, sinking large currents into the 3V supply.

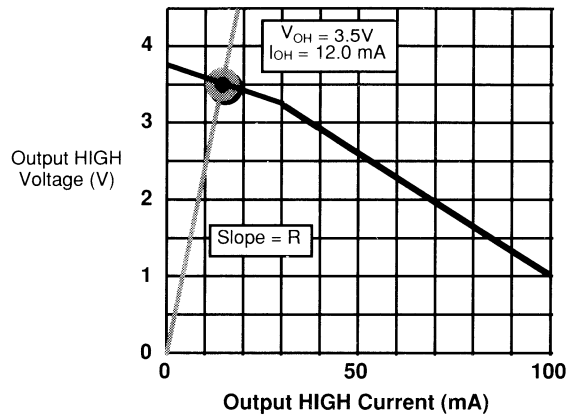
The best solution in this case is to use a type 2 (5V tolerant) device (like LCX) to replace the 3V type 1 device or to translate between the two devices.

If, however, LCX cannot be used, the following should be considered when interfacing 5V TTL to 3V type 1 (non-5V tolerant) devices:

1) Run the 5V supply on the low side, and the 3V supply on the high side to minimize the 5V V_{OH} to 3V V_{CC} difference. Also, regulate both supplies together to avoid having the 5V supply rise while the 3V supply droops.

2) Add a parallel termination resistor to ground on every signal where the 5V device is driving the 3V device. This will help lower V_{OH} at the expense of additional output current. The method of determining "R" is determined on the next foil.

Case 1: Old Method (continued)



This is an example. Actual value of R will depend V_{OH}-I_{OH} curve.

- R = 3.5V / (I_{OH} @ V_{OH} = 3.5V)
  - Note: Using parallel resistor termination will consume additional power

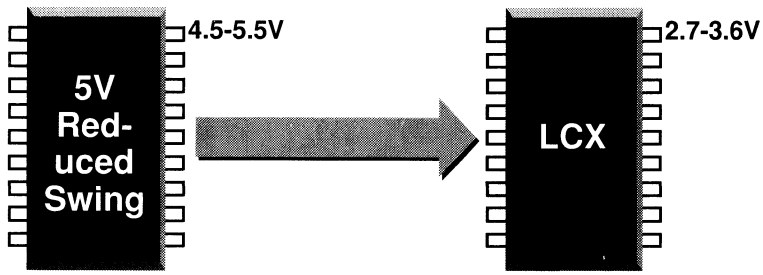
Use the V_{OH} vs. I_{OH} curve of the 5V TTL device to find "R." The goal is to reduce the V_{OH} to a safe value. Since V_{OH} should not be above the 3V V_{CC} plus a 0.7V ESD diode voltage drop (3.3V-10% + 0.7V = 3.7V), we choose V_{OH} max to be 3.5V This would correspond to an I_{OH} of 12mA and a termination resistance of R = 3.5V/12mA = 292Ω or about 250Ω to be safe.

Note that the termination resistor will increase DC I_{OH}. Also, a 5V FAST® device is used in this example; make sure you use the correct V_{OH} vs. I_{OH} curve.

Some designers use a series resistor between 3V and 5V devices instead of a parallel resistor. This series resistor is intended to limit the current through the ESD diode of the 3V device when it turns on. This method also suffers from problems. Once the ESD diode turns on, current will flow from the 5V to the 3V supplies, adding noise to both supplies. Also, the resistor will addadditional delay to the signal by increasing the RC time constant and by forcing the 5V device to have to turn off the ESD diode which does take time.

Clearly both of these schemes should be avoided. Use 5V tolerant LCX logic instead.

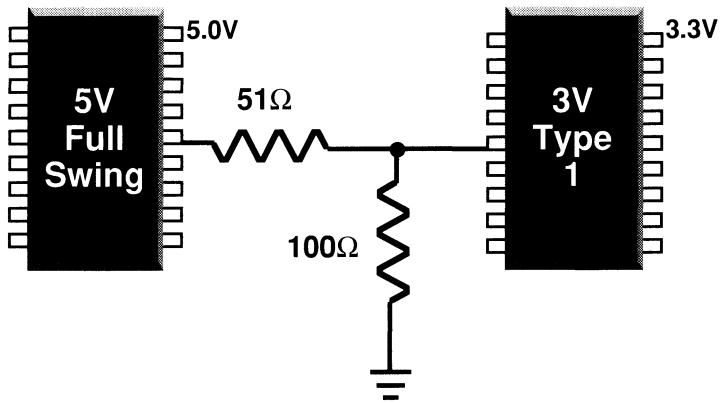
Case 1: LCX Solution (continued)



- Direct Interface: No Extra Components Needed!

The best way to interface between 5V reduced swing outputs and a 3V device is to replace the 3V device with a 5V tolerant family like LCX from National Semiconductor. LCX may also be used between the devices as a dedicated translator.

Case 2: Old Method



- Use 5V Tolerant I/O (Type 2) Instead!

Similar to case 1, non-5V tolerant type 1 inputs should not interface to 5V full-swing CMOS outputs because the 5V output V_{OH} may be greater than the 3V supply voltage plus the 0.7V ESD diode drop. This will cause the ESD diode to turn on, sinking large currents into the 3V supply.

The best solution in this case is to use a 5V tolerant device like LCX to replace the 3V type 1 device or to translate between the two devices.

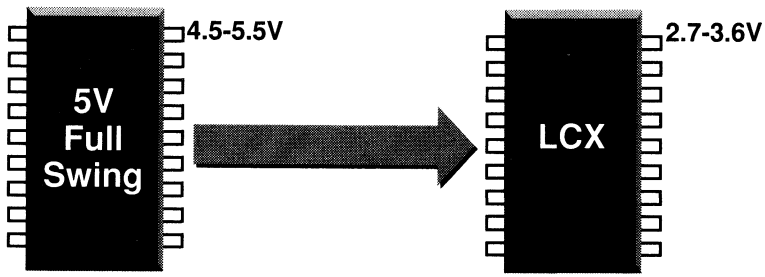
If, however, LCX cannot be used, the following should be considered:

1) Run the 5V supply on the low side, and the 3V supply on the high side to minimize the 5V V_{OH} to 3V V_{CC} difference. Also, regulate both supplies together to avoid having the 5V supply rise while the 3V supply droops.

2) Use a resistor divider network to reduce the 5V CMOS swing to acceptable levels. Empirically, it has been found that R1 = 51Ω and R2 = 100Ω are a good compromise between DC power loss and signal fidelity. Using a resistor network will impact propagation times and DC power consumption.

As in previous slides, 5V CMOS refers to 5V rail-to-rail input/output swing not process technology.

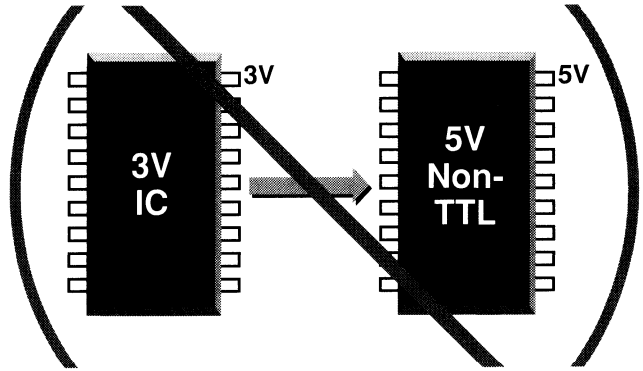
Case 2: LCX Solution (continued)



- Direct Interface: No Extra Components Needed!

The best way to interface between 5V full swing outputs and a 3V device is to replace the 3V device with a 5V tolerant family like LCX from National Semiconductor. LCX may also be used between the devices as a dedicated translator.

Case 3



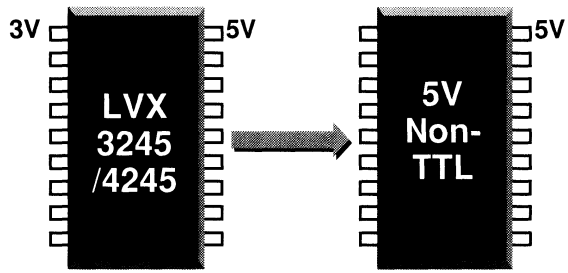
- 3V Outputs Cannot Meet The V_{IH} Requirement of 5V Non-TTL Compatible (full swing) Inputs
- Use A Dual Supply Translator (Type 3) Instead!

Never try to drive a 5V non-TTL compatible CMOS input (i.e. $V_{IH} \geq 3V$) with a 3V type 1 or 2 device because the V_{OH} of the 3V device will not meet the V_{IH} of the 5V non-TTL compatible CMOS device. Doing so will result in one or more of the following: (1) the 5V CMOS device will not switch reliably; (2), you will have no noise margin; (3), the CMOS input structure of the 5V device will not fully switch, resulting in excessive DC power consumption.

In this case you must use a dual supply translator (type 3) like National's 74LVX3245 or 74LVX4245 whose outputs can swing high enough to exceed the 5V CMOS V_{IH}.

As in previous slides, 5V CMOS refers to 5V rail-to-rail non-TTL compatible input swing, not process technology.

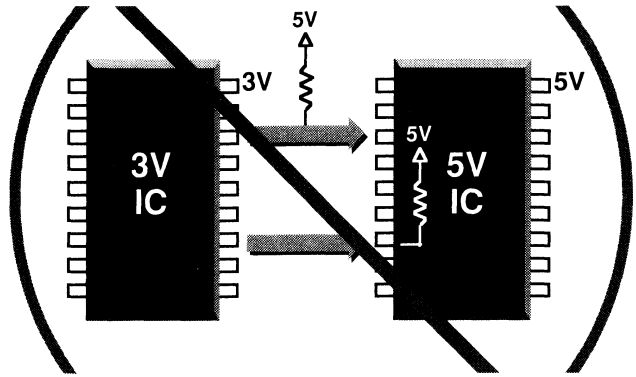
Case 3: LVX3245/4245 Solution (continued)



- Direct Interface: No Extra Components Needed!

Using a National 74LVX3245/4245 dual supply translator allows a direct connection between 3V components and a 5V non-TTL compatible (full swing input) CMOS component. The dual supply translator will scale 3V swing signals at its inputs to a full 5V rail-to-rail swing on its outputs.

Case 4

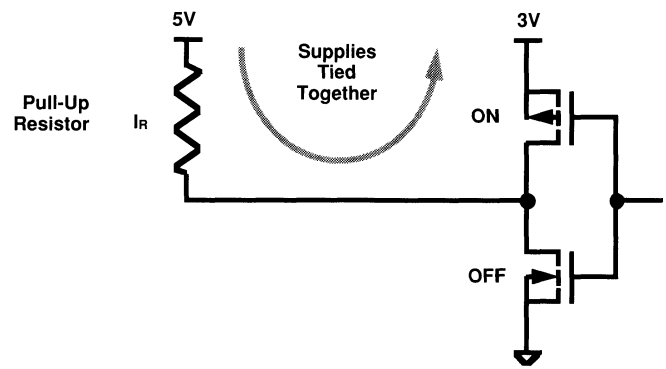


- Type 1 & 2 Outputs Should NOT Be Pulled Up To 5V
  - Allows current to flow into 3V supply
- *Use A Dual Supply Translator (Type 3) Instead!*

Although most 3V devices can safely drive 5V TTL devices, the designer should be aware that many busses are terminated through a pull-up resistor to 5 volts and many IC's (including PLD's, chipsets, etc.) have pull-ups on their inputs which will pull the 3V output to 5 volts. In addition, there is always the possibility for high contention on busses which can also expose the 3V output to 5 volts.

The best solution is to use a dual supply translator (type 3) device like National's 74LVX3245/425 with the 5V I/O interfacing to the 5V IC or bus which contains pull-ups.

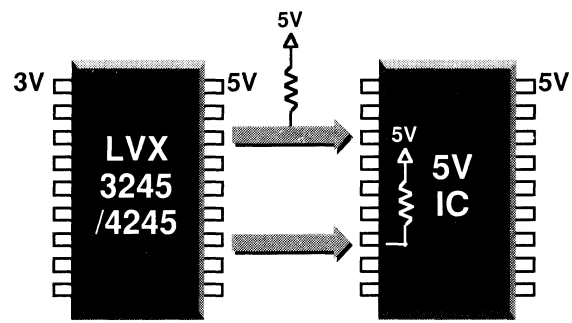
Case 4: Driving a Bus Pulled Up to 5V (continued)



- 3V Driver Will Connect 3V and 5V Supplies Together Through Resistor When In HIGH State

Clearly 3V active outputs cannot tolerate 5 volts without allowing large currents to flow into the 3V supply. To understand why this happens, consider the case that the outputs of the 3V device are in the high state. This means there is a very low impedance connection (through the output upper PMOS transistor) between the outputs and the 3V supply. If the outputs are pulled up to the 5V supply, you will be in effect connecting the 5V supply and 3V supply together through a resistor. If this resistor has a large value, only a small currents will flow which may be okay. If the resistor is small, then a large current may flow between the supplies. Either way, these situations and also bus contention between 3V and 5V outputs should be avoided.

Case 4: LVX3245/4245 Solution (continued)



- Direct Interface: No Extra Components Needed!

Using a National 74LVX3245/4245 dual supply translator allows a direct connection between 3V components and 5V pull-up resistors since the dual supply translator will scale 3V swing signals at its inputs to a full 5V rail-to-rail swing on its outputs. Therefore, the output of the dual supply translator, when in the HIGH state, will be at the 5V rail, not at the 3V rail.

3V/5V Interface Solutions

Receiver (Input)

Driver (Output)		5V		3V		
		TTL	CMOS (Non-TTL Compatible)	TTL/CMOS Pure 3V (Type 1)	TTL/CMOS 5V Tolerant (Type 2)	TTL/CMOS Dual Supply Translator (Type 3)
5V	TTL (Red. Swing)	Yes Direct	Use Type 3	Use Type 2	Yes Direct	Yes Direct
	CMOS (Full Swing)	Yes Direct	Yes Direct	Use Type 2	Yes Direct	Yes Direct
3V	TTL/CMOS Pure 3V (Type 1)	Use Types 1,2, or 3†	Use Type 3	Yes Direct	Yes Direct	Yes Direct
	TTL/CMOS 5V Tolerant (Type 2)	Use Types 1,2, or 3†	Use Type 3	Yes Direct	Yes Direct	Yes Direct
	TTL/CMOS Dual Supply Translator (Type 3)	Yes Direct	Yes Direct	Yes Direct	Yes Direct	Yes Direct

Direct Interface Exceptions

Case 1

Case 2

Case 3

Case 4

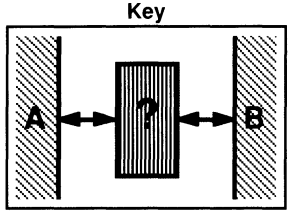
† Use dual supply (type 3) when pull-ups to 5V supply are present, otherwise use any 3V logic family.

This table summarizes the solutions that can be utilized for the four exceptions where a direct interface is not recommended. It shows what I/O types to use to make a ***direct*** interface possible without the need for external resistors, etc.

The important point here is that 5V tolerant logic such as LCX from National Semiconductor can be used in almost all cases but two in which a dual supply translator must be used.

As in previous slides, 5V CMOS refers to 5V rail-to-rail input/output swing not process technology.

3V/5V Bidirectional Interface Solutions



A \ B		5V		3V
		CMOS (Full Swing)	TTL	TTL/CMOS
5V	CMOS (Full Swing)	AC HC VHC etc.	ACT FCT HCT	Dual Supply
5V	TTL	ACT FCT HCT	ALS FAST etc.	LCX, LVT Dual Supply
3V	TTL/CMOS	Dual Supply	LCX, LVT Dual Supply	Any 3V Family

The previous slide shows how to interface unidirectional signals. In many cases a bidirectional signal is present which is buffered through a logic '245 function. This table shows what 3V logic family to use ("?") between two other devices ("A" & "B") one of which is probably 3V and the other 5V.

As in previous slides, 5V CMOS refers to 5V rail-to-rail input/output swing not process technology.

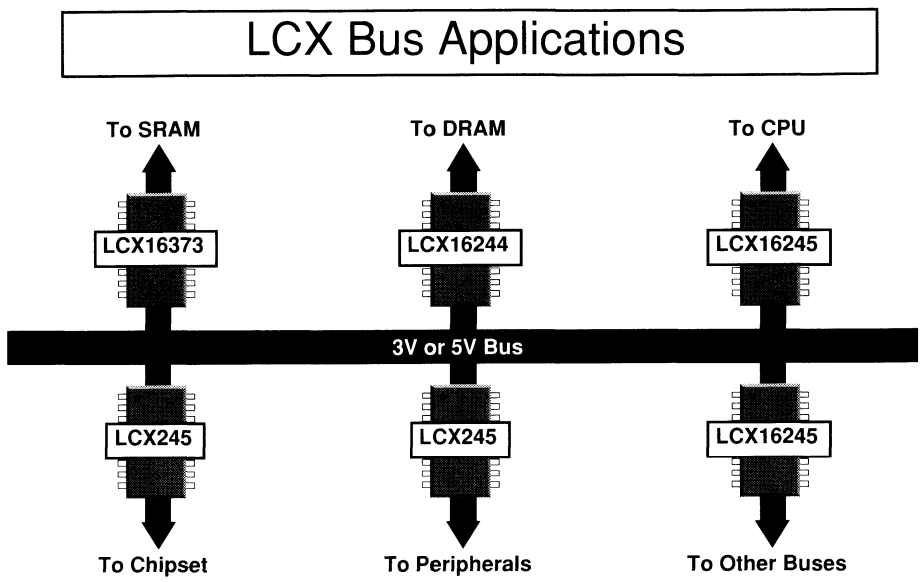
Interfacing 3V/5V Logic Summary

Type

1 Be Careful When Using Non-5V Tolerant Logic
2 5V Tolerant LCX Logic Can Interface Directly To 5V Logic In Most Cases!
3 Use Dual Supply Translators When:
  - Driving 5V non-TTL CMOS inputs
  - Interfacing to IC's or busses whose inputs are pulled up to 5V
  - Highest noise margins are required

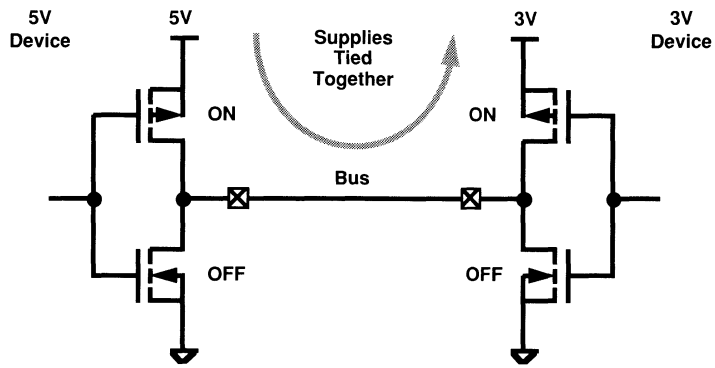
In summary:

- Use non-5V tolerant (type 1) logic to interface to 3V-only signals
- 5V tolerant (type 2) logic is perfect for most 3V-only and mixed 3V/5V cases, except:
- Use dual supply translators (type 3) logic to interface to 5V CMOS swing inputs or busses which are pulled up to 5V



5V tolerant inputs and outputs allows LCX devices to function seamlessly in both 3V and mixed 3V/5V systems. Here are a few examples showing where LCX can be used to interface system components to a 3V or a 5V bus. Note that there are many other applications for LCX in a typical system in addition to bus applications.

Avoid 3V/5V Bus Contention



- Contending 3V and 5V Drivers Will Connect 3V and 5V Supplies Together When In HIGH State

Normally one tries to avoid bus contention since two devices driving a bus to opposite logic levels will create a short circuit between V_{CC} and ground. Current will be limited by the ON resistance of the sinking and sourcing transistors and/or the 5V supply itself.

Similarly bus contention should be avoided for 3V devices. When 5V tolerant 3V devices are driving a 5V bus, bus contention will cause large currents to flow not only when outputs are driving to opposite logic levels, but also when 3V and 5V outputs are both driving to the HIGH state! In this case, the 3V and the 5V supply will be connected and current will only be limited by the ON resistance of the drivers and/or the supplies themselves. Clearly this situation causes wastes much power, creates noise on both supplies, and can damage system components!

Therefore, avoid bus contention and avoid driving 5V buses which are pulled up to 5V through pull up resistors for the same reason.

How We Guarantee Overvoltage Tolerance

- 5V tolerance is listed in the LCX product title and also the features
- Input and output voltages (V_I & V_O) are specified up to 7V in the absolute maximum ratings and up to 5.5V in the recommended operating conditions
- Input and TRI-STATE output leakage currents (I_I & I_{OZ}) are specified at ±5μA @ 5.5V in the DC electrical characteristics
- Bench data shows typical National LCX overvoltage tolerance to 13V

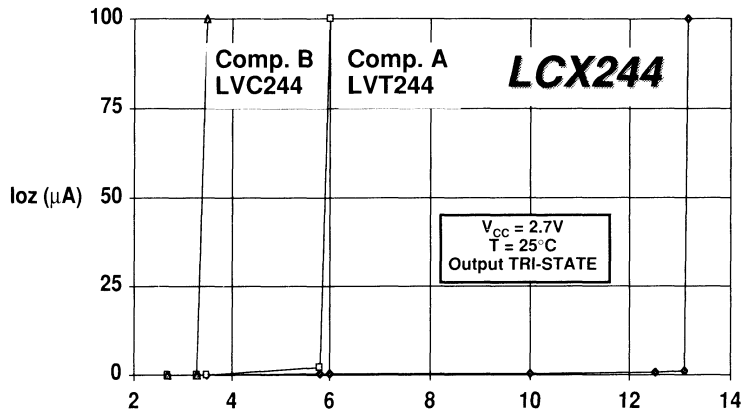
LCX overvoltage tolerance is guaranteed in a few ways. First, 5V tolerance is actually declared as part of the product title and product features. Second, overvoltage tolerance is guaranteed by the combination of V_I, V_O, I_I, and I_{OZ} parameters. These voltage and current parameters define the maximum allowable voltages upon the signal pins and how much leakage current will flow when the signal pins are exposed to overvoltage. Note that the current parameters are the most important parameters because they guarantee only small leakage currents will flow during overvoltage (usually 5.5V). Do NOT be fooled by families that claim 5V tolerance but force the system designer to limit the current during overvoltage conditions. In these cases, the families do not guarantee the signal pin breakdown voltage will exceed the 5 volts. The LCX family not only guarantees 5V tolerance without breakdown, but bench data shows typical overvoltage tolerance to 13V on today's LCX devices.

LCX Overvoltage Tolerance

Pin	Recom.	Abs. Max	Condition
Input	5.5V	7V	
Control	5.5V	7V	
I/O	5.5V	7V	TRI-STATE or Input
Output	5.5V	7V	TRI-STATE

The table above shows the signal pin overvoltage tolerance absolute maximum ratings and recommended operating conditions for LCX devices. Up to 7V is allowed on signal pins and within the recommended operating condition $0V \leq V_{I,O} \leq 5.5V$ input and output leakage currents are specified to be very small. Typical bench data shows that National LCX devices being manufactured today will tolerate up to 13V on inputs, control pins, TRI-STATE I/O pins, and disabled outputs before breaking down.

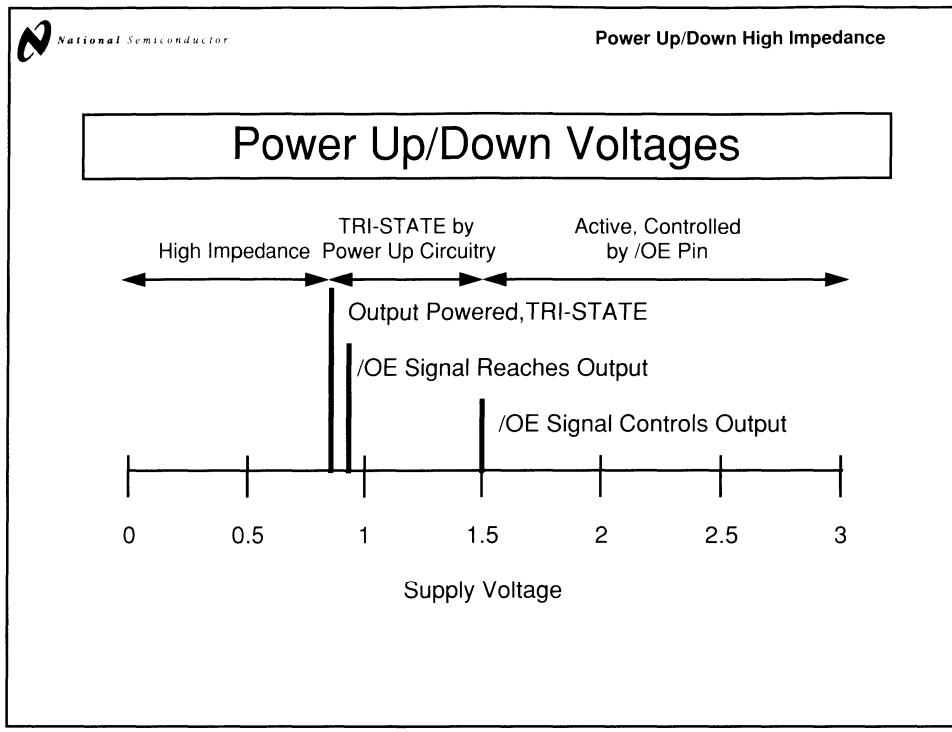
Output Overvoltage Tolerance Comparison



Note that signal overshoot and reflections can cause voltages above 5V for short durations.

The chart above illustrates the overvoltage tolerance of TRI-STATE outputs of various 3V logic families. Note that LCX is not only 5V tolerant, but also tolerates overvoltages greater than 5V which could be caused by reflections, noise, etc. The LVC device is not considered 5V tolerant at its outputs and large currents will flow into its outputs if the outputs are exposed to 5V.

Chapter 3
Power Up/Down High Impedance

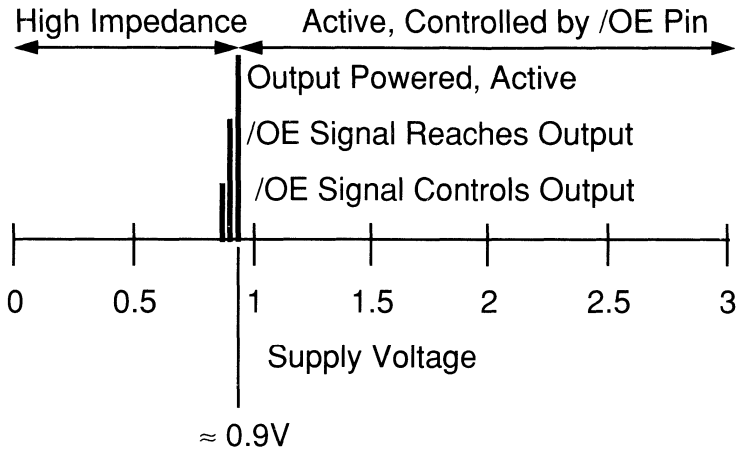


In both power management and live insertion applications where power up and power down high impedance is an issue, the system designer would ideally like to avoid having the device which is powering up or down discharging significant charge onto or out of the bus.

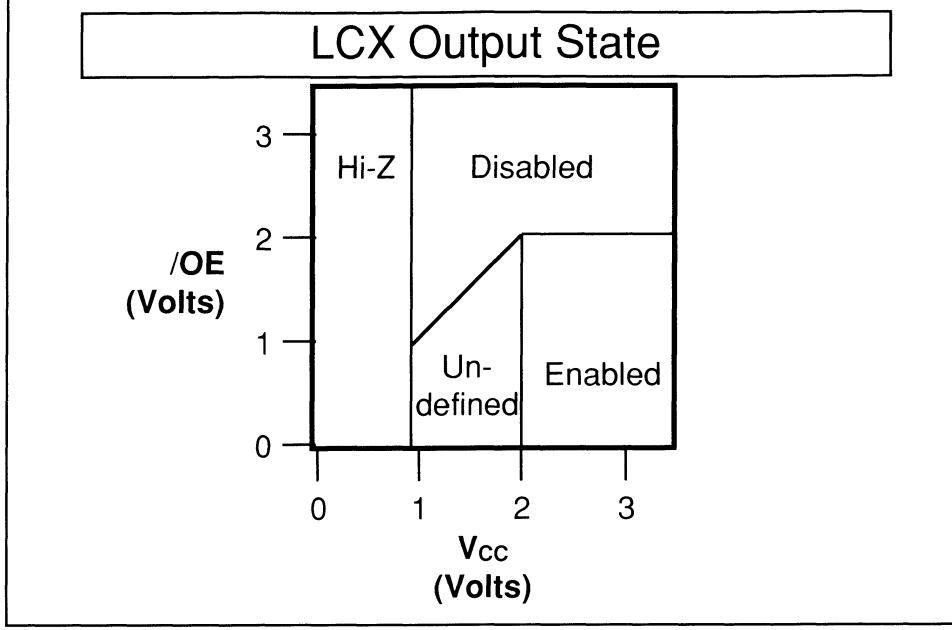
To facilitate this, the signal pins of a transceiver should remain at high impedance until commanded by the active system. This includes output pins which therefore should remain either at high impedance or TRI-STATE until the /OE (output enable) pin can respond to a purposely generated signal. While in either the high impedance or TRI-STATE states the outputs will typically source or sink typically <1μA of current, thereby not significantly disturbing already active portions of the system.

The diagram above shows the power up/down chart of a transceiver which meets these criteria. Internal circuitry assures that the outputs are powered, TRI-STATE, and are receiving the /OE pin signal before control is relinquished to the /OE pin. In this case, the output represents a high impedance until the output active voltage and is then TRI-STATE until the time the /OE signal is allowed to control the output. At this point, the output will remain TRI-STATE only if the /OE pin is high. This can be usually be assured by pulling the /OE pin to V_{CC} through a pull-up resistor.

LCX Power Up/Down Voltages



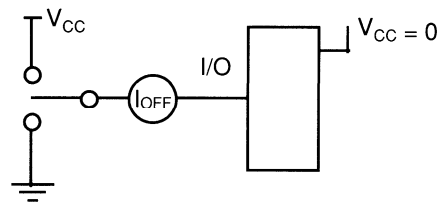
National LCX signal pins stay in the high impedance state at supply voltages lower than about 0.9V. At about 0.9V, the outputs become active, but not before the /OE signal assumes control of the outputs. Therefore, if the /OE pin is controlled during power up (e.g. it is pulled to V_{CC} through a resistor), the LCX outputs will remain in the high impedance state or TRI-STATE during power up or power down regardless of the supply voltage.



Here is another way to view the relationship of /OE and V_{CC} to the output state. If /OE follows (is pulled up to) V_{CC}, the LCX outputs will transition directly from high impedance to TRI-STATE and vice-versa during power up and power down. The high impedance nature of LCX outputs when powered down is a direct result of the LCX's overvoltage tolerance circuitry which remove the diode paths from the I/O to V_{CC} pins (see Chapter 2).

The LCX I_{OFF} Specification

- I_{OFF}= the maximum leakage into/out of an LCX signal pin when $V_{CC} = 0$.
- $I_{OFF} \leq 10\mu A$ for LCX.
- Low I_{OFF} means active circuitry/buses will not be affected by powered down LCX devices.



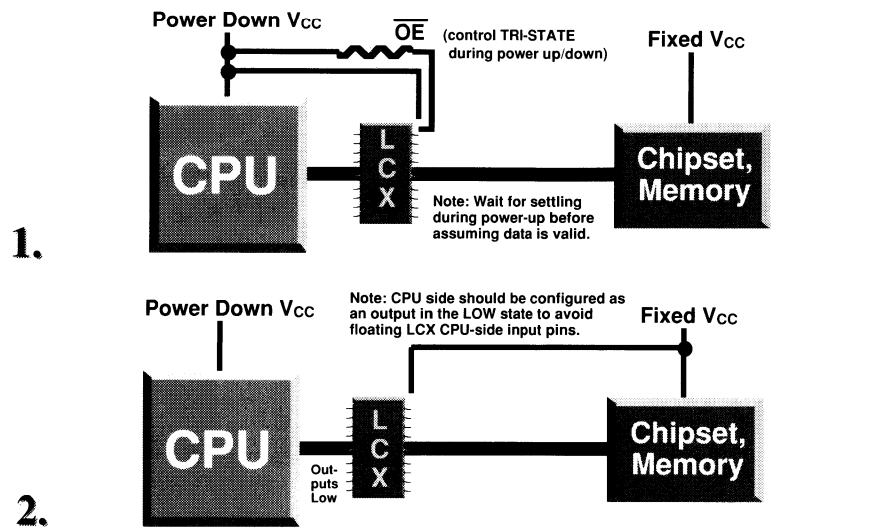
The I_{OFF} specifications guarantees LCX signal pins power down in the high impedance state.

I_{OFF} is the maximum current that will flow into or out of the signal pin of a device which is completely powered down. For LCX, I_{OFF} is less than 10µA which means that powered down LCX devices will not significantly disturb active signals to which the LCX device may be connected.

LCX For Power Management

The trend toward portability, battery operation, and green appliances is driving the need for complex power management schemes. The fact that LCX inputs and outputs power down to the high impedance state allows LCX to isolate active portions of the system from powered down portions of the system, greatly reducing the power consumption of the entire system.

Power Management Applications



In addition to very low static and dynamic power consumption, the ability of LCX logic inputs and outputs to power down to the high impedance state can help system designers implement power management schemes to even further reduce power consumption. In these power management schemes, portions of the system will be powered down to save power while other portions are active.

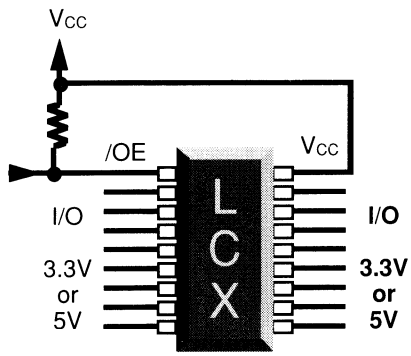
The example above shows a microprocessor (CPU) being powered down, while peripherals are still active. LCX can be used to isolate the powered down from the active portions of the system in two configurations:

1) Power down the LCX device with the other circuitry to be powered down. The LCX inputs and outputs will power down to the high impedance state so that the LCX device will not affect the signals of the active circuitry.

2) Keep LCX powered up while it interfaces to the powered down circuitry. In this situation, pins that communicate to the powered down circuitry should be configured as outputs in the LOW state since inputs which are connected to powered down devices will float. Charges can accumulate on the floating inputs, moving the input voltage into the threshold region, causing the device to switch or even oscillate. Pull floating control input pins either high or low.

Configuration 1 is recommended since it takes advantage of the LCX power down high impedance feature and avoids the floating input problem of configuration 2.

Seamless Power Management

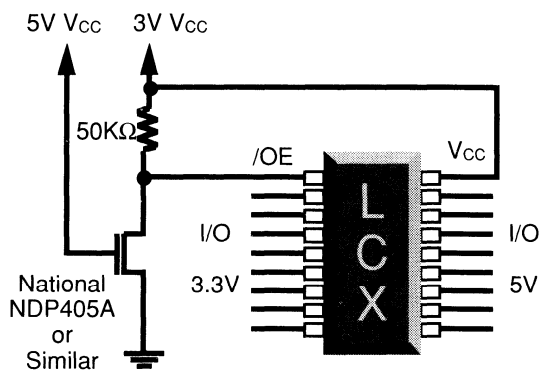


- Seamless power up/down operation

In power management applications, some circuits will be powered down while others are powered up. For example, the microprocessor may be powered down while peripheral devices are active. LCX can form a perfect interface between devices which are active and those which are powered down because LCX signal pins power down to high impedance. By using a pull-up resistor to V_{CC} on the /OE pin, glitch-free power up/down operation can be accomplished since the outputs will remain inactive until the /OE pin is asserted low.

The operation of LCX in this configuration is graphed at the end of this chapter.

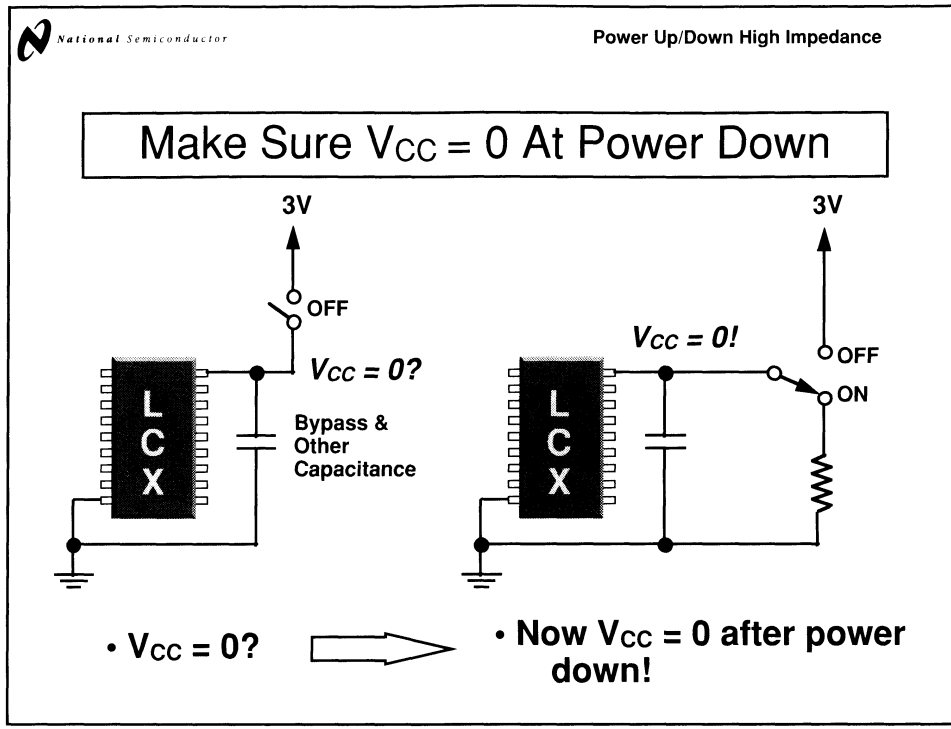
Isolating 3V and 5V Buses During 3V and/or 5V Power Failure



- 3.3V bus—5V bus isolation interface
- Isolation during 3.3V or 5V V_{CC} power up/down

Since LCX devices have 5V tolerant inputs and outputs (when TRI-STATE®), they are often used to buffer and translate between a 3V and 5V bus. Some applications require that this LCX buffer isolate the two buses when either the 3V or the 5V supply fails. By adding a simple transistor to the configuration, LCX outputs will be disabled/high impedance when either the 3V or the 5V supply is off.

Note: this circuit does not allow external signal control of the /OE (i.e., control by another IC) since this would contend with the pull-down MOSFET. External control of the /OE pin can be accomplished, however, by adding some additional circuitry.



In power managed applications, power is applied through a power FET or relay. It is often assumed that when the switch is open, devices will be powered down and the inputs and outputs of devices like LCX will be in the high impedance state. This is true when V_{CC} = 0 (below ≈0.9V for LCX), but since CMOS devices consume only microamps of static power and the bypass and other capacitiances between power and ground may be relatively large, it may take a long time before V_{CC} becomes zero. Therefore, a scheme to discharge current from the power/ground capacitance may be necessary to guarantee this so that the power down impedance feature of LCX can be taken advantage of.

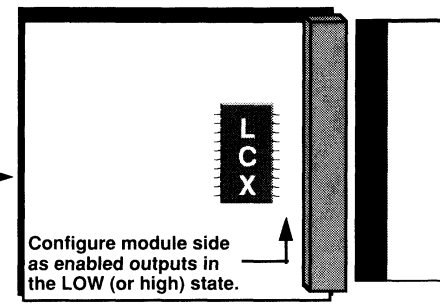
LCX For Modular Interfaces

For power managed applications, power up/down high impedance is needed for "2nd Level" live insertion capability. A staggered pin arrangement at the PC card edge in order to bias the /OE pin before supply and data pins is also required. This will ensure that when the card is inserted or removed, the LCX outputs will be at high impedance and the perturbations of the bus will be minimal, due only to passive (mostly capacitive) changes in bus loading when the board in inserted/removed.

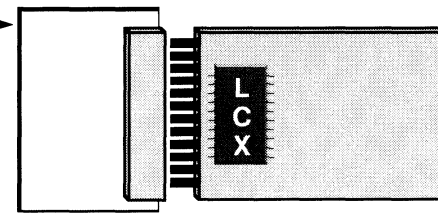
Modular Interface Applications

- Growing trend toward modularity
- Facilitates:
  - faster time to market
  - multiple product versions
  - upgrade path

1 Host Side
  - Configure Module Side As Outputs to Avoid Floating These Pins



2 Module Side
  - Connect In Sequence:
    - Ground
    - OE pin
    - Power
    - Other Pins



As consumers demand a wider range of product features, configurability, upgradeability, etc. modular interfaces are becoming more important. Logic is often used to buffer connectors and LCX is no exception. LCX can be used in two configurations, either on the host side or the card side:

1) Host Side: When the module is removed, the LCX inputs on the module side will be left floating. Therefore, configure module side pins as active (enabled) outputs in the low (or high) state when the module is removed. Pull floating control inputs high or low.

2) Module Side: LCX's power up/down high impedance capability can be used to provide level two live insertion capability. In other words, if the /OE pin is pulled high during power up/down, then the LCX outputs will remain in the high impedance state througout process of inserting or removing the board, minimally disturbing the host bus.

Live Insertion

- Live Insertion
  - Boards like those seen in a telephone company's central office switch are often removed and inserted while the backplane remains active.
  - Insertion and removal generates glitches and voltage level changes on the backplane.
- Level of Isolation
  - The capability level of the interface device to allow insertion of the board to which it is mounted.
  - 1st Level of Isolation
    - The ability of the interface device to allow board insertion without having to power the system down.
  - 2nd Level of Isolation
    - The ability of the interface device to allow board insertion without having to power the system down or suspend bus activity.
  - 3rd Level of Isolation
    - The ability of the interface device to allow board insertion without any limitations, restrictions or requirements of other circuits.

The requirements for the 1st level isolation include a method of suspending the bus activity to prevent glitch or level corruption of bus data.

Requirements for the 2nd level isolation include a method by which a bus can check for, and correct, faults introduced on the backplane during board insertion or a method for providing proper biasing of the board interface devices with a staggered pin arrangement on the board -backplane connector. Precondition biasing circuity for the interface device may also provide the required isolation.

The level of isolation has a direct impact on system uptime. Increasing levels of isolation allow for increased serviceability without system interruption. Board isolation provided by an interface device gives more freedom to the designer for focusing on purpose built board functions, reducing board design complexity and ultimately, board cost. LCX products offer the board designer and the board user these benefits with a 2nd level isolation solution.

Live Insertion Applications with LCX Products

- Power Up/Down High Impedance
- "2nd Level" Live Insertion

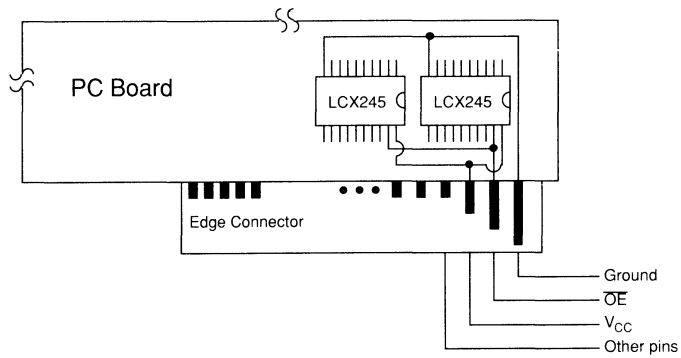


Figure 1: Staggered Pin Arrangement

For live insertion applications, power up/down high impedance is needed for "2nd level" live insertion. A staggered pin arrangement at the PC card edge is required (Figure 1) in order to bias the /OE pin before supply and data pins.

This will ensure that when the card is inserted or removed, the LCX outputs will be at high impedance and the perturbations of the bus will be minimal, due only to passive (mostly capacitive) changes in bus loading when the board is inserted or removed.

Chapter 4
Power Consumption

Power consumption is extremely important in battery powered applications. It should also be a concern in all other applications in order to reduce device-damaging heat in the system. The LCX family not only consumes virtually zero static power, but also is one of the lowest dynamic power consumers among advanced CMOS logic families. This means LCX can contribute significantly to lower power consumption in your system and allow you to meet your power budget.

In addition, the ability of LCX inputs and outputs to power down to the high impedance state means LCX can help isolate active and powered down portions of power managed systems, greatly reducing system power consumption further (see Chapter 3).

Power Specs and Terminology

- I_{CCQ}
  - Quiescent Power Supply Current
  - Spec = 10 µA maximum at V_{CC} = Max, 20 µA for 16-bit
  - Specifies power supply drain at 0 MHz or with inputs/outputs not switching (DC)
- I_{CCD}
  - Dynamic Power Supply Current
  - Not specified, but is graphed at the end of this chapter
- ΔI_{CC}
  - Power Supply Current Input at TTL HIGH ($V_{IH} = V_{CC} - 0.6V$)
  - Spec = 500 µA maximum at V_{CC} = Max
  - CMOS inputs at TTL HIGH level will exhibit a "soft" P- and N-channel turn-on creating resistive V_{CC} - GND current
- C_{PD}
  - Equivalent Power Dissipation Capacitance

I_{CCQ} is the static current consumed by the device. The outputs are disabled and unloaded so that only the power consumption of the device is measured.

I_{CCD} is the current consumed at a given switching frequency. Since this specification varies with frequency and load, it is not specified on the datasheet, but is plotted at the end of this chapter. It can also be roughly calculated from C_{PD} (see next foil).

ΔI_{CC} is the current consumed when the inputs are at $V_{IN} = V_{CC} - 0.6V$. When inputs are in this state, there will be some leakage from V_{CC} to ground caused by the internal transistors being "soft on." This leakage current is ΔI_{CC}. ΔI_{CC} is not normally used to calculate power dissipation since the LCX device inputs will normally be driven rail-to-rail.

C_{PD} is the "equivalent" power dissipation capacitance of an LCX device when it is switching. C_{PD} is used to roughly calculate dynamic power consumption.

Calculating LCX AC Power Consumption

- Static Power = Device Leakage
  @25°C 10 µA $V_I = V_{CC}$ or GND
  ±10 µA $3.6 \leq (V_I, V_O) \leq 5.5V$
- Dynamic Power (P_d)

$P_d = (C_L + C_{pd}) * V_{CC}^2 * f$

Typical Value of C_{pd} for LCX: 25 pF

C_L = Load capacitance at output
C_{PD} = Equivalent dynamic power dissipation capacitance
f = Switching frequency

Two factors contribute to dynamic power consumed in CMOS devices: capacitance (C_L and C_{PD}) and switching frequency (f).

This slide shows how power consumption for CMOS may be calculated.

The typical value of C_{PD} for LCX devices is 25 pF. If the switching frequency is 33 MHz and the capacitive load is 10 pF (times 8 outputs) then total dynamic power consumption at 33 MHz is:

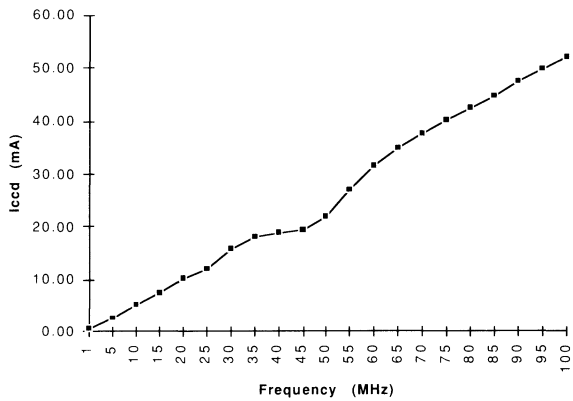
Pd = (25 pF + 8 * 10 pF) * (3.3V) *(3.3V) * 33 MHz

= 38 mW

As can be seen from the I_{CC} vs. f curves in a later chapter, LCX dynamic power consumption is among the lowest in the industry.

Note: C_{PD} is measured empirically.

LCX245 Dynamic I_{CC} vs Frequency

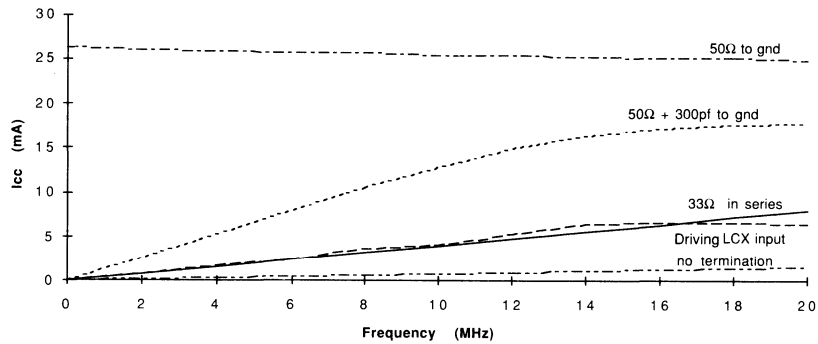


Vcc=3.3V, Temp=25C
A-Inputs=0V, 3.3V; B-Outputs=Unloaded

This graph shows the dynamic Icc of a typical LCX Octal device under no-loads condition. LCX245 consumes the least dynamic power among the alternate products (See comparison data at the end of this chapter).

LCX I_{CC} vs Termination

74LCX245 Icc vs Frequency for various terminations



Power dissipation in CMOS systems should be carefully considered.

At DC most terminating schemes do not drain current from the power supply. The exceptions are parallel termination and Thevenin termination (not shown here but almost identical to parallel termination).

AC current drain increases linearly with frequency for all but the AC termination, which rolls off at higher frequencies. Parallel and Thevenin terminations do not increase much with increasing frequency. Parallel and Thevenin terminations do, however, drain very large amounts of current across the entire bandwidth of the driver.

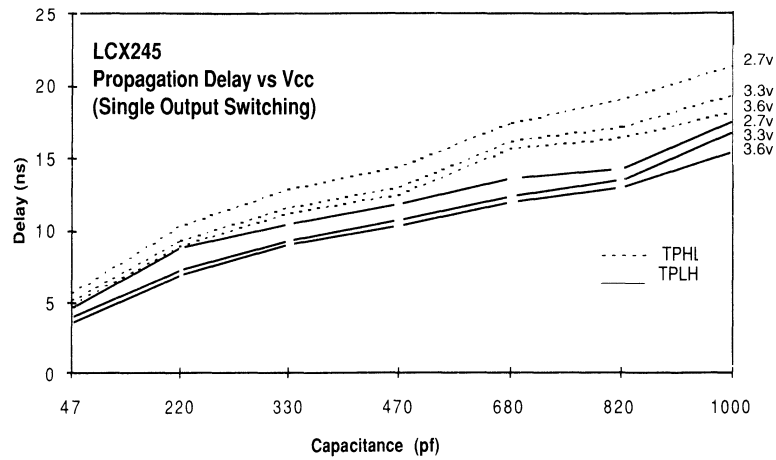
Power consumption and noise are usually the two main factors considered when choosing a termination scheme. For noise data and discussion regarding these termination schemes see Chapter 7.

Chapter 5
Speed Derating Curves

Speed Derating Curves

Although the speed (t_{PD}, t_{CLK}, etc.) of a logic device is specified in the datasheet for conditions which are usually worst case, the actual speed of a device in your system will vary depending on many conditions such as load, actual supply voltage, temperature, number of outputs switching. In most cases the datasheet specification represents the worst case and derating curves can be used to find out how much faster a device is likely to run in your application. (One notable exception is speed versus number of outputs switching. For historical reasons, the datasheet specification is usually for one output switching.) The rest of this chapter consists of speed related derating curves to illustrate LCX performance over a wide range of conditions. Other derating curves such as I_{CC} vs. frequency (Chapter 4) and output drive (Chapter 7) graphs appear in other chapters.

Propagation Delay vs C_L V_{CC}

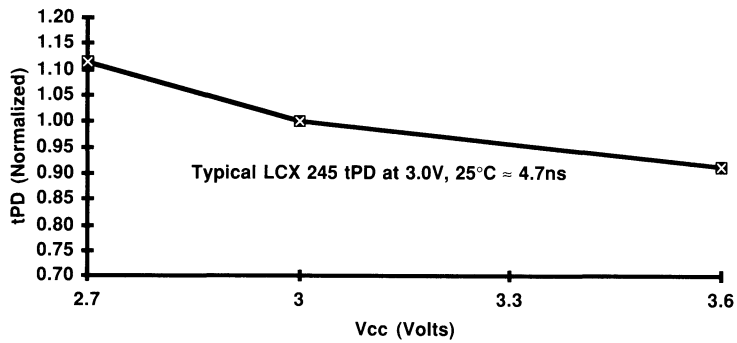


This graph shows how LCX performs with changes in V_{CC} and load capacitance.

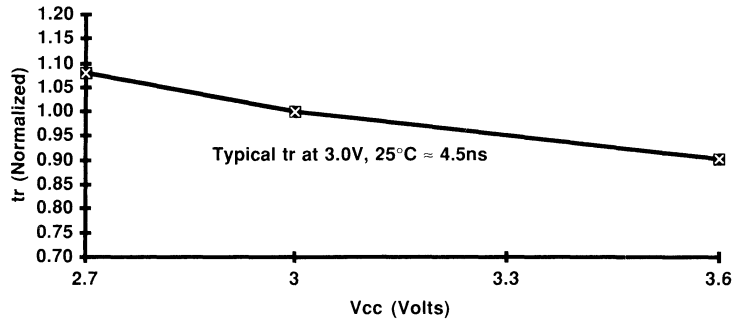
There is less than 1 nanosecond change from 2.7 volts to 3.6 volts V_{CC} with a 50 pF load.

Note the fairly linear change to the propagation delay over the 50 pF to 1000 pF range of load capacitance.

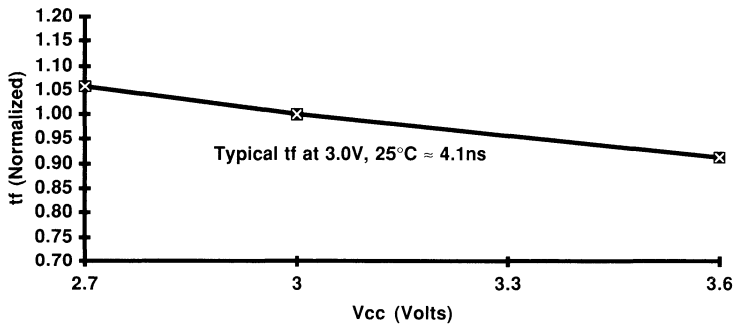
8-bit LCX t_{PD} vs. V_{CC}



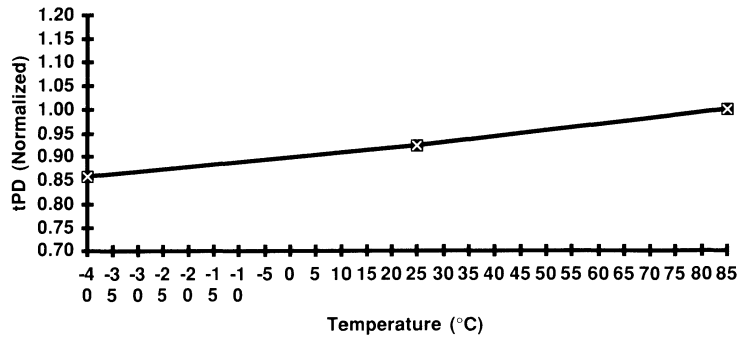
8-bit LCX t_r vs. V_{CC}



8-bit LCX t_f vs. V_{CC}

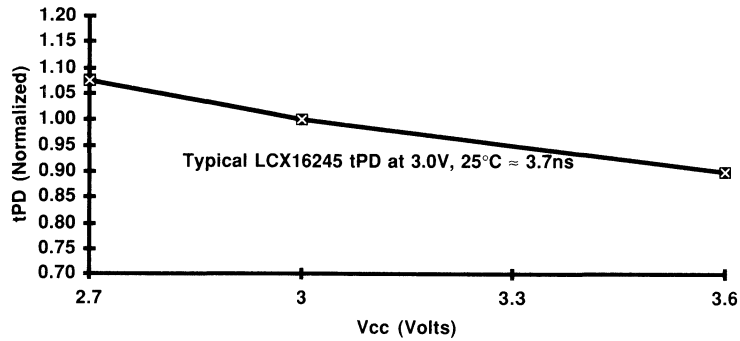


8-bit LCX t_{PD} vs. Temperature

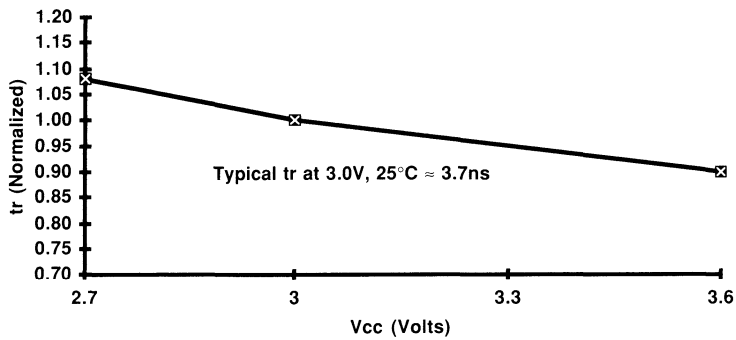


V_{CC} = 3.0V

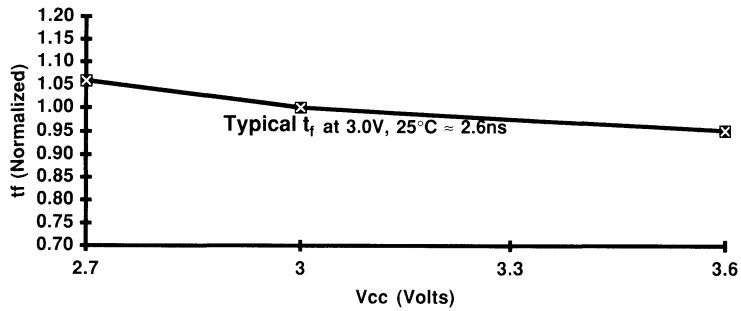
16-bit LCX t_{PD} vs. V_{CC}



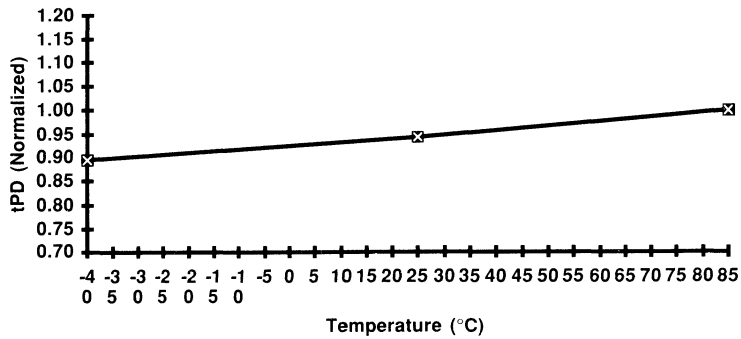
16-bit LCX t_r vs. V_{CC}



16-bit LCX t_f vs. V_{CC}



16-bit LCX t_{PD} vs. Temperature



V_{CC} = 3.0V

Chapter 6
Device and System Noise

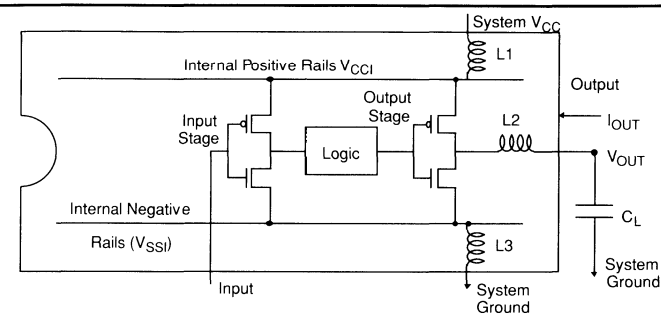
Device-Generated Noise In High-Performance Systems

Device-Generated Noise In High-Performance Systems

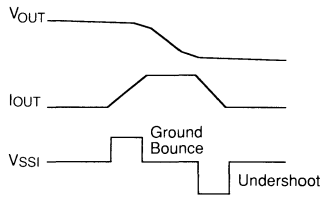
- Fundamentals of device-generated noise
- Examples of device-generated noise problems
- Test fixture noise vs system noise
- System-level design techniques to minimize device-generated noise
- IC design techniques to minimize device-generated noise

An understanding of device-generated noise phenomena is very important in the design of high-speed low voltage digital systems. A complete understanding requires knowledge of the sources of the noise as well as methods of solution.

Typical IC Device Noise Model



L1, L2, L3 Combination of die , bond wire , and leadframe inductance



$$I_{OUT} = -C_L \frac{dV_{OUT}}{dt}$$

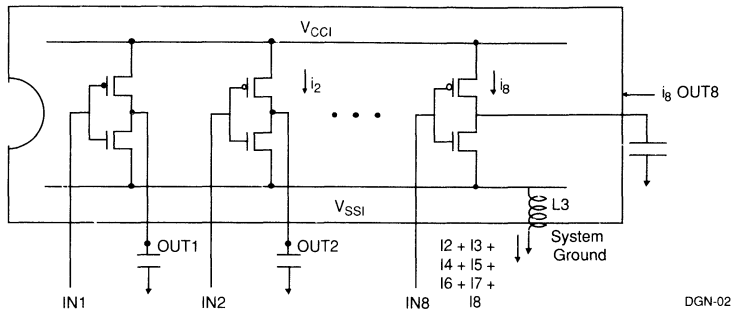
$$V_{SSI} = L3 \frac{di}{dt}$$

Similar phenomena on V_{CCI}

DGN-01

Disturbances on the internal supply rails of an integrated circuit can disrupt the normal operation of the circuit. The most dramatic disturbances generally occur as a result of charging and discharging load capacitance through parasitic package inductances. As the output capacitors present a very low impedance when turned on, they are capable of passing large current to and from such loads very quickly. The voltage developed on the internal supply rails across the parasitic package inductances can be far from negligible. As the input threshold of a gate is referred to these rails, the effective input threshold of the integrated circuit as seen by the outside world can be changed dramatically. In addition, output stages that are hard on and hard off will follow a bouncing internal ground or power rail respectively.

Multiple Outputs Switching

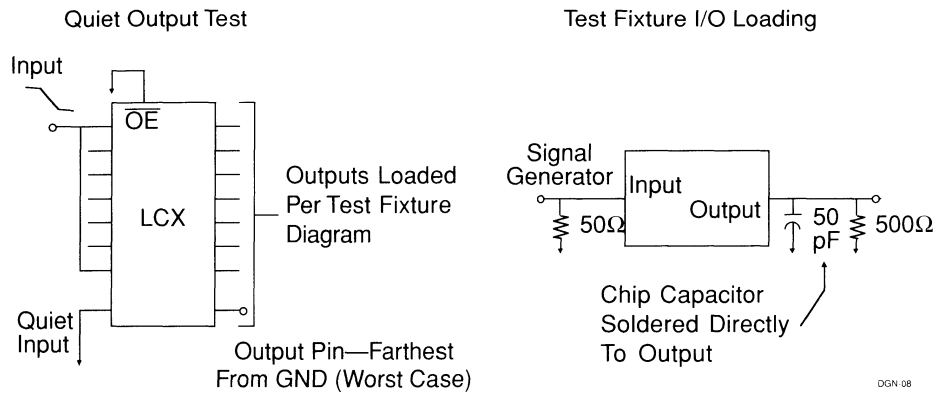


- Simultaneously switching outputs 2 thru 8 causes a large di/dt transition in L3, causing large V_{SSI} spike
- Assuming N-channel pull-down on OUT1 is ON, OUT1 follows V_{SSI} excursions

A case in point is the simultaneous switching of seven of eight output stages on a typical octal circuit, while the eighth output is "quiet." Discharging all seven loads through the ground inductance creates a worst-case spike on V_{SSI} which can exceed a volt on some cases! This can cause the "quiet" output to rise more than a volt while supposedly low. At the same time, the input thresholds of all the input stages will rise dramatically, possibly causing a glitch or oscillation at the outputs.

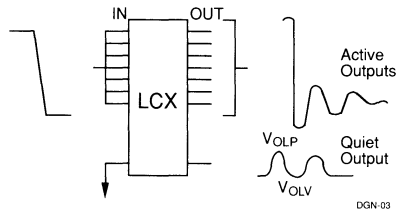
The ground-side manifestations of these phenomena are usually of greatest interest because device-generated noise generally is of greatest concern when driving TTL inputs whose input thresholds are at less than half of the positive rail in five volt systems. Similar phenomena are experienced on the internal V_{CC} rail

Test Fixture Ground Bounce



A typical low voltage CMOS octal part, the LCX was tested in an industry-standard test fixture, with lumped capacitive loading, and generated ground bounce of ≤ 0.8 Volts on the "quiet" output.

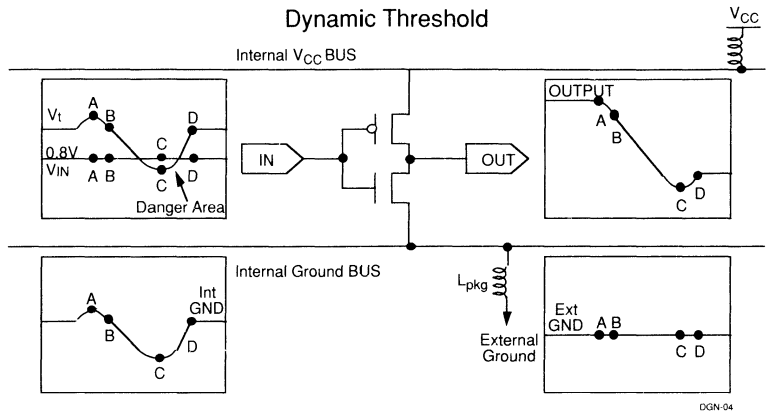
Device Noise



- Ground bounce can be observed by switching seven outputs and monitoring the quiet output
- V_{OLP} - Peak voltage on quiet output
- V_{OLV} - Maximum undershoot on quiet output

V_{OLP} and V_{OLV} are two primary indicators of device-generated noise performance. V_{OHP} and V_{OHV}, the positive rail counterparts of V_{OLP} and V_{OLV}, are generally of less concern because of higher noise margins in the HIGH state.

Device Noise



- The threshold of a gate is referenced to Internal Ground
- Ground bounce appears to the input as a change in its switching threshold (V_t)
- Danger area occurs when the threshold dips below the voltage on the input (V_{IN})

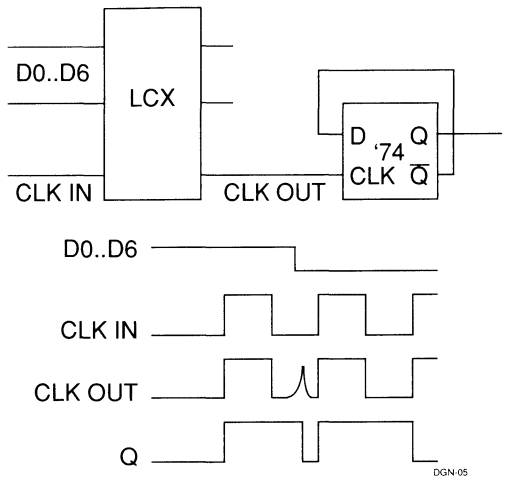
Dynamic threshold shift is the third indicator of device-generated noise performance. While a V_{ILD} failure is shown here, transitions of Vt above 2.0V can be just as serious.

When Are These Phenomena An Issue?

- Ground bounce can cause asynchronous systems to change state when they are not supposed to
- Undershoot magnifies crosstalk, ring, and EMI problems, and stresses downstream input stages
- Dynamic threshold shifts create a variety of problems:
  - Reduced noise margin
  - Glitches in asynchronous and synchronous circuits
  - State changes in asynchronous circuits
  - Oscillations

All three types of device-generated noise can cause problems in a system. By understanding the different problem areas and failure mechanisms, the systems designer can put himself/herself in a better position to address the issue effectively.

System Noise Effects

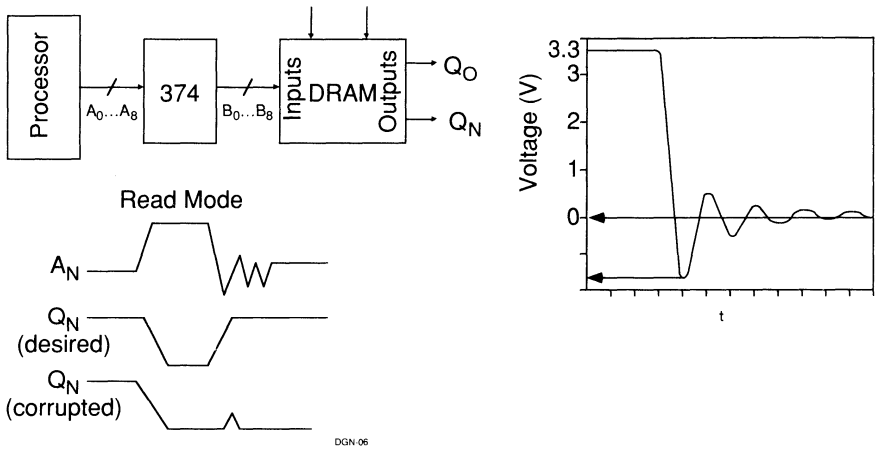


During output switching, noise is generated on otherwise quiet outputs. If the receiver input is an asynchronous input, the noise may be interpreted as a valid signal. In this example, ground noise generated while D0..D6 switch, incorrectly generates a clock on the flip-flop. The Q output is then corrupted.

Asynchronous systems are particularly vulnerable to device generated noise problems, because a short glitch at the output of a device can be interpreted as a valid transition by a down stream device. This is particularly true of clock distribution circuitry.

System Noise Effects

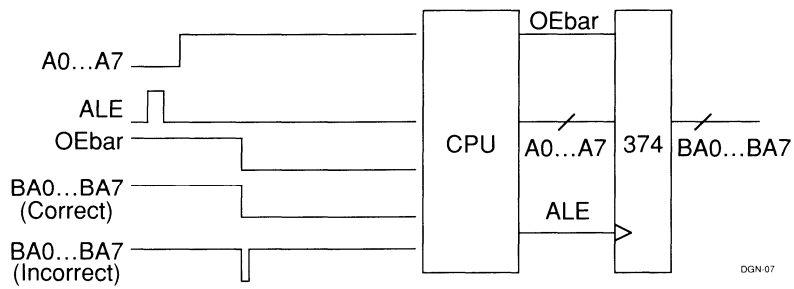
Undershoot and Ringing



Certain circuit configurations are sensitive to overshoot and undershoot at their input stages. A case in point is a typical dynamic RAM. Some dynamic RAM implementations are very sensitive to undershoot, and may lose or corrupt data when inputs are driven too far below the ground rail.

System Noise Effects

- Ground noise is generated when outputs are enabled
- Outputs BA0 - BA7 should switch LOW
- If the ALE input level is above the dynamic threshold of the '374, then a HIGH level is clocked into the part, and the outputs switch HIGH (incorrect)



A typical dynamic threshold problem involves a "quiet" input which gets confused when its input threshold changes due to a bouncing supply or ground rail, causing the state of a latch or flip-flop t change erroneously.

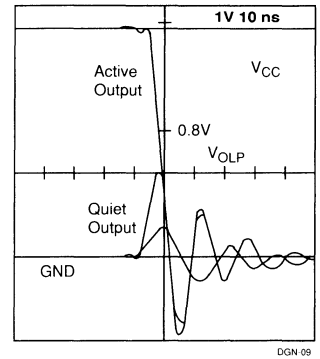
Test Fixture Noise vs System Noise

- Test fixture load capacitance is a lumped capacitance
- System load capacitance is a capacitance distributed along a transmission line
- Device loaded with lumped capacitances exhibit worst-case levels of device-generated noise
- Devices loaded with distributed capacitances exhibit 50% less device-generated noise than devices with lumped load capacitances
- Characteristic inductance and capacitance of a transmission line, as well as the distribution of the load capacitance, has a dramatic effect on device-generated noise levels
- Any termination on the system transmission line will also drain switching current from the load capacitances

Even though device-generated noise levels can be high in a system, they will be much higher in a test fixture environment. The reason for this is that the test fixture environment is optimized for discharging large capacitive loads quickly, exactly the thing that causes large noise levels. While the test fixture environment provides a convenient way to perform uniform characterization of parts, it provides very pessimistic evaluation of noise performance. For this reason, all noise specifications should be considered absolute worst-case estimates.

Test Fixture Ground Bounce

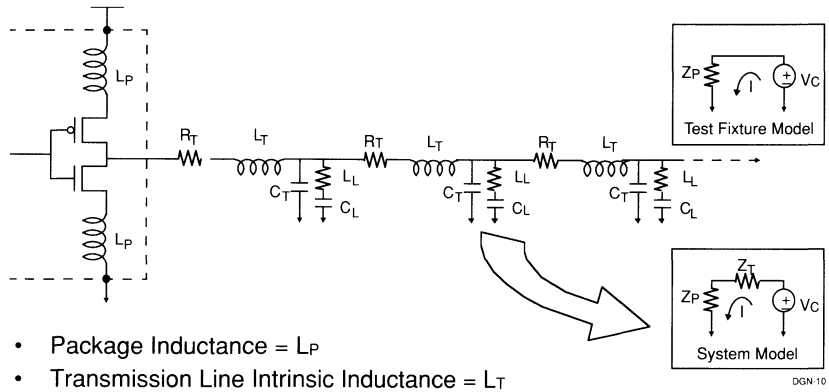
Standard Test Setup



Seven Outputs Switching
V_{CC} = 3.3V C_L = 50pF
Worst-Case Output Pin

This is not LCX!

System Transmission Line With Distributed Loads



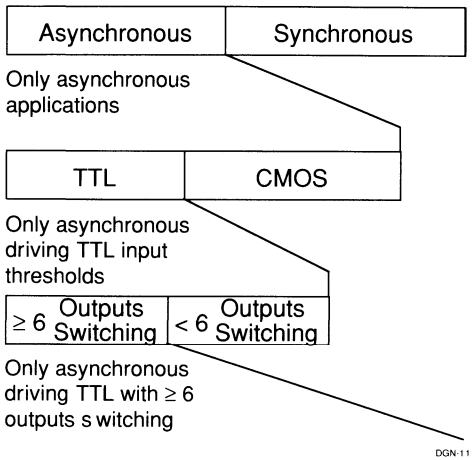
- Package Inductance = L_P
- Transmission Line Intrinsic Inductance = L_T
- Transmission Line Intrinsic Resistance = R_T
- Transmission Line Intrinsic Capacitance = C_T
- Load Inductance = L_L
- Load Capacitance = C_L

This slide illustrates the model for a typical system. The most important difference between a test fixture and a system is the distributed loading of a system's transmission line. The net effect is a lower capacitive load on the output of the driver resulting in much lower ground bounce levels.

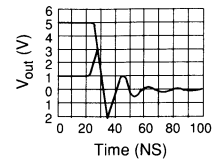
Addressing The Device-Generated Noise Issue

Both the user and the integrated circuit vendor can address the device-generated noise issue. By applying the product properly, and by knowing when it's necessary to take extra precautions, the user can effect significant improvement in device-generated noise performance. By improving the product, the vendor can add substantially to this improvement.

Locate Problem Areas



Outlet output and Falling edge



DGN-11

Input Switching Requirements
CMOS 2.9V for 2ns
TTL 1.7V for 2ns

Number of Outputs Switching	System Bounce
3	0.4V
4	0.54V
5	0.67V
6	0.8V
7	0.92V

A very important point is that device-generated noise is only a problem in a few applications areas. Because noise levels are quite low when less than six outputs change state simultaneously, octal/16-bit parts are the major problem area. Indeed, even with octal/16-bit parts the noise levels are generally not a problem unless TTL input levels are involved. The first step in addressing this issue is to locate potential problems.

System-Level Techniques

USE GOOD LAYOUT TECHNIQUES

- Use multilayer boards with homogenous supply planes
- Avoid sockets
- Decouple each device with a 0.1 µF capacitor - Place capacitor properly
- Keep power and ground connections as short as possible
- Remember that outputs near ground can be up to 50% quieter than those far from ground
- Use board design practices which reduce any additive noise sources such as crosstalk, reflections, etc.
- Use surface-mount technology

The techniques used to combat device-generated noise all have one goal: to limit the inductive reactance between the system supply planes and the internal rails. Any inductance in series with the supply and ground pins adds directly to the parasitic package inductances and increases noise levels. Careful attention to details can improve performance significantly.

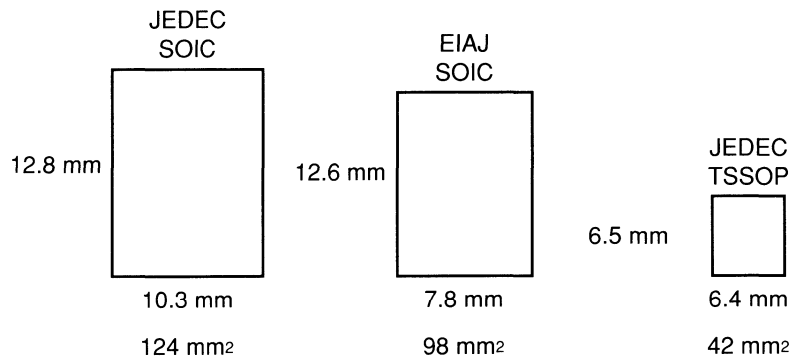
How Can The Vendor Reduce Ground Bounce?

- Reduce package inductance by reducing package size
- Output waveshaping techniques

Anything that can be done to reduce the inductance of the supply and ground pins will reduce device-generated noise.

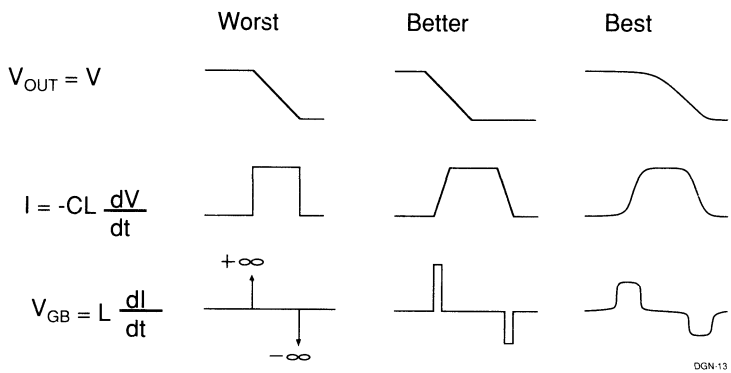
Package Footprint

20-Lead Surface Mount Package Footprints



For example, by switching to a smaller package size, not only will this help reduce the inductance of the supply and ground pins, the board area required by a given circuit can be reduced by as much as 66%.

Design Techniques To Minimize Ground Bounce

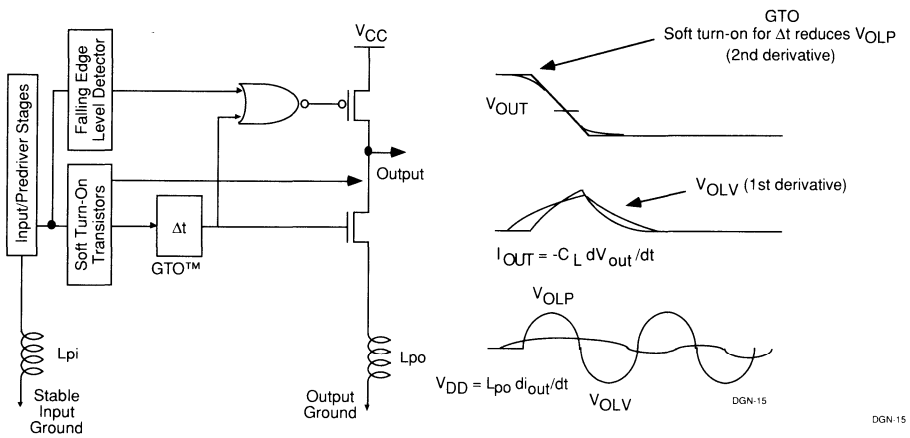


Ground bounce magnitude is governed by the size of the load capacitor, the parasitic inductance of the ground pin, and the abruptness with which the output stage turns on. Undershoot is similar, except that the abruptness with which the output voltage stops changing is important there. By limiting the abruptness of the voltage transitions of the output, the vendor can go a long way toward limiting device-generated noise.

LCX Noise/EMI Reduction

The LCX family addresses the device-generated noise issue on two fronts: 1) gradual turn-on of the output stage to reduce ground bounce; 2) offering smaller footprint packages that have reduced ground bus inductance.

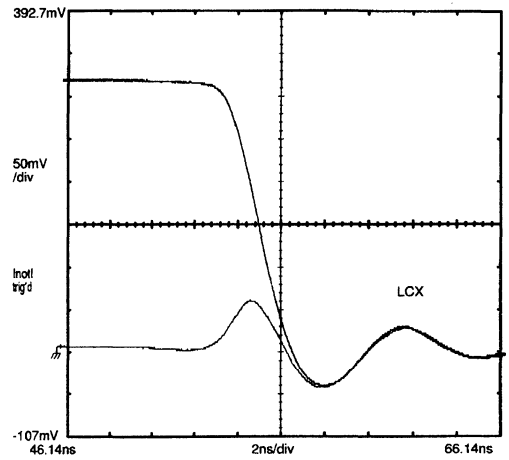
LCX Output Control



Circuitry in the output stage greatly improves noise performance. A Gradual Turn-on Output buffer (GTO™) rounds the initial high-to-low transition of the output buffer by staggering the turn-on of the N-channel output transistors. Small N-channel transistors are initially turned on to initiate the transition. After a short delay, the largest transistors are turned on. The softer transition improves V_{OLP} dramatically.

In a standard CMOS output buffer, when the load is almost discharged, the current through the ground inductor starts to fall off. This di/dt transition induces a negative voltage across the ground inductor.

LCX Quiet Series™ Circuitry



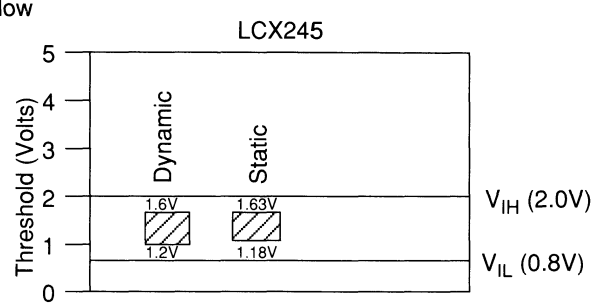
Note: Vertical scale is reduced by 10x

The results are impressive: Lower V_{OLP}'s and V_{OLV}'s and less ringing.

LCX products feature <0.8V typical V_{OLP}.

Typical Dynamic Threshold

- DC input specs require thresholds to be within 0.8V - 2.0V window
- DC input voltages are LCX245 valid logic levels outside of 0.8V - 2.0V window

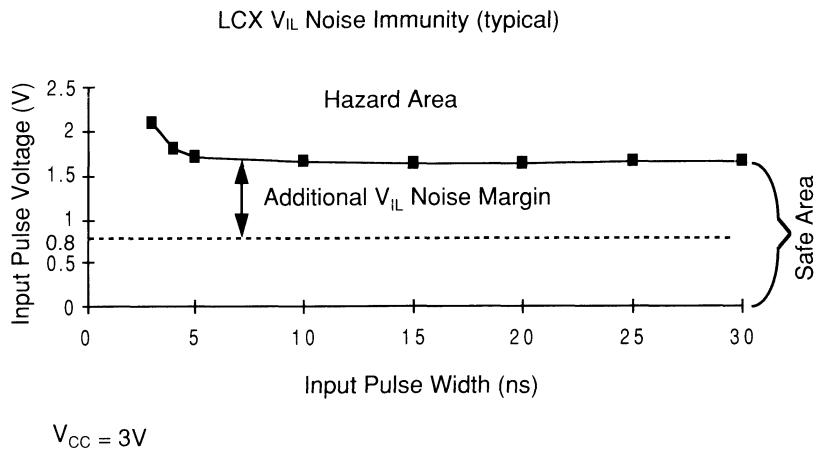


V_{CC} = 3.0
Temperature = 25°C
Output Loading 50 pF/500Ω

DGN-18

The LCX family with dynamic thresholds are so close to the static threshold that they remain within the TTL static threshold window.

Typical LCX V_{IL} Noise Immunity

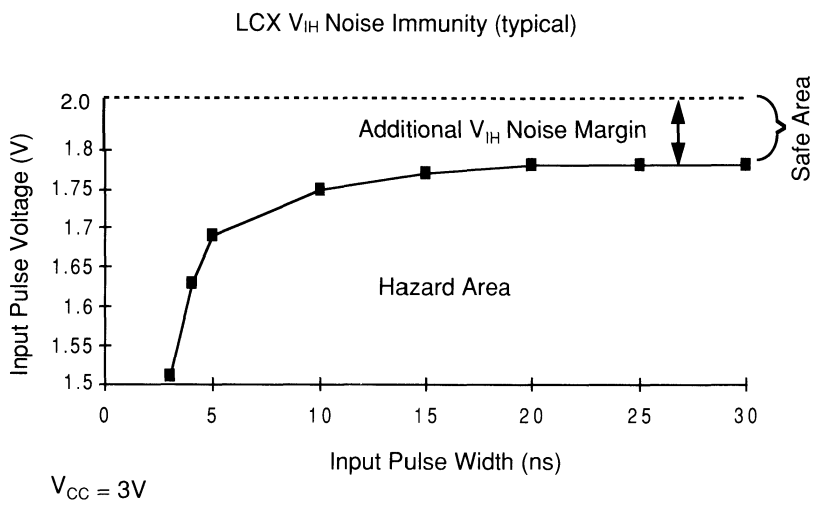


Noise immunity is excellent for LCX as this slide shows.

Noise immunity is a measurement of the duration and amplitude of a noise pulse necessary to cause an invalid level of output.

A square wave form is generated with V_{IL} =0 and V_{IH} = 0.8V with a fixed pulse width. Then V_{IH} is raised until the corresponding output no longer sustains its valid logic level. This exercise is then repeated with different input pulse widths.

Typical LCX V_{IH} Noise Immunity



For V_{IH} Noise Immunity measurement, the exercise is similar to V_{IL}. $V_{IH} = V_{CC}$, V_{IL} starts at 2.0V and then is lowered down until the correponding output no longer maintains its valid logic level.

Device-Generated Noise Summary

- Device-generated noise is the result of load capacitances discharging through IC package and chip inductances
- Effects small application segment: LCX octal switching asynchronous signals into TTL-level inputs
- Device-generated noise levels in a system are 50% less than device-generated noise levels in a test fixture due to transmission line effects
- Significant device-generated noise reduction can be obtained through new IC design techniques
- The LCX family reduces device-generated noise by implementing the GTO, exclusive to National Semiconductor
- Minimizing device-generated noise also minimizes other system-generated noise such as EMI crosstalk

Through an understanding of device-generated noise phenomena, and with a little help from the integrated circuit vendor, the system designer can improve the performance and reliability of the final product.

Electromagnetic Interference

Electromagnetic Interference

EMI/RFI

- Electromagnetic interference
- A phenomenon by which electric and magnetic fields combine to create radiated and conducted interference of transmitted/ received data or communications signals

Like crosstalk, EMI is noise that is radiated or conducted via electric and magnetic fields. Since direct contact between the source and receiver is not necessary to transmit or receive this type of noise, it is more difficult to identify and debug.

This section will first review some EMI basics and then describe the role of high-performance logic in the generation of EMI. Several design recommendations for low-noise, high-performance systems will conclude this section.

EMI

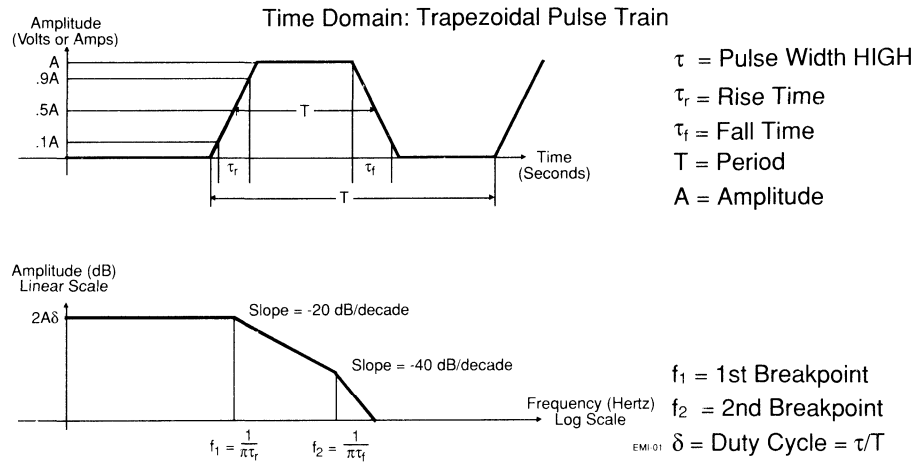
EMI generation is a function of:

- Signal characteristics: switching frequency, duty cycle, edge rate, noise content, and voltage levels
- Signal current loop area
- Radiation efficiency of the geometry of the current loop

The two major factors affecting EMI generation are the frequency content on potential radiators in the system and the efficiency of those radiators.

The first factor is determined by the wave forms propagated within the system. The second factor is determined by the geometry of transmission lines, circuit boards, connectors, and enclosures.

Time Domain To Frequency Domain Conversion



To best understand EMI, the observer must be some-what fluent in converting from the time domain to the frequency domain.

As an exercise in EMI prediction, a basic trapezoidal pulse train is illustrated in the time domain. Parameters that will be used to approximate the frequency responses include the amplitude, rise/fall time, duty cycle, and period.

The lower curve illustrates the approximation of the upper boundary of the frequency spectrum. The break points are calculated using the rise/fall time pulse width, and the period of the time domain signal. Once the upper bound approximation is complete, superimposing the fundamental frequency and its harmonics, as well as any noise (ringing) on the signal, will yield the frequency envelope in which EMI generation may be expected. The lowest frequency that may radiate is the fundamental. The highest frequency that may radiate is that at which the upper bound crosses the ∅ dB axis.

As the rise/fall time decreases and /or the pulse width decreases the frequency envelope increases to higher frequencies and radiated wavelengths decrease.

PCB Trace Far-Field Radiation

$$E = \frac{i\,\ell\,\pi f}{5r} \quad \sin\left(\frac{2\pi t}{\lambda}\right)^{*}$$

i = current in line	f = frequency
ℓ = line length	λ = wave length
t = PCB thickness	r = distance from the line

- For short lines, E is proportional to ℓ
- For lines longer than $\frac{\lambda}{4}$ substitute $\frac{\lambda}{4}$ for ℓ

*See EMI CONTROL by White and Mardiguian

Theory suggests that the magnitude of the electric field at distances greater than $\lambda/2\pi$ is proportional to the length of the line.

Radiation of high-frequency harmonics can be reduced in some cases by minimizing line length.

Design Recommendations—Device Level

- Round output waveform edges
  Sharp edges contain high-frequency components
- Minimize output voltage swing
- Eliminate device-generated ringing
  This noise contains many high-frequency components
- Minimize ground bus inductance
- LCX solves these issues with the implementation of the GTO™ circuitry

The following several slides list recommended guide-lines in designing with high-speed logic for highest performance and lowest noise.

On the logic IC level several design improvements have improved signal quality. The outcome is less device-generate noise on the signal lines as well as a change in some of the key signal characteristics that generate EMI.

LCX implements several design improvements intended to minimize device-generated noise. One of the benefits of these design improvements was the effect these improvements had on the signal characteristics that are involved in generating EMI.

Design Recommendations—Board Level

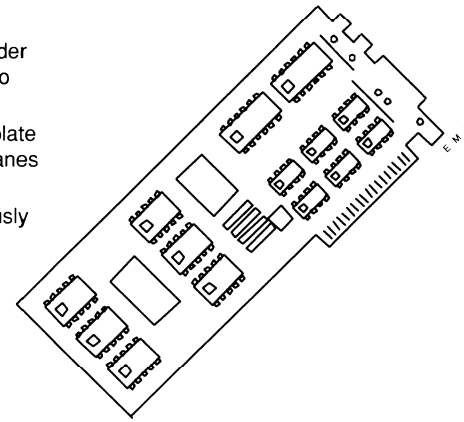
- Use multilayer circuit boards
- Use power and groundplanes. Avoid power and ground traces
- Avoid using wirewrap boards—they offer no EMI shielding

At the printed circuit board level many techniques are available to minimize system noise. The reduction of overall system-generated noise will have a very positive effect in minimizing EMI.

In designing with state-of-the-art IC technologies, it is important to use state-of-the-art board design to gain the highest performance available.

Design Recommendations—Board Level

- Avoid using sockets
- For through-hole technology solder power and ground pins directly to the power and ground planes
- For surface mount technology, plate through to power and ground planes as close to device as possible
- Minimize number of simultaneously switching outputs
- Use terminations to eliminate reflections and ringing
- Minimize crosstalk



Board design techniques that minimize system-generated noise such as crosstalk and reflections will also go a long way towards minimizing EMI. Reduction of device-generated noise will also minimize EMI.

Design Recommendations—Power Distribution

- Decoupling is vital to eliminating problems from power supply coupled noise
- Use tantalum or aluminum electrolytic capacitors in the power supply distribution network
- Use low ESR multilayer ceramic capacitors to decouple the power supply where it enters the board 1 - 10 µF are recommended values
- Use low ESR multiplayer ceramic capacitors to decouple every IC package

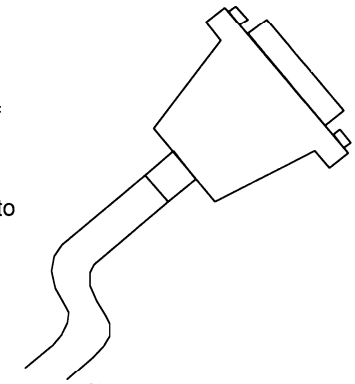
  0.1µF is the recommended value

Out of all the sources of energy in a system, there is no other more widespread than the power distribution network. True, power supply manufacturers have made inroads in reducing the noise in the power supply as well as on the power supply outputs. The techniques used in the distribution of this power within a system will also have a major impact on the noise overhead within that system.

The two key fundamentals to remember are 1) keep power distribution impedance to a minimum; and 2) provide adequate decoupling at every level of the distribution network.

Design Recommendations—System Level

- Use multilayer backplane boards
- Use twisted pair or coax cables if using wirewrap backplanes
- Use multiple power and ground connections from the backplane to the circuit board to minimize connection impedance
- Use care in shielding I/O cables. Insure that they are tied to the chassis ground with a low impedance connection



EMI-03

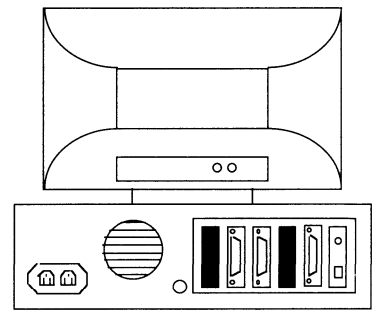
The proper low-noise design techniques used at the board level should be used at every level of the system design.

On the system level, connections from one part of a system to another must be made with the optimal amount of shielding and the lowest possible impedance.

Proper grounding of shields to chassis ground will ensure maximum shielding. Knowing the cost of shielding, losing the effect of that shielding due to improper grounding can be a frustrating, costly over-sight. Attention to proper grounding can either make or break a low-noise, high-performance system.

Design Recommendations—Enclosure Level

- Use shielded I/O cables whenever possible
- Minimize the number and size of any openings in the system enclosures
- Ensure that all openings and access panels are properly shielded
- Ensure that the recommended pressure is applied to shielding gaskets and brushes, per manufacturer


EMI-04

The system design is completed at the enclosure level or back-end. The same low-noise guidelines must be followed up to and including this level of design. Openings in an enclosure can act as antennae. Minimizing the size of these openings can reduce EMI levels.

Even cracks in the system's enclosure can radiate EMI. Using shielding gaskets and brushes will shield these cracks from radiating EMI to the outside world. Manufacturers of these types of shielding often hold seminars and publish technical information on the various types of shielding.

EMI Summary

- EMI radiation is a function of signal and antenna characteristics
- Most EMI is radiated by long signal traces and I/O cables
- Major causes of EMI problems are improperly shielded or grounded I/O cables
- Good system design rules will minimize EMI and overall system noise

System-generated noise and device-generated noise are very interactive. Design techniques intended to minimize one may have a very positive effect on minimizing others. The cost in debugging and redesigning a system to meet FCC regulations or to eliminate intra-system noise that may be causing system faults far outweighs the cost of using prudent and effective design techniques on the first pass.

Power Distribution and Decoupling

Why Is Power Distribution An Issue?

- Minimizing power grid impedance will reduce V_{CC} droop
- Proper decoupling will reduce V_{CC} droop
- Reducing supply noise improves noise margin
- Proper decoupling reduces device-generated noise

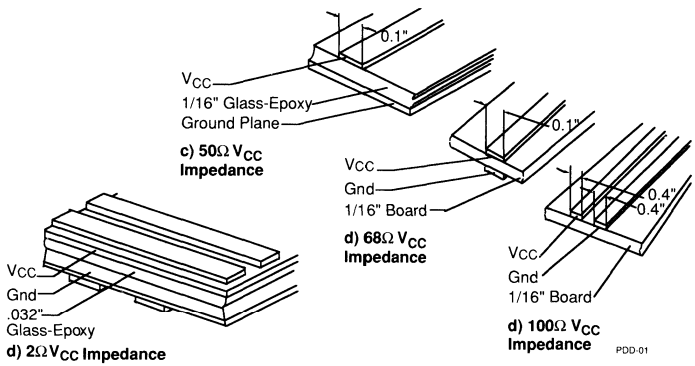
In today's high performance systems, minimizing noise in the power distribution network is critical. The power distribution network is critical. The power distribution network covers the entire system. Any noise in this network can have adverse effects in system performance, either at the source of the noise or elsewhere in the system. Careful consideration of some basic guidelines can avoid these problems.

Minimum power grid impedance and proper decoupling will have a very positive effect in reducing V_{CC} droop.

The benefit of a reduction in power supply noise is an increase in noise margin.

In addition to a reduction in V_{CC} droop, proper decoupling will also reduce device-generated noise.

Evolution of Power Distribution Schemes



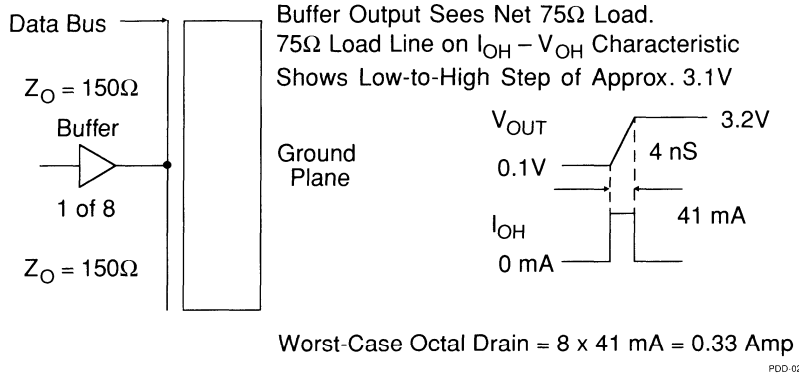
Techniques for distributing power within a system have gone through a considerable evolution.

Early printed circuit boards were one-sided affairs with power and ground traces intermixed with signal traces. These narrow traces resulted in V_{CC} impedances on the order of 100 ohm.

The use of two-sided boards allowed the placement of V_{CC} and ground on separate sides. This eventually led to a ground plane. The impedance of V_{CC} was cut in half as compared to the one-sided board.

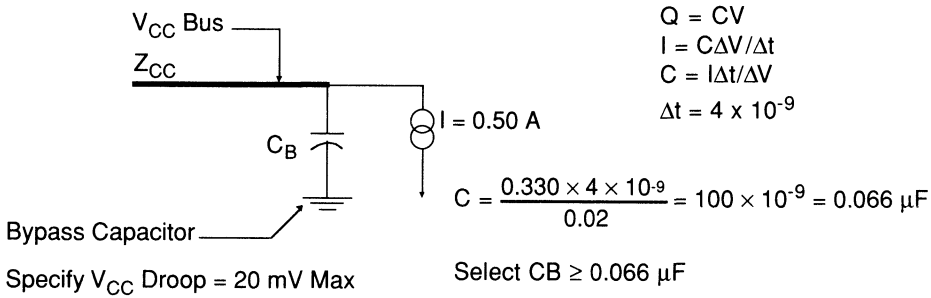
Today's high-performance circuitry requires that the board designer use three or more layers. This allows the use of a V_{CC} plane as well as a ground plane and results in a V_{CC} impedance of 2 ohms or less.

Octal Buffer Driving Bus



Best-case, under typical loading conditions, an LV logic output can swing 3.1 volts in less than 4 ns. Into an equivalent 75-ohm load, this voltage swing translates into a 41 mA current pulse on each output. For an octal device, this translates to a current spike on V_{CC} of 330 mA.

V_{CC} Droop



$Q = CV$
$I = C\Delta V/\Delta t$
$C = I\Delta t/\Delta V$
$\Delta t = 4 \times 10^{-9}$

$$C = \frac{0.330 \times 4 \times 10^{-9}}{0.02} = 100 \times 10^{-9} = 0.066\ \mu F$$

Select CB ≥ 0.066 µF

Place one decoupling capacitor adjacent to each package

PDD-03

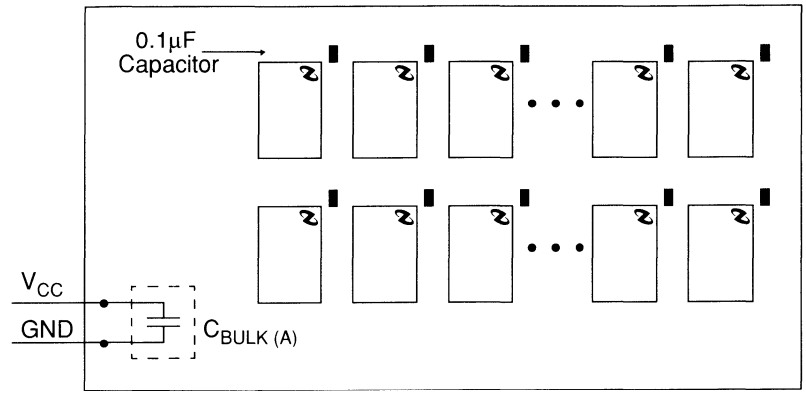
Adequate decoupling capacitance must be chosen in order to satisfy the 300 mA current requirement of V_{CC} without creating a large voltage droop on the V_{CC} plane.

The calculation of the minimum decoupling capacitance requirement is illustrated here.

Assuming a design requirement of 20 mV maximum V_{CC} droop, a 300 mA pulse of 4 ns requires a minimum of 0.066 µF of decoupling capacitance.

To ensure that current transients on the V_{CC} plane are minimized, one decoupling capacitor should be placed adjacent to each package. The impedance of these decoupling capacitors should be minimized as well. The use of chip capacitors, soldered as close to either V_{CC} or ground pins as possible, is recommended.

Board-Level Decoupling Capacitor



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typical used (50-100 μF)

In addition to the localized decoupling at the chip, a bulk capacitor must be placed on the board. Continuing with the example of the last slide, consider multiple chips switching at the same time or at slightly different times. The 20 mV V_{CC} ripple generated by a single IC's can lead to unacceptable levels of V_{CC} noise. This is typically remedied by placing a relatively large electrolytic, 100 μF, near the power entry point to the board.

Crosstalk

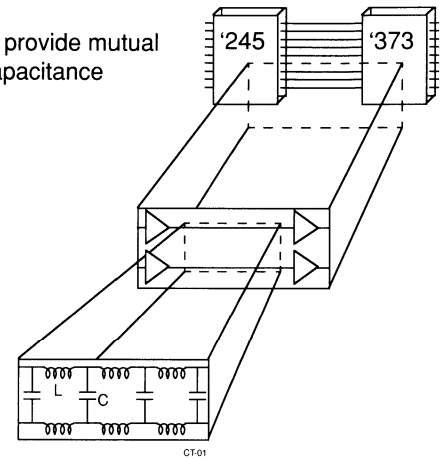
What Is Crosstalk?

- Crosstalk is a system-level noise phenomenon in which energy is inadvertently coupled from an active part of the system into an adjacent part of the system
- Crosstalk reduces system noise margin

The coupling of energy from one section of a circuit to another section is called cross talk. Crosstalk adds directly to other system noise phenomena, reducing overall system noise margin.

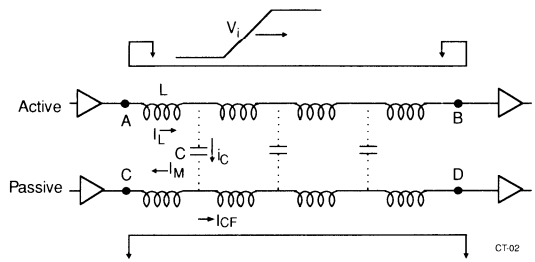
Where Does Crosstalk Take Place?

- Two parallel signal lines provide mutual inductance and shunt capacitance

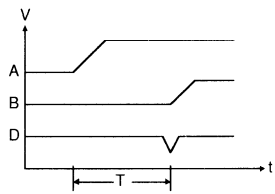


Unshielded lines in any system are at least loosely coupled to neighboring lines through parasitic capacitances and mutual inductances. The closer any two lines are, the tighter the coupling between them. Adjacent printed circuit board traces and unshielded lines in bundles are prime candidates for crosstalk.

Forward Crosstalk



- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -C\ dV_i/dt$
- Mutually Induced Current = $I_M = mI_L$
- Forward Crosstalk Current = I_{CF}

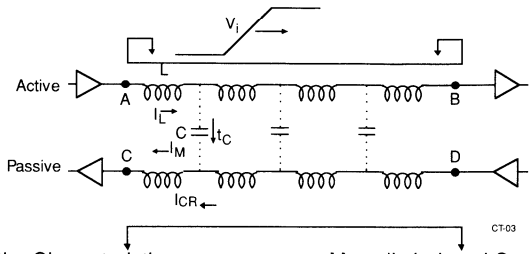


As the active signal, V_i, propagates from A to B ...

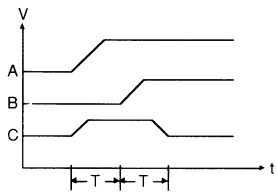
... a negative-going spike, V_f, propagates from C to D, coindident with V_i

At any given instant, crosstalk current is only coupled into a passive line from the areas on the active line at which wavefronts exits. Capacitively coupled current splits on the passive line. Some of it travels in the direction of the propagating wave and some of it travels in the opposite direction. Mutually induced current, which is generally much larger in magnitude, travels in a direction opposite to that of the progressing wavefront. Thus the total current in the passive line which is traveling in the same direction as the active wavefront is negative spike is called forward crosstalk.

Reverse Crosstalk



- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -CdV_i/dt$
- Mutually Induced Current = $I_M = mI_L$
- Reverse Crosstalk Current = I_{CR}

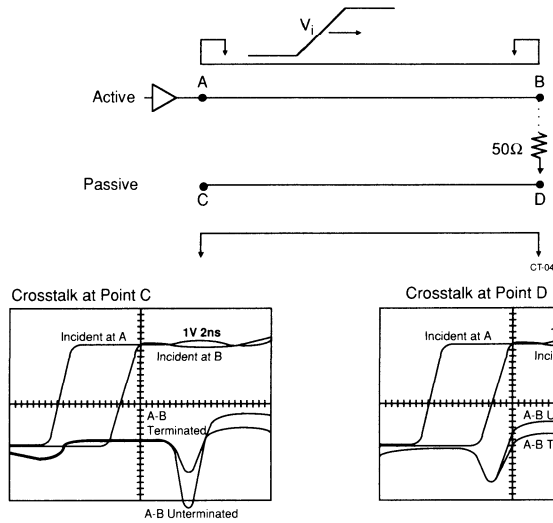


As the active signal, V_i, propagates from A to B ...

... a positive pulse appears at C for a duration twice the coupled line delay T

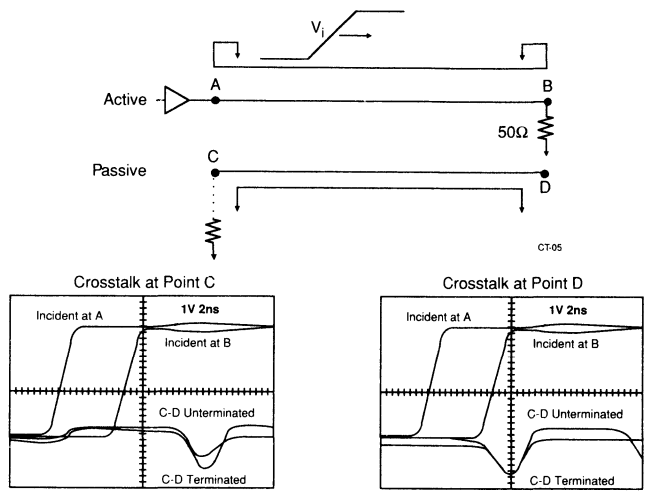
Crosstalk current traveling in a direction opposite to the active wavefront is positive. As the wave propagates down the active line, reverse crosstalk current is pushed into point C, thus raising the line until the active wave front reaches point B. At this point, crosstalk current requires time T to reach point C, so the total duration of the voltage rise at point C is 2T.

Effects Of Termination On Crosstalk



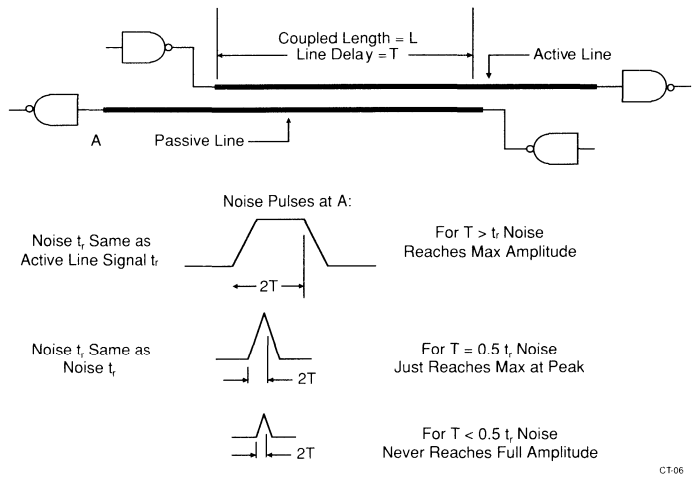
Properly terminating the active line reduces reflections on it, thus reducing or eliminating wavefronts on the active line which would contribute to crosstalk to the passive line.

Effects Of Termination On Crosstalk



Properly terminating the passive line reduces reflections of crosstalk signals on the passive line, improving overall system noise margin. Good transmission line matching is an easy way to improve many aspects of system performance.

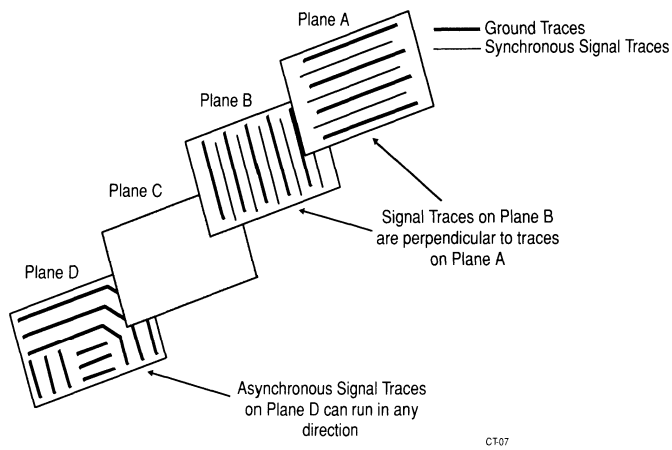
Partially Coupled Lines



The relationship between the transition time and the electrical length of the coupled section of the lines affects the magnitude of the crosstalk. If the lines are only in close proximity for an electrical length which is comparable to the transition time, the reverse crosstalk pulse may be reduced in duration or amplitude.

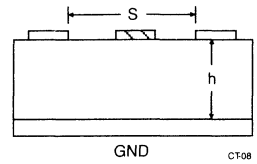
Recommended Crosstalk—Avoidance Structure

- Synchronous Signal Plane
- Synchronous Signal Plane
- Ground Plane
- Asynchronous Signal Plane



Careful circuit layout can reduce crosstalk noise considerably. An all-out approach is to separate traces on different layers of the printed circuit board by function. Synchronous signals which could interfere with each other are run perpendicular to each other on adjacent PCB planes. Ground traces between parallel traces on a given plane kill parasitic inductance and capacitance, killing crosstalk. Separating sensitive asynchronous circuitry from the synchronous circuitry with a ground plane is very effective.

Recommended Crosstalk—Avoidance Structure



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace ▨ between signal traces
- Minimize distance h to keep line impedance low

On printed circuit boards, the biggest factor in reducing crosstalk is to minimize coupling by keeping parallel traces as short and as far apart as possible.

Crosstalk Summary

- Crosstalk results from parasitic inductance and capacitance between adjacent PCB traces
- Reverse crosstalk is generally of greater concern
- Proper termination reduces crosstalk
- Good layout techniques reduce crosstalk

A little preventive medicine can go a long way toward reducing crosstalk problems and improving system reliability.

Device and System Noise Summary

- Advanced LCX logic interfaces easily with other logic technologies
- Attention to transmission line effects will improve performance of LV CMOS logic systems
- Careful consideration of PCB geometry will improve system noise margin by reducing crosstalk
- Selection of good power distribution and decoupling techniques is essential for high-performance, low-noise systems
- Device-generated noise can be reduced by both good system design technique and IC vendor design improvements, such as GTO
- Adherence to proper system design rules will minimize spectral content as well as most other types of system-generated noise and device-generated noise

In summary, Chapter 6 of the LCX Designer's Guide has shown that design with high speed LV logic, especially LCX is not difficult. A little discipline and adherence to some basic guideline will allow a designer to maximize the performance of a system with the use of high-speed logic.

Chapter 7
Line Driving and Termination

Terminations For LV Logic

WHY SHOULD LV LOGIC USERS CONSIDER TERMINATION?

- Improper matching of source and load to a transmission line can cause extra delay, ringing, and unacceptable voltage excursions on the line
- These effects degrade system speed and noise performance
- The high speed and even the drive capability of LV logic can make even short lines look like transmission lines
- Proper termination techniques will reduce system power consumption

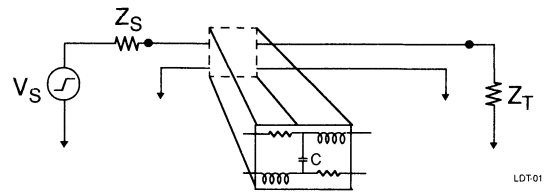
As Low Voltage (LV) Logic system designers become familiar with low voltage high speed logic, one thing becomes clear; the output edge rates are still very fast. ECL system designers are already well versed in the use of logic with very fast edges rates. In either case careful considerations must be made in determining if termination is necessary, and if so, what is the best choice of termination.

In determining whether a transmission line being driven by a LV logic device needs to be terminated, two factors must be considered. The first factor to consider is the effect of discontinuities along the transmission line. The second is the relationship of the delay of the transmission line with the signal's edge rate.

The result of a poorly terminated line is reflected energy. This energy creates unwanted noise and will degrade system performance.

The result of proper termination is a quiet, high-performance system with minimal power supply drain. Good termination can be achieved with the use of a variety of schemes, two of which are ideal for LV logic.

Lossless Transmission Line



- Source Impedance = Z_S and Voltage Source = V_S
- Termination Impedance = Z_T
- Propagation Delay per Unit Length of a Lossless Transmission Line = t_{pd}
- Intrinsic Series Inductance Per Unit Length = L_O
- Intrinsic Shunt Capacitance Per Unit Length = $C_O = t_{pd}/Z_O$
- Characteristic Impedance of Lossless Transmission Line = $Z_O = \sqrt{\frac{L_O}{C_O}}$
- Reflection Coefficient at Termination = $\rho_T = \frac{Z_T - Z_O}{Z_T + Z_O}$
- Reflection Coefficient at Source = $\rho_S = \frac{Z_S - Z_O}{Z_S + Z_O}$

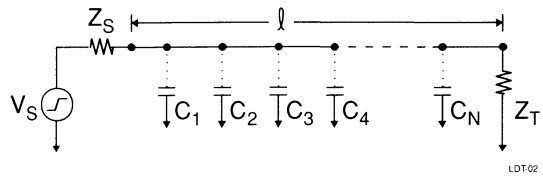
To begin with, let us review basic transmission line concepts.

A transmission line exists between any driving device and a receiving device. This transmission line is comprised of intrinsic series inductance, series resistance, and shunt capacitance.

Both the source and the destination of the signal have impedance. Should a mismatch of impedance occur between the signal source and the transmission line and/or the signal destination and the transmission line; a reflection will occur. The magnitude and direction of the reflection may be determined by calculating the reflection coefficients of the respective nodes.

No reflection will occur should the impedance of the source and the destination equal that of the transmission line. The reflection coefficient is zero.

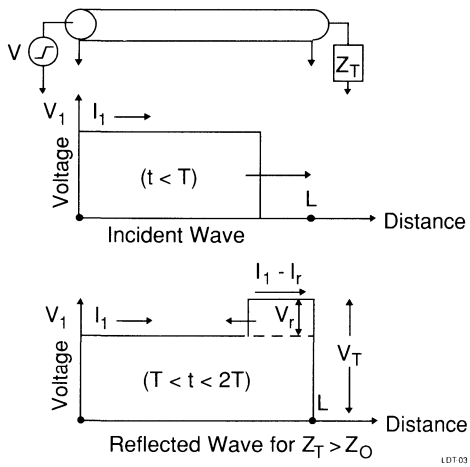
Transmission Line With Distributed Loading



- Length of Transmission Line = ℓ
- Distributed Load Capacitance per Unit Length = $C_D = \sum_{n=1}^{N} C_L / \ell$
- Characteristic Impedance of a Transmission Line = $Z'_O = \sqrt{\frac{L_O}{C_O + C_D}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_O}}}$
- Effective Reflection Coefficient at Termination = $\rho = \frac{Z_T - Z'_O}{Z_T + Z'_O}$

The previous slide illustrated reflections on a lossless transmission line. In a real system, transmission lines are often comprised of several loads distributed along those lines. The result is a lower impedance due to the added capacitance along the transmission line. This slide describes the equation that can be used to define a transmission line in a real system. Care should be used to ensure that the termination values chosen matches the effective impedance, Z'_O, rather than the lossless impedance Z_O.

Reflections for $Z_T > Z_O$



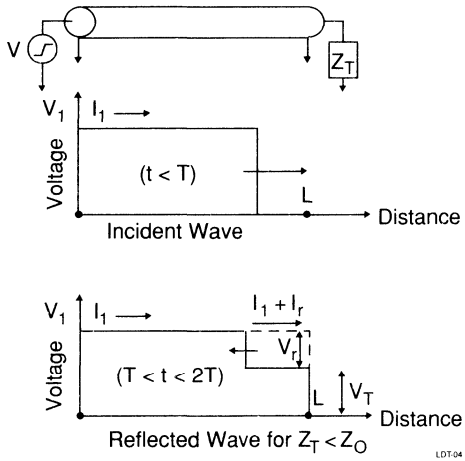
- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I_1
- Incident Wave Voltage = V_1
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

As the incident wave arrives at the end of the transmission line, if the impedance of the destination, or termination, is greater than the impedance of the transmission line, the reflection coefficient is positive and a positive voltage is reflected back to the source as illustrated.

The result is that the voltage swing observed at the receiving end of the transmission line has a substantial amount of overshoot generated by reflected energy. Often undershoot and overshoot is the result of reflected energy and is not caused by the driving device.

If LV logic drivers are being used to drive the transmission line, undershoot and overshoot in excess of 1.0 volts is most probably the effect of poor termination.

Reflection For $Z_T > Z_O$



- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I_1
- Incident Wave Voltage = V_1
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

As the incident wave arrives at the end of the transmission line, if the impedance of the destination, or termination, is less than the impedance of the transmission line, the reflection coefficient is negative, and a negative voltage is reflected back to the source as illustrated.

The result may be that several reflections are needed to achieve voltage levels at the receiver necessary to guarantee proper logic levels.

Terminations For LV Logic

WHEN DO WE USE TERMINATION?

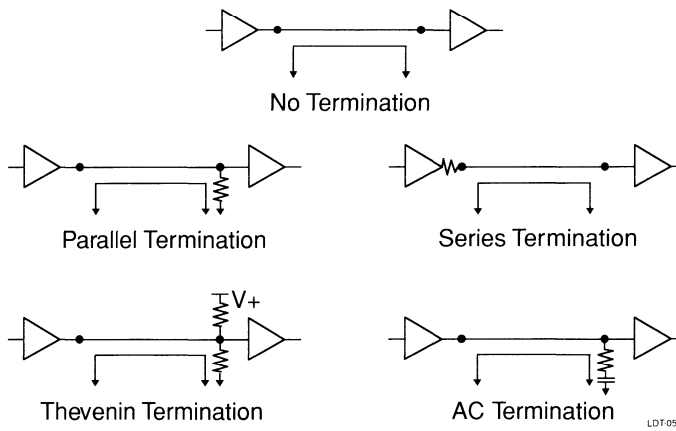
- Long Lines ($T_d > 1/3\ T_r$) should be terminated
- Typically, system backplanes should be terminated
- Noise critical signal lines should be terminated
  (e.g., lines prone to EMI, or asynchronous signal paths)

If the transmission line is short with respect to the edge rate of the incident signal then reflections will have no effect on the quality of the incident signal.

The length of the transmission line above which termination may be necessary is not absolute. A good rule of thumb is to carefully consider terminating a line whose delay exceeds one-third (1/3) the rise or fall time of the incident signal. For typical transmission lines in today's systems, this translates to approximately 20 centimeters (8 inches).

Signal lines in a backplane are generally longer than 20 centimeters and are prime candidates for termination.

Termination Circuits

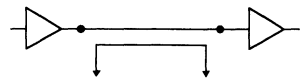


This section will discuss the attributes of four types of termination in addition to no termination. The most components a termination scheme may require is two per line.

Terminations for LV Logic

NO TERMINATION

- Lowest-cost solution
- Useful for line lengths < 20 cm (8 in.)



No Termination

LDT-06

For short lines, no termination may be necessary.

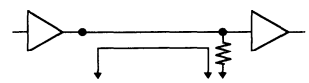
LCX inputs, have proprietary ESD protection circuitry on their inputs. The ESD circuitry do not fully terminate a line but will clamp some undershoot. There is no traditional upper ESD protection diode to clamp overshoot. In other words, LCX inputs (like all other 5V tolerant low voltage logic families) will exhibit high impedance in the face of overshoot beyond the supply voltage. Traditional 5V logic devices will clamp the input voltage to a diode drop above the supply voltage because they use a traditional upper diode ESD protection device.

Caution should be used when driving some PLDs, DACs, or DRAMs. These types of devices often have no input protection circuitry.

Terminations for LV Logic

PARALLEL TERMINATION

- Traditional bipolar solution
- Dissipates the most power
- Power dissipation is a function of the signal's duty cycle
- Has an unbalanced effect on the outputs
- Not generally recommended
- Best used when interfacing LV Logic to bipolar circuits



Parallel Termination

LDT-09

Parallel termination is a traditional bipolar termination. Bipolar logic typically dissipates a fairly high amount of DC power. The high level of DC current drain associated with parallel termination is not a concern in bipolar systems.

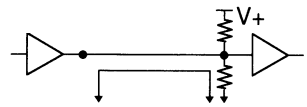
Parallel termination's heavy load increases the voltage drop at the output in either the HIGH or LOW logic state, depending on the rail to which the termination resistor is attached. This will cause an asymmetrical output pulse.

Do not connect the termination to a V_{CC} voltage which is different than the V_{CC} of all the devices on the bus. Doing so will allow current to flow between the different V_{CC}'s when the output of a device (with a non-termination V_{CC}) is in the high state.

Terminations For LV Logic

THEVENIN TERMINATION

- Power dissipation is comparable to parallel termination, but is duty cycle independent
- Traditional bipolar termination
- Has a balanced effect on the outputs
- Not generally recommended
- Lines with Thevenin termination should not be left floating



Thevenin Termination

LDT-11

Thevenin termination is much like parallel termination, except that Thevenin termination has a balanced effect on the output voltage. It too, is a popular terminating technique for bipolar systems. It is often found in popular bus protocols such as VME and Multibus.

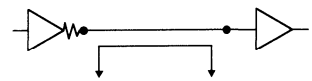
Again, this termination scheme is not recommended for use in LV CMOS systems because of its high DC current drain.

A note of caution: lines terminated with a Thevenin termination should not be floated or tri-stated, because the Thevenin termination voltage divider may pull inputs to voltage near the threshold voltage of the device. High power consumption will result and any noise on this DC signal may cause the device to falsely switch or even oscillate (possibly damaging the device). As with parallel termination, do not use different device and termination V_{CC}'s.

Terminations For LV Logic

SERIES TERMINATION

- Lowest power consumption of all termination circuits, including no termination
- Reduces crosstalk on adjacent lines
- Excellent for point loads
- Not recommended for distributed loads



Series Termination

LDT-13

Series termination is one of the two types of termination schemes recommended for LV CMOS logic. It is the lowest-power termination technique, along with no termination.

This type of termination divides the line voltage in half. The reflection created at the end of the line doubles the voltage back up to its original value.

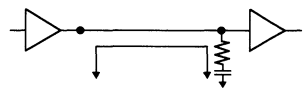
Since the voltage swing along the line is one-half of the driver output, this type of termination may reduce the amplitude of any crosstalk created on an adjacent line.

As any receiver located along the line, other than at the very end, will have to wait for a reflection to double its input voltage, this type of termination is recommended for point loads only. That is, a single receiver at the end of the transmission line.

Terminations For LV Logic

AC TERMINATION

- A capacitor used to block DC current drain which reduces power requirements
- For low frequency signals, the capacitor acts like an additional load capacitance
- AC power rolls off at higher frequencies
- The additional component will increase your manufacturing cost
- Ideal for distributed loads



AC Termination

LDT-15

AC termination is the second of the two types of termination recommended for LV CMOS logic.

AC termination contributes zero DC power dissipation since driving current through the capacitor requires a voltage transition.

AC power dissipation is similar to that of no termination. However, as the frequency of the incident signal increases, AC power dissipation for AC terminated lines decreases.

This termination technique is recommended for transmission lines driving distributed receivers.

Terminations For LV Logic

TERMINATION VALUES

- Parallel: Resistor = Z_O
- Thevenin: Resistor = 2 X Z_O
- Series: Resistor = $Z_O - Z_{OUT}$
- AC: Resistor = Z_O

  Capacitor = $C > \frac{3t_r}{Z_O}$

The objective of selecting a termination value is generally to achieve a reflection coefficient of zero. Therefore the termination impedance must equal that of the transmission line. The exception is the series termination, in which the reflection coefficient is forced to be one.

For series termination calculations the output impedance of a typical LCX device is 15 ohms.

The values listed in these equations are not absolute. Since the number and location of the loads and other transmission line effects will alter the total line impedance the termination values chosen may not be optimal. For better results it is helpful to prototype with variable components and select termination values based on actual signal quality.

How is the capacitor value chosen for the AC termination?

f = frequency

C = AC termination capacitance

Z_O = Characteristic impedance of the transmission line

t_r = The faster of the rise or fall time

Let: $1/(2 * f * C * \pi) = 0.1 * Z_O$

$C = 5/(\pi * Z_O * f)$

Let: $f = 1/(t_r + t_f) = 1/2 * t_r$

Then: $C = (10 * t_r)/(\pi * Z_O)$ or

C = approximately $3 * t_r/Z_O$

Termination Summary

- **Parallel Termination**—Popular bipolar solution. Not recommended for LV CMOS logic because of its high power dissipation
- **Thevenin Termination**—Popular bipolar solution. Found in many standard bus protocols. Not recommended for LV CMOS logic because of its high power dissipation
- **Series Termination**—Good LV CMOS logic termination. Recommended for termination point loads. Lowest-power termination scheme
- **AC Parallel Termination**—Good LV CMOS logic termination. Recommended for terminating distributed loads

In bipolar applications, the selection of the lowest-power termination technique may not be critical. However, in LV CMOS logic applications where power is one of the major considerations, selection of the lowest-power termination solution is vital in achieving the highest performance system available.

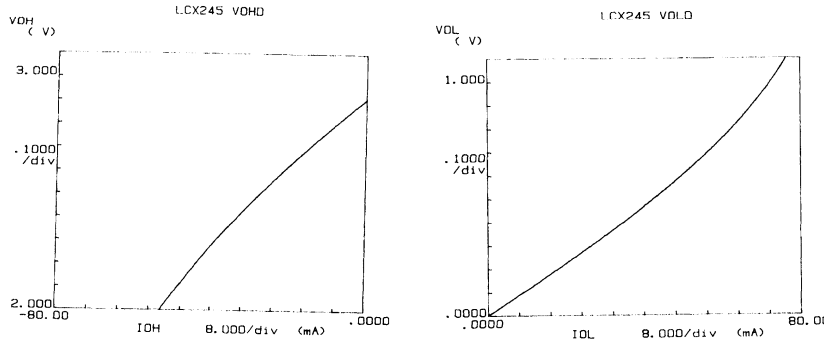
LCX Line Driving and Termination Performance

LCX 75Ω Line Driving Capability

- Objective
  - To be able to switch at incident wave into a 75Ω line impedance
  - Switching from 0.1 volts to 2.0 volts is a swing of 1.9 volts. We need to source 25 mA (1.9V ÷ 75Ω)
  - And switch from 3.6 volts to .8 volts or swing through 2.4 volts. We therefore need to sink 36 mA (2.4V ÷ 75Ω)

Here we describe the objective for our output circuit specification and a simple calculation that demonstrates the switching capability of 75 ohm drive. The dynamic drive characteristic to sink and source the dynamic drive current necessary to drive a 75 ohm line is +36/-25mA respectively.

Output Characteristics

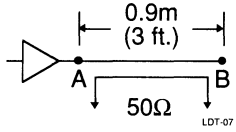


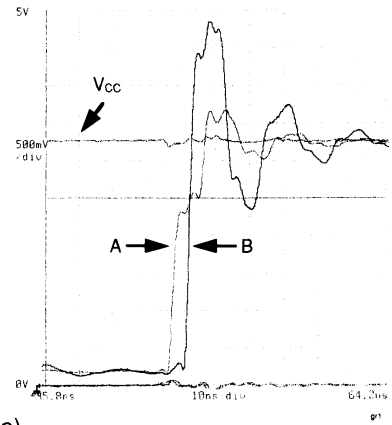
Dynamic drive

- V_{OHD}
- V_{OLD}

Here are plots of the dynamic drive capability of LCX245. As can be seen here the LCX245 is capable of supplying more than enough drive to drive a 75 ohm line. Note that the dynamic drive capability of the LCX family allows it to drive a 75Ω line with incident wave switching even though its static output drive capability is specified at ±24mA.

LCX Driving 0.9m (3ft.) 50Ω Open Ended Coax Cable*



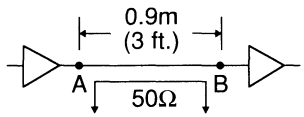


* RG-174/U coaxial cable (50 Ω impedance)

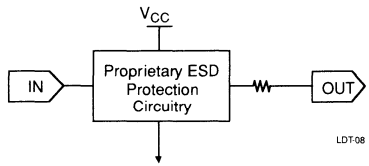
This oscillograph illustrates a large positive reflection at the end of a three-foot 50Ω open-ended transmission line. Theoretically the reflection coefficient is 1 and the reflected voltage is equal to the incident voltage. The result is a doubling of the incident voltage at the end of the transmission line.

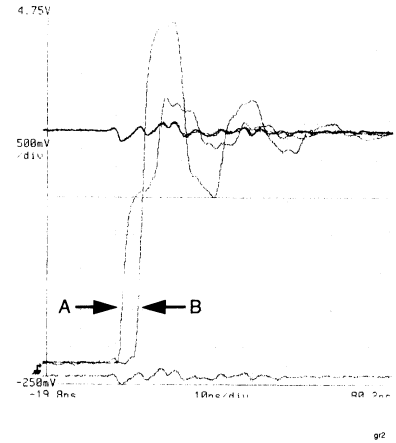
The oscillograph shows a large overshoot. A similar effect would be seen on a high-to-low transition in the form of a large undershoot. Obviously proper termination would be desirable.

LCX Driving LCX



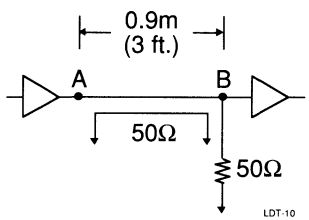
LCX Input Protection Network

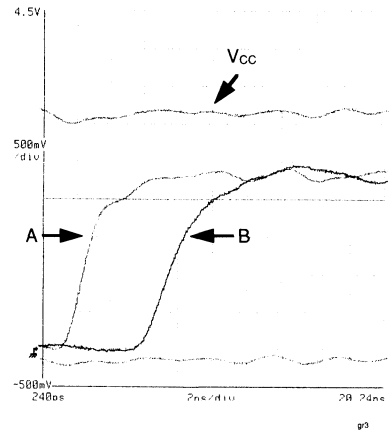




This oscillograph illustrates the effect of an LCX receiver at the end of the same 50Ω transmission line. Again, termination should be used in this case to better match the impedance of the cable.

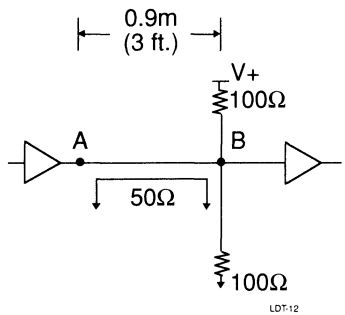
LCX Driving LCX With Parallel Termination

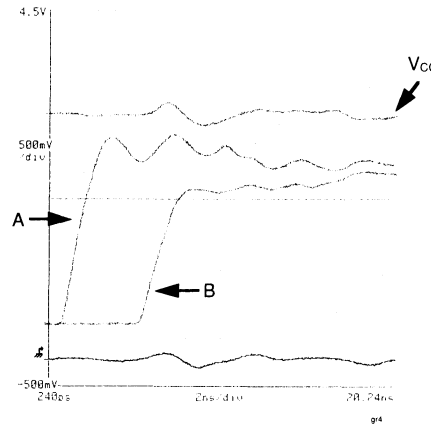




This oscillograph illustrates the unbalanced effect that parallel termination has on output voltage. The signal is well terminated and valid logic levels at the receiver are easily achieved.

LCX Driving LCX With Thevenin Termination





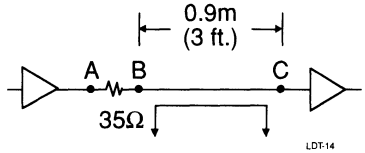
V_{CC}

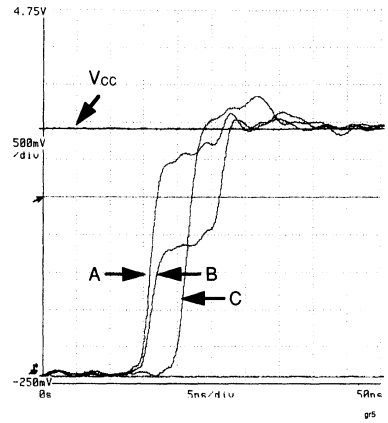
This oscillograph illustrates the symmetrical voltage swing of outputs driving Thevenin-terminated lines.

Valid logic levels are again achieved.

If the output of device A is TRI-STATE, the line voltage at point B will be pulled to V+/2 which may be near the threshold of device B. This can cause two problems. Device B may oscillate and will consume large amounts of current due to shoot-through effects (upper and lower CMOS transistor structures are "soft on"). Therefore, care must be taken when using Thevenin termination.

LCX Driving LCX With Series Termination





This oscillograph illustrates the effect of the series resistor on the line voltage. The line voltage does not reach the rail for a time which varies between one and two line delays.

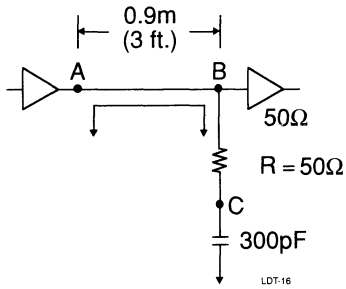
The voltage at the end of the transmission line, point C, is equal to that of the output of the driver, point A.

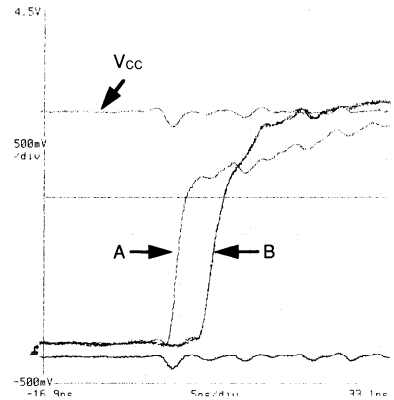
The on-resistance of a output is approximately 15 ohms. The value of the termination resistor should be the line impedance, Z_O, minus the output impedance of the LV CMOS driver. Therefore,

$$R_t = Z_0 - R_{out}$$
$$= 50W - 15W$$
$$= 35W$$

in this case.

LCX Driving LCX With AC Termination

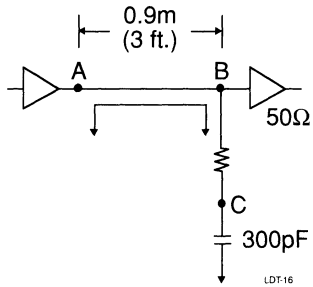


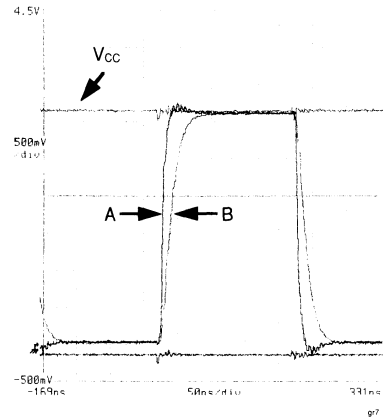


Frequency: 1 MHz

This oscillograph illustrates the effectiveness of AC termination. Like with parallel termination, proper termination is achieved, but the capacitor blocks DC power loss.

LCX Driving LCX With AC Termination



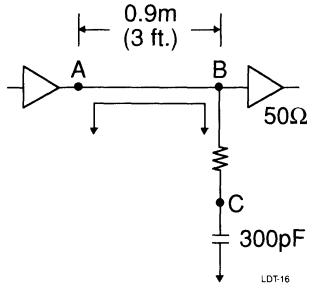


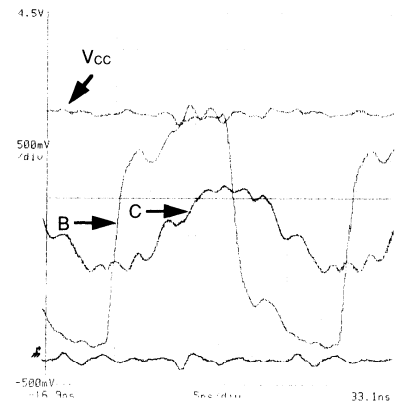
Frequency: 2.5 MHz

Depending on the value chosen for the AC termination, at low frequencies the termination capacitor must be included in the calculation of the load capacitance.

This oscillograph illustrates that a termination capacitor of 300 pF fully charges and discharges at 2.5 MHz.

LCX Driving LCX With AC Termination





Frequency: 30 MHz

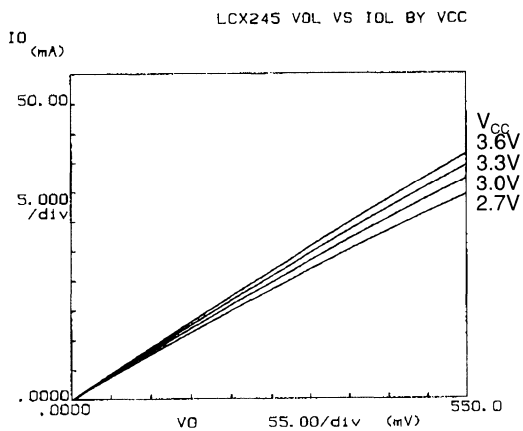
At 30 MHz the termination capacitor is never fully charged or discharged and should not be included in the calculation of load capacitance.

Output Drive (V_{OL}/I_{OL}, V_{OH}/I_{OH})

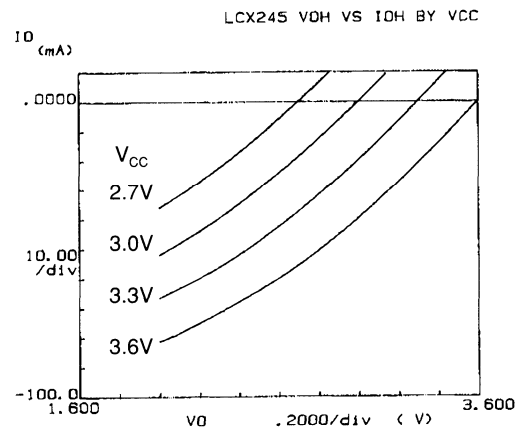
The following plots show the output drive characteristics of LCX devices for different values of V_{CC}. These are useful for determining the suitability of LCX for high drive applications.

LCX Output Drive vs. V_{CC}

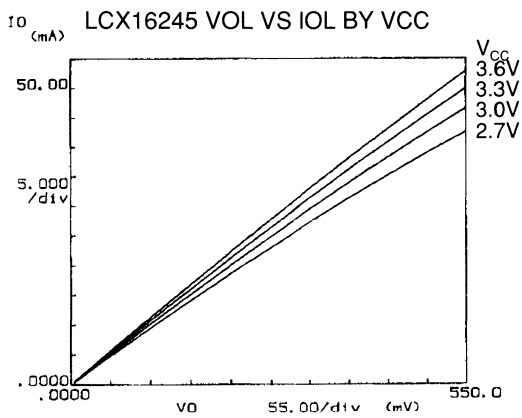
LCX245 VOL VS IOL BY VCC



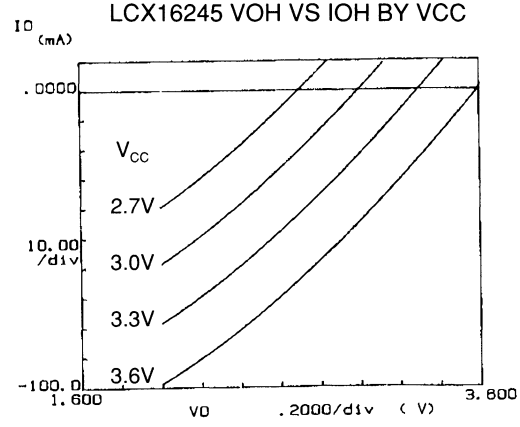
LCX245 VOH VS IOH BY VCC



LCX16245 VOL VS IOL BY VCC



LCX16245 VOH VS IOH BY VCC



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